DRV8848 双路 H 桥电机驱动器

1 特性

- 双路 H 桥电机驱动器
  - 单通道/双通道刷式直流
  - 步进
- 脉宽调制 (PWM) 控制接口
- 可选电流调节，具有 20μs 固定关断时间
- 每个 H 桥均提供高输出电流
  - 最大驱动器电流为 2A（12V 且 T_A = 25°C 时）
  - 并联模式下最大驱动器电流为 4A（12V 且 T_A = 25°C 时）
- 工作电源电压范围为 4V 至 18V
- 3μA 低电流睡眠模式
- 散热增强型表面贴装封装
- 保护特性
  - VM 欠压闭锁 (UVLO)
  - 过流保护 (OCP)
  - 热关断 (TSD)
  - 故障条件指示引脚 (nFAULT)

2 应用

- 电器
- 通用刷式电机和步进电机
- 打印机

3 说明

DRV8848 为家用电器和其它机电一体化应用提供了一款双路 H 桥电机驱动器。 该器件可用于驱动一个或两个直流电机、一个双极性步进电机或其它负载。 利用一个简单的 PWM 接口便可轻松连接到控制器电路。

每个 H 桥驱动器的输出块都包含配置为全 H 桥的 N 通道和 P 通道功率 MOSFET，用于驱动电机绕组。 每个 H 桥都含有一个调节电路，可通过固定关断时间斩波方案调节绕组电流。 DRV8848 能够从每个输出驱动高达 2A 电流，在并联模式下驱动高达 4A 电流（正常散热，12V 且 T_A = 25°C 时）。

低功耗睡眠模式可将部分内部电路关断，从而实现极低的静态电流和功耗。 这种睡眠模式可通过专用的 nSLEEP 引脚来设定。

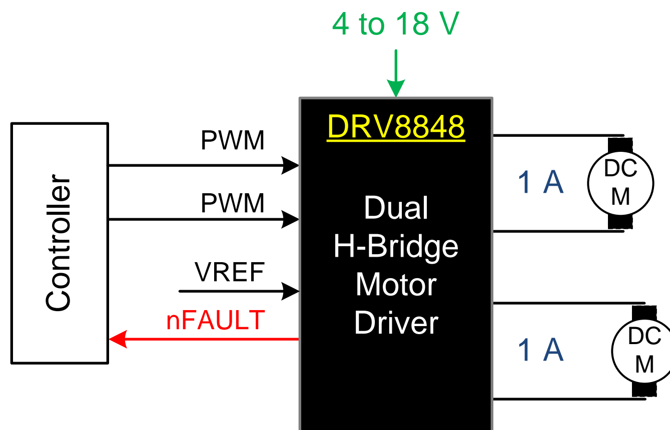
还提供用于 UVLO、OCP、短路保护和过热保护的内部保护功能。 故障条件通过 nFAULT 引脚指示。

器件信息(1)

部件号	封装	封装尺寸（标称值）
DRV8848	HTSSOP (16)	5.00mm x 6.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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5 修订历史记录

日期	修订版本	注释
2014 年 10 月	*	最初发布。

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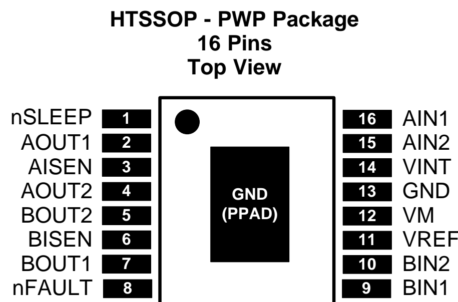
6 Pin Configuration and Functions

HTSSOP - PWP Package
16 Pins
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	NO.			
AIN1	16	I	Bridge A input 1	Controls AOUT1; tri-level input
AIN2	15	I	Bridge A input 2	Controls AOUT2; tri-level input
AISEN	3	O	Winding A sense	Connect to current sense resistor for bridge A, or GND if current regulation is not required
AOUT1	2	O	Winding A output	
AOUT2	4			
BIN1	9	I	Bridge B input 1	Controls BOUT1; internal pulldown
BIN2	10	I	Bridge B input 2	Controls BOUT2; internal pulldown
BISEN	6	O	Winding B sense	Connect to current sense resistor for bridge A, or GND if current regulation is not required
BOUT1	7	O	Winding B output	
BOUT2	5			
GND	13	PWR	Device ground	Both the GND pin and device PowerPAD must be connected to ground
	PPAD			
nFAULT	8	OD	Fault indication pin	Pulled logic low with fault condition; open-drain output requires external pullup
nSLEEP	1	I	Sleep mode input	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
VINT	14	—	Internal regulator	Internal supply voltage; bypass to GND with 2.2-µF, 6.3-V capacitor
VM	12	PWR	Power supply	Connect to motor power supply; bypass to GND with a 0.1- and 10-µF (minimum) ceramic capacitor rated for VM
VREF	11	I	Full-scale current reference input	Voltage on this pin sets the full scale chopping current; short to VINT if not supplying an external reference voltage

External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM}	VM	GND	10-µF (minimum) ceramic capacitor rated for VM
C_{VM}	VM	GND	0.1-µF ceramic capacitor rated for VM
C_{VINT}	VINT	GND	6.3-V, 2.2-µF ceramic capacitor
R_{nFAULT}	VCC[(1)]	nFAULT	>1 kΩ
R_{AISEN}	AISEN	GND	Sense resistor, see *Typical Application* for sizing
R_{BISEN}	BISEN	GND	Sense resistor, see *Typical Application* for sizing

(1) VCC is not a pin on the DRV8848, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to VINT

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) [1]

		MIN	MAX	UNIT
	Power supply voltage (VM)	–0.3	20	V
	Power supply voltage ramp rate (VM)	0	2	V/µs
	Internal regulator voltage (VINT)	–0.3	3.6	V
	Analog input pin voltage (VREF)	–0.3	3.6	V
	Control pin voltage (AIN1, AIN2, BIN1, BIN2, nSLEEP, nFAULT)	–0.3	7	V
	Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–0.3	VM + 0.6	V
	Continuous shunt amplifier input pin voltage (AISEN, BISEN) [2]	–0.6	0.6	V
	Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN)	Internally limited		A
T_J	Operating junction temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	–4	4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	–1.5	1.5	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{VM}	Power supply voltage range [1]	4	18	V
V_{VREF}	Reference rms voltage range [2]	1	3.3	V
f_{PWM}	Applied STEP signal	0	250	kHz
I_{VINT}	VINT external load current		1	mA
I_{rms}	Motor rms current per H-bridge [3]	0	1	A
T_A	Operating ambient temperature	–40	85	°C

(1) Note that $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V.
(2) Operational at VREF between 0 and 1 V, but accuracy is degraded.
(3) Power dissipation and thermal limits must be observed.

7.4 Thermal Information

THERMAL METRIC [1]		PWP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	28.7	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	11.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VINT)						
V_{VM}	VM operating voltage		4		18	V
I_{VM}	VM operating supply current	V_{VM} = 12 V, excluding winding current, nSLEEP = 1	2.5	3.8	5.5	mA
I_{VMQ}	VM sleep mode supply current	V_{VM} = 12 V, nSLEEP = 0	0.5	1.2	3	μA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep mode			1	ms
t_{WAKE}	Wake time	nSLEEP = 1 to output transition			1	ms
t_{ON}	Power-on time	V_{VM} > V_{UVLO} rising to output transition			1	ms
V_{INT}	VINT voltage	V_{VM} > 4 V, I_{OUT} = 0 A to 1 mA	3.13	3.3	3.47	V
LOGIC-LEVEL INPUTS (BIN1, BIN2, NSLEEP)						
V_{IL}	Input logic low voltage		0		0.7	V
V_{IH}	Input logic high voltage		1.6		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_{IN} = 0 V	–1		1	μA
I_{IH}	Input logic high current	V_{IN} = 5 V	1		30	μA
R_{PD}	Pulldown resistance	BIN1, BIN2		200		kΩ
		nSLEEP		500		
t_{DEG}	Input deglitch time	AIN1 or AIN2		400		ns
		BIN1 or BIN2		200		ns
t_{PROP}	Propagation delay	AIN1 or AIN2 edge to output change		800		ns
		BIN1 or BIN2 edge to output change		400		ns
TRI-LEVEL INPUTS (AIN1, AIN2)						
V_{IL}	Tri-level input logic low voltage		0		0.7	V
V_{IZ}	Tri-level input Hi-Z voltage			1.1		V
V_{IH}	Tri-level input logic high voltage		1.6		5.5	V
V_{HYS}	Tri-level input hysteresis		100			mV
I_{IL}	Tri-level input logic low current	V_{IN} = 0 V	–30		–1	μA
I_{IH}	Tri-level input logic high current	V_{IN} = 5 V	1		30	μA
R_{PD}	Tri-level pulldown resistance	To GND		170		kΩ
R_{PU}	Tri-level pullup resistance	To VINT		340		kΩ
CONTROL OUTPUTS (NFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	V_O = 3.3 V	–1		1	μA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	V_{VM} = 12 V, I = 0.5 A, T_J = 25°C		550		Ω
		V_{VM} = 12 V, I = 0.5 A, T_J = 85°C[(1)]		660		
$R_{DS(ON)}$	Low-side FET on resistance	V_{VM} = 12 V, I = 0.5 A, T_J = 25°C		350		Ω
		V_{VM} = 12 V, I = 0.5 A, T_J = 85°C[(1)]		420		
I_{OFF}	Off-state leakage current	V_{VM} = 5 V, T_J = 25°C	–1		1	μA
t_{RISE}	Output rise time			60		ns
t_{FALL}	Output fall time			60		ns
t_{DEAD}	Output dead time	Internal dead time		200		ns
PWM CURRENT CONTROL (VREF, AISEN, BISEN)						
I_{REF}	Externally applied VREF input current	V_{VREF} = 1 to 3.3 V			1	μA
V_{TRIP}	xISEN trip voltage	For 100% current step with V_{VREF} = 3.3 V		500		mV

(1) Not tested in production; limits are based on characterization data

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Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BLANK}	Current sense blanking time			1.8		μs
A_{ISENSE}	Current sense amplifier gain	Reference only		6.6		V/V
t_{OFF}	Current control constant off time			20		μs
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	V_{VM} falling; UVLO report			2.9	V
		V_{VM} rising; UVLO recovery			3	
I_{OCP}	Overcurrent protection trip level		2			A
t_{DEG}	Overcurrent deglitch time			2.8		μs
t_{OCP}	Overcurrent protection period			1.6		ms
T_{TSD} [(1)]	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C
T_{HYS} [(1)]	Thermal shutdown hysteresis	Die temperature T_J		50		°C

7.6 Timing Requirements

T_A = 25°C, over recommended operating conditions unless otherwise noted

NO.	PARAMETER		MIN	MAX	UNIT
1	t_1	Delay time, xIN1 to xOUT1	100	600	ns
2	t_2	Delay time, xIN2 to xOUT1	100	600	ns
3	t_3	Delay time, xIN1 to xOUT2	100	600	ns
4	t_4	Delay time, xIN2 to xOUT2	100	600	ns
5	t_F	Output rise time	50	150	ns
6	t_R	Output fall time	50	150	ns

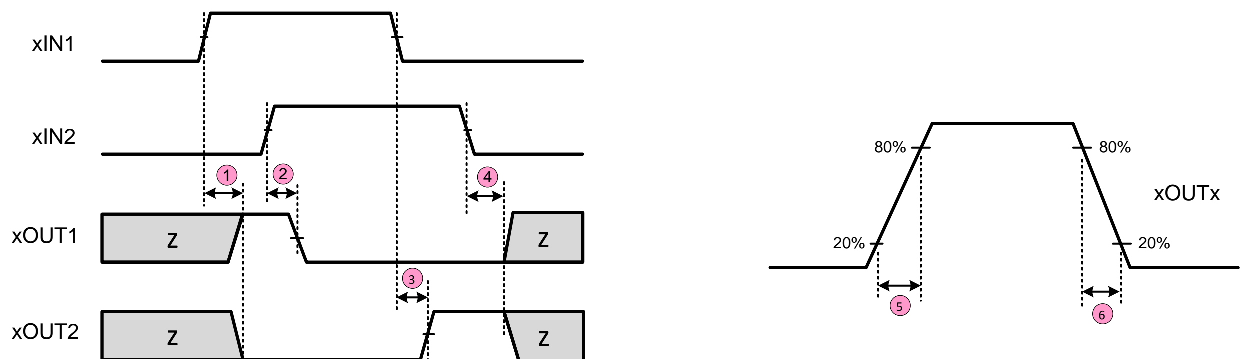

Figure 1. Timing Diagram

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7.7 Typical Characteristics

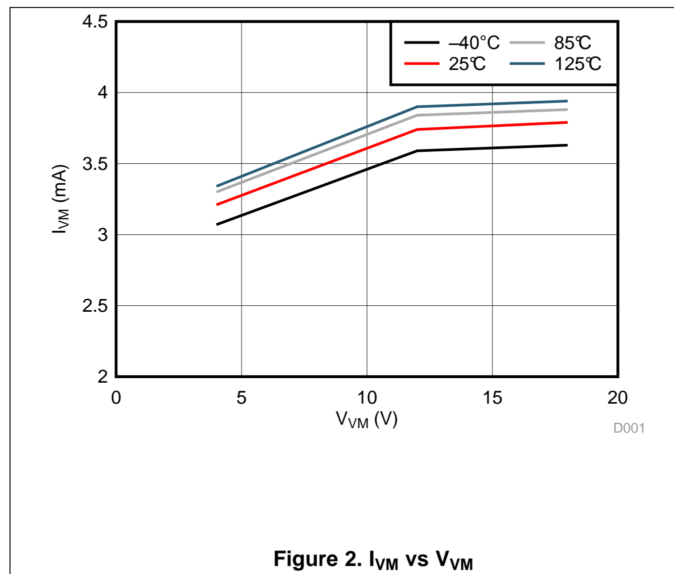

Figure 2. I_{VM} vs V_{VM}

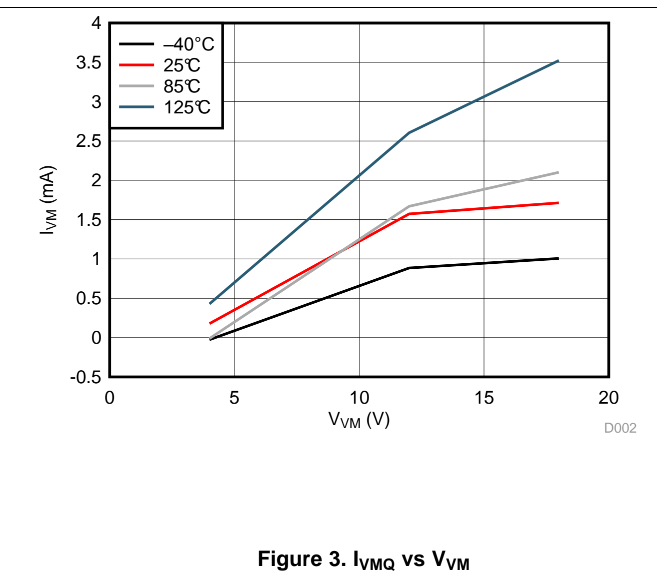

Figure 3. I_{VMQ} vs V_{VM}

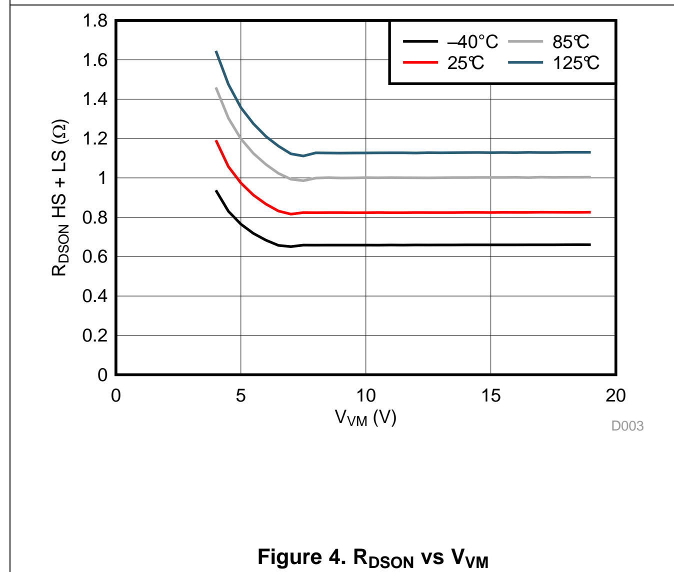

Figure 4. R_{DSON} vs V_{VM}

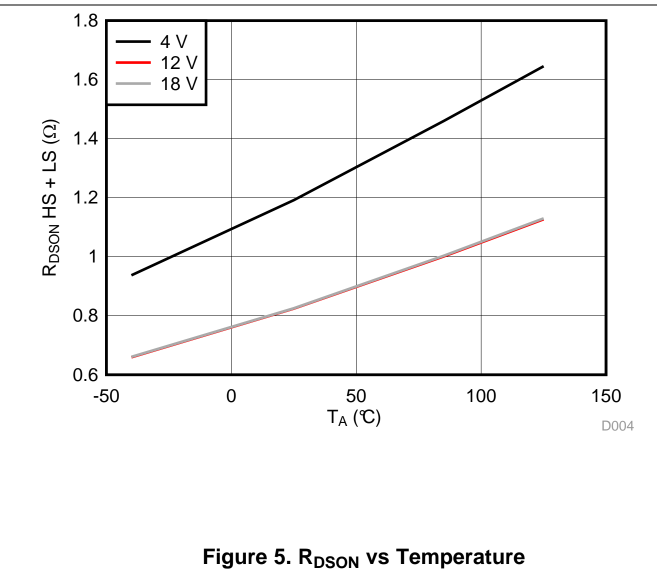

Figure 5. R_{DSON} vs Temperature

8 Detailed Description

8.1 Overview

The DRV8848 is an integrated motor driver solution for two DC motors or a bipolar stepper motor. The device integrates two H-bridges that use NMOS low-side drivers and PMOS high-side drivers and current sense regulation circuitry. The DRV8848 can be powered with a supply range between 4 to 18 V and is capable of providing an output current to 1-A rms.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation uses a fixed off-time (t_{OFF}) PWM scheme. The current regulation trip point is controlled by the value of the sense resistor and the voltage applied to VREF.

A low-power sleep mode is included, which allows the system to save power when not driving the motor.

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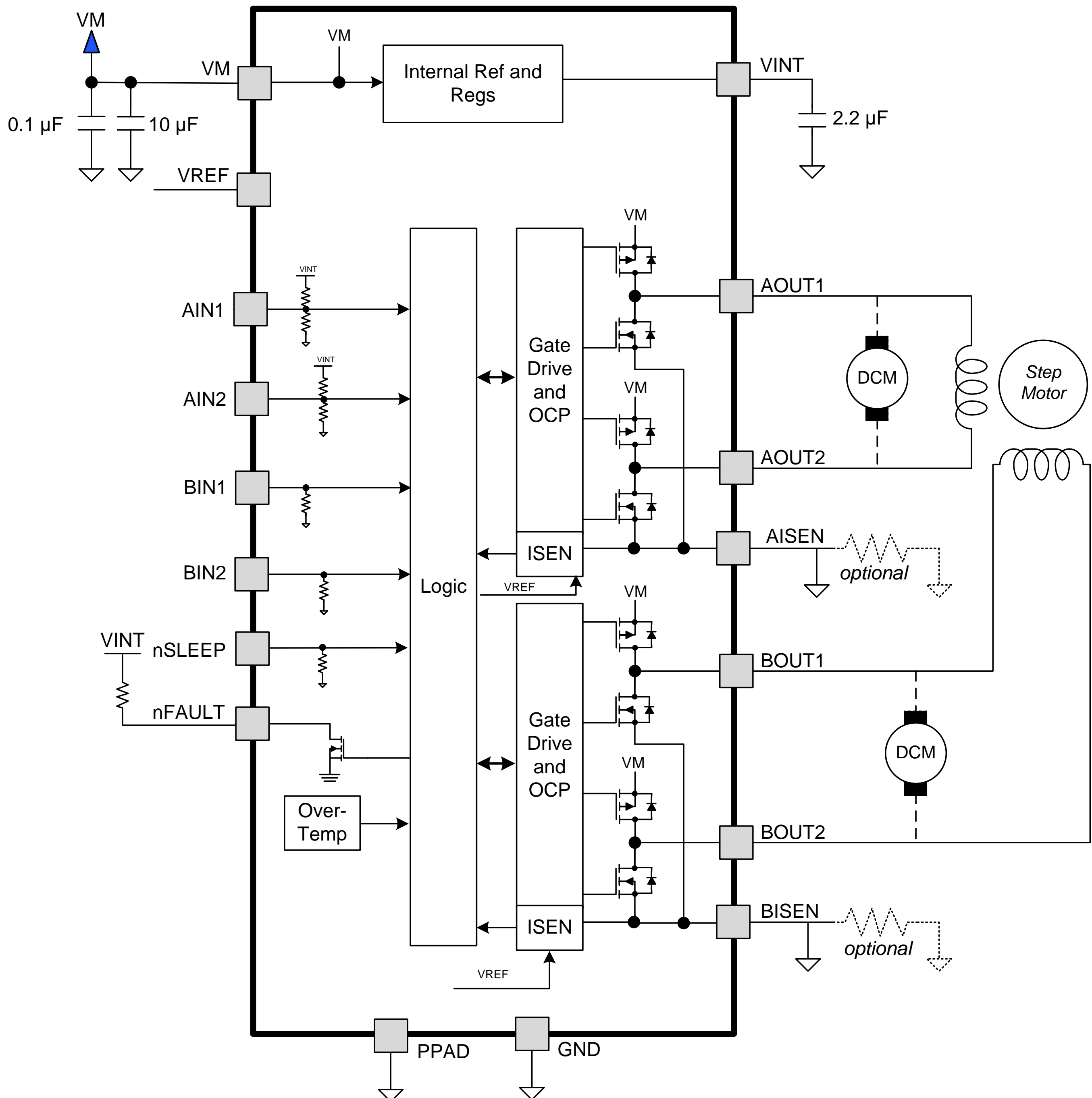
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM Motor Drivers

DRV8848 contains two identical H-bridge motor drivers with current-control PWM circuitry. Figure 6 shows a block diagram of the circuitry.

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Feature Description (continued)

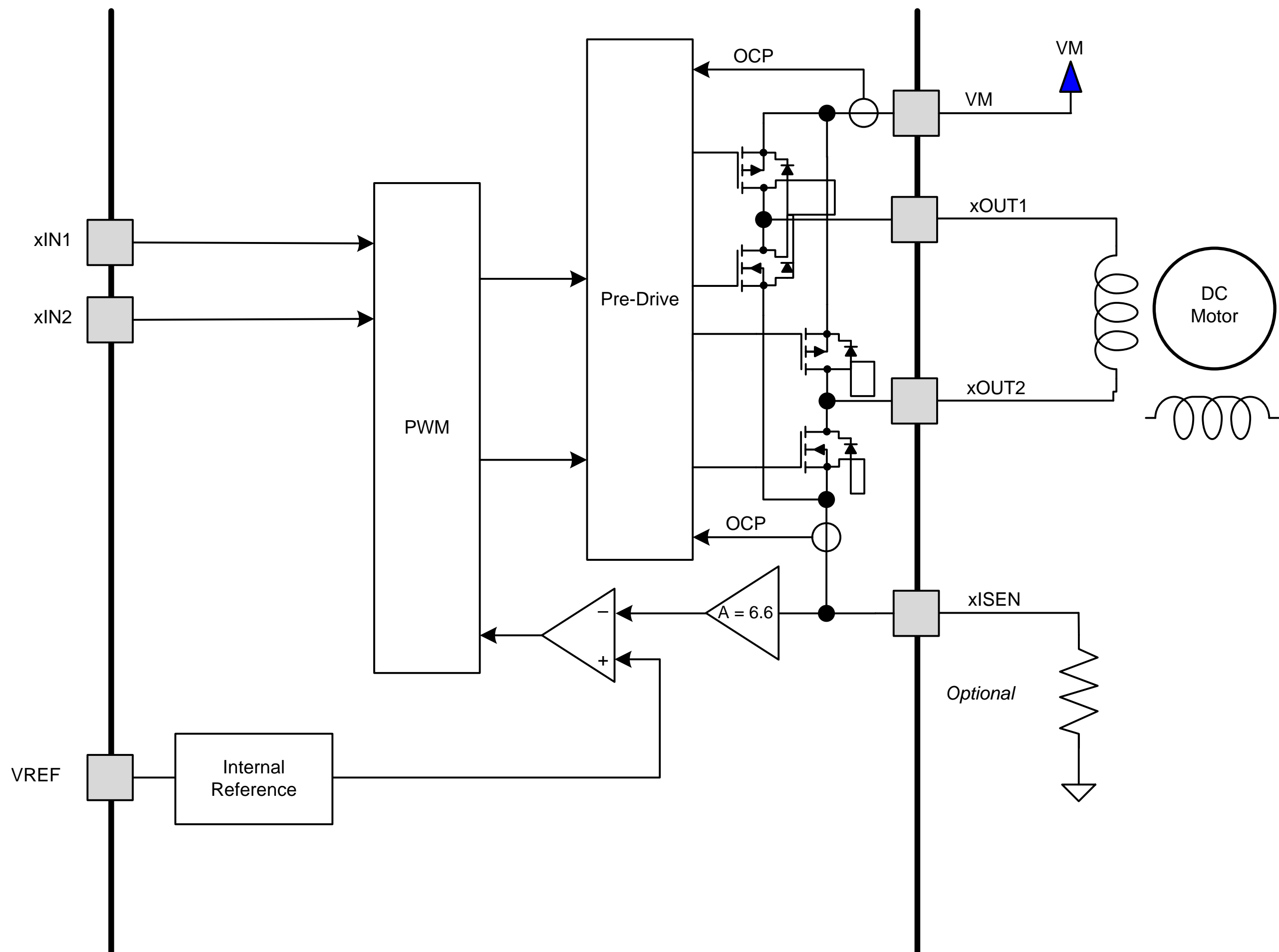

Figure 6. PWM Motor Driver Circuitry

8.3.2 Bridge Control

Table 1 shows the logic for the inputs xIN1 and xIN2.

Table 1. Bridge Control

xIN1	xIN2	xOUT1	xOUT2	Function (DC Motor)
0	0	Z	Z	Coast (fast decay)
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake (slow decay)

NOTE

Pins AIN1 and AIN2 are tri-level, so when they are left Hi-Z, they are not internally pulled to logic low. When AIN1 or AIN2 are set to Hi-Z and not in parallel mode, the output driver maintains the previous state.

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8.3.3 Parallel Operation

The two drivers can be used in parallel to deliver twice the current to a single motor. To enter parallel mode, AIN1 and AIN2 must be left Hi-Z during power-up or when exiting sleep mode (nSLEEP toggling from 0 to 1). BIN1 and BIN2 are used to control the drivers. Tie AISEN and BISEN to a single sense resistor if current control is desired. To exit parallel mode, AIN1 and AIN2 must be driven high or low and the device must be powered-up or exit sleep mode. Figure 7 shows a block diagram of the device using parallel mode.

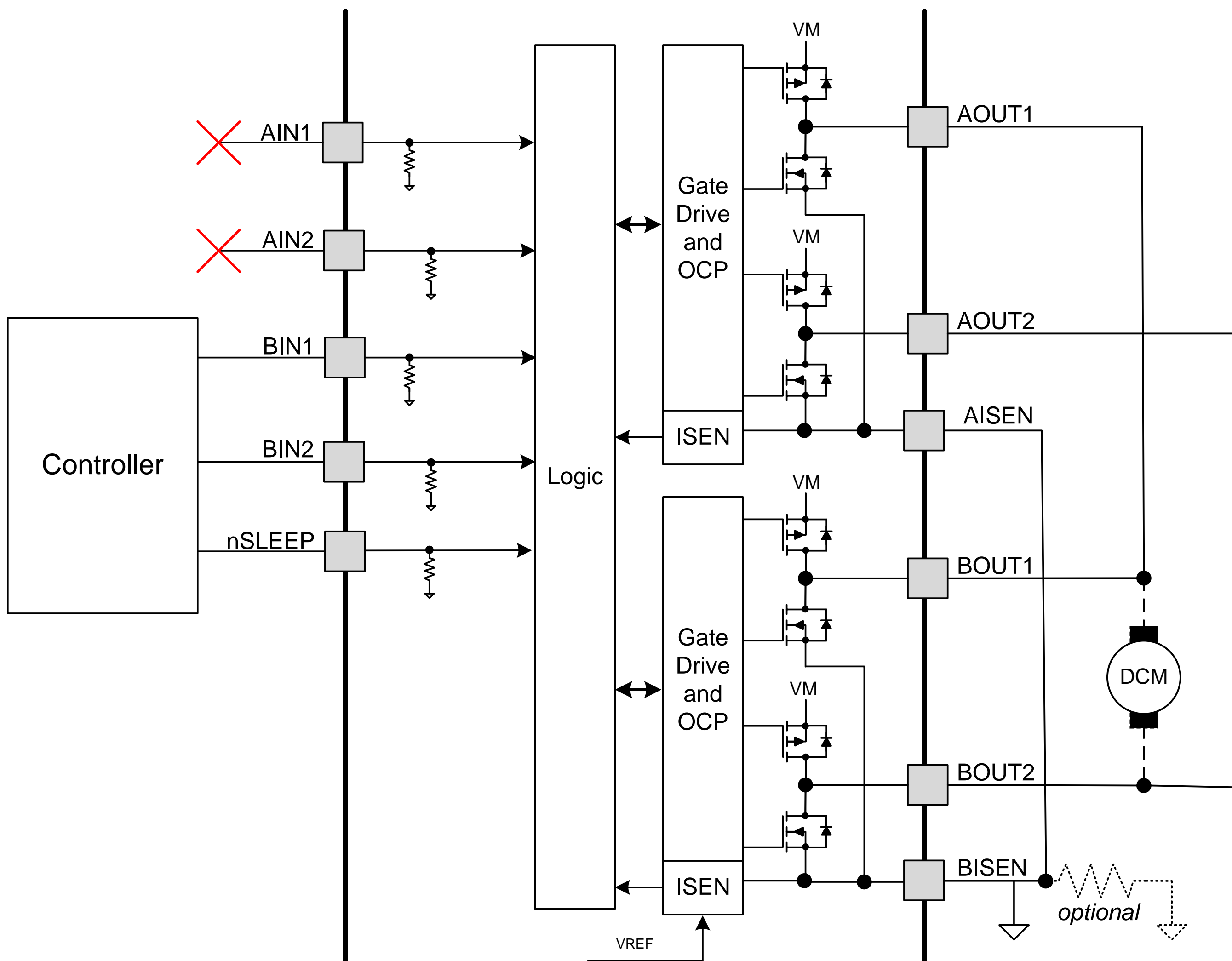

Figure 7. Parallel Mode Operation

8.3.4 Current Regulation

The current through the motor windings is regulated by a fixed-off-time PWM current regulation circuit. With DC brushed motors, current regulation can be used to limit the stall current (which is also the startup current) of the motor.

Current regulation works as follows:

When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current for a time t_{OFF} before starting the next PWM cycle. Note that immediately after the current is enabled, the voltage on the xISEN pin is ignored for a period of time (t_{BLANK}) before enabling the current sense circuitry. This blanking time also sets the minimum on-time of the PWM cycle.

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The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor, connected to the xISEN pin, with a reference voltage. The reference voltage is derived from the voltage applied to the VREF pin and it is V_{VREF} / 6.6. The VREF pin can be tied, on board, to the 3.3 V – VINT pin, or it can be externally forced to a desired VREF voltage.

The full scale chopping current in a winding is calculated as follows:

$$I_{FS} = \frac{V_{VREF}}{6.6 \times R_{ISENSE}}$$

where

- I_{FS} is the regulated current.
- V_{VREF} is the voltage on the VREF pin.
- R_{ISENSE} is the resistance of the sense resistor. (1)

Example: If V_{VREF} is 3.3 V and a 500-mΩ sense resistor is used, the full-scale chopping current is 3.3 V / (6.6 × 500 mΩ) = 1 A.

Note that if the current control is not needed, the xISEN pins may be connected directly to ground. In this case, VREF should be connected to VINT.

8.3.5 Current Recirculation and Decay Modes

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached (see case 1 in Figure 8).

After the chopping current threshold is reached, the drive current is interrupted, but due to the inductive nature of the motor, current must continue to flow for some period of time. This is called recirculation current. To handle this recirculation current, the DRV8848 H-bridge operates in mixed decay mode.

Mixed decay is a combination of fast and slow decay modes. In fast decay mode, the opposite drivers are turned on to allow the current to decay (see case 2 in Figure 8). If the winding current approaches zero, while in fast decay, the bridge is disabled to prevent any reverse current flow. In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge (see case 3 in Figure 8). Mixed decay starts with fast decay, then goes to slow decay. In DRV8848, the mixed decay ratio is 25% fast decay and 75% slow decay (as shown in Figure 9).

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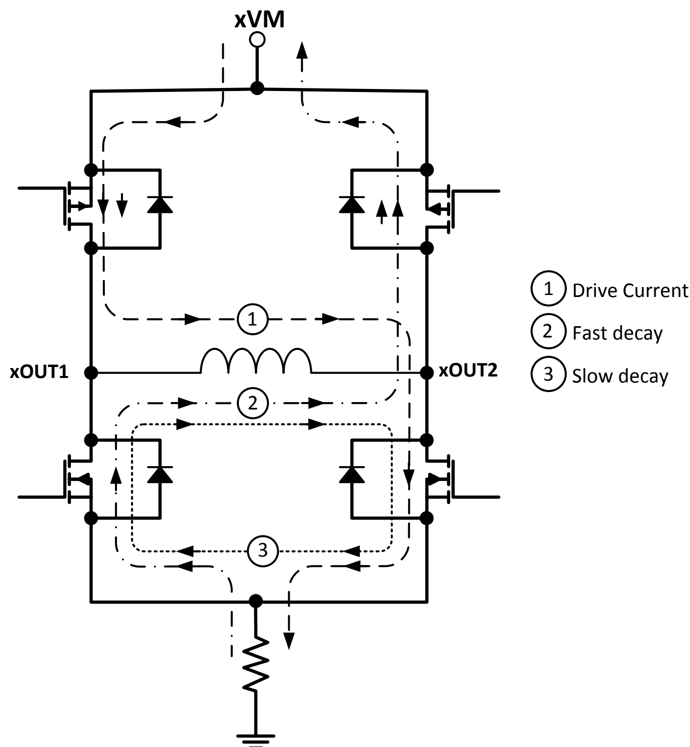

Figure 8. Decay Modes

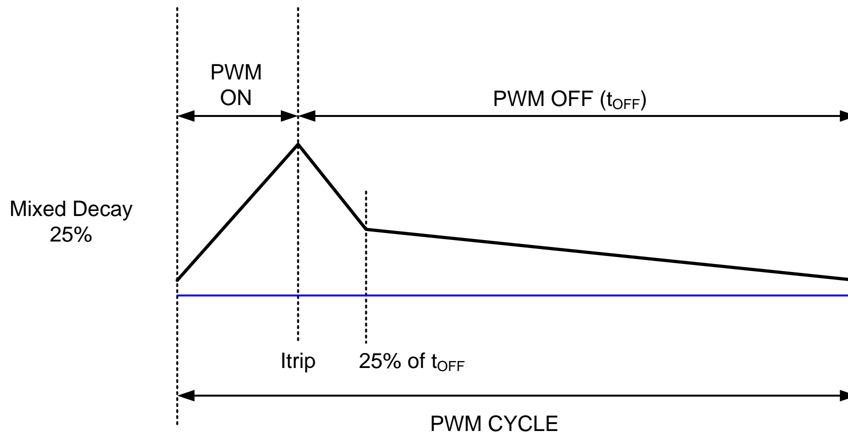

Figure 9. Mixed Decay

8.3.6 Protection Circuits

The DRV8848 is fully protected against undervoltage, overcurrent, and overtemperature events.

8.3.6.1 OCP

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time t_{OCP}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until the retry time t_{RETRY} occurs. The OCP is independent for each H-bridge.

Overcurrent conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an OCP event. Note that OCP does not use the current sense circuitry used for PWM current control, so OCP functions even without presence of the xISEN resistors.

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8.3.6.2 TSD

If the die temperature exceeds safe limits T_{TSD}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed.

8.3.6.3 UVLO

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when V_{VM} rises above the UVLO rising threshold. The nFAULT pin is driven low during an undervoltage condition and is released after operation has resumed.

Table 2. Fault Handling

Fault	Error Report	H-Bridge	Internal Circuits	Recovery
VM undervoltage (UVLO)	nFAULT unlatched	Disabled	Shut down	System and fault clears on recovery
Overcurrent (OCP)	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery and motor is driven after time, t_{RETRY}
Thermal shutdown (TSD)	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery

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8.4 Device Functional Modes

The DRV8848 is active unless the nSLEEP pin is brought logic low. In sleep mode, the VINT regulator is disabled and the H-bridge FETs are disabled Hi-Z. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8848 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the output change state after wake-up.

When V_{VM} falls below the VM UVLO threshold (V_{UVLO}), the output driver, internal logic, and VINT regulator are reset.

Table 3. Functional Modes

Mode	Condition	H-Bridge	VINT
Operating	$4\ V < V_{VM} < 18\ V$ nSLEEP pin = 1	Operating	Operating
Sleep	$4\ V < V_{VM} < 18\ V$ nSLEEP pin = 0	Disabled	Disabled
Fault	Any fault condition met	Disabled	Depends on fault

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8848 is used in stepper or brushed DC motor control. The user can configure the DRV8848 with the following design procedure.

9.2 Typical Application

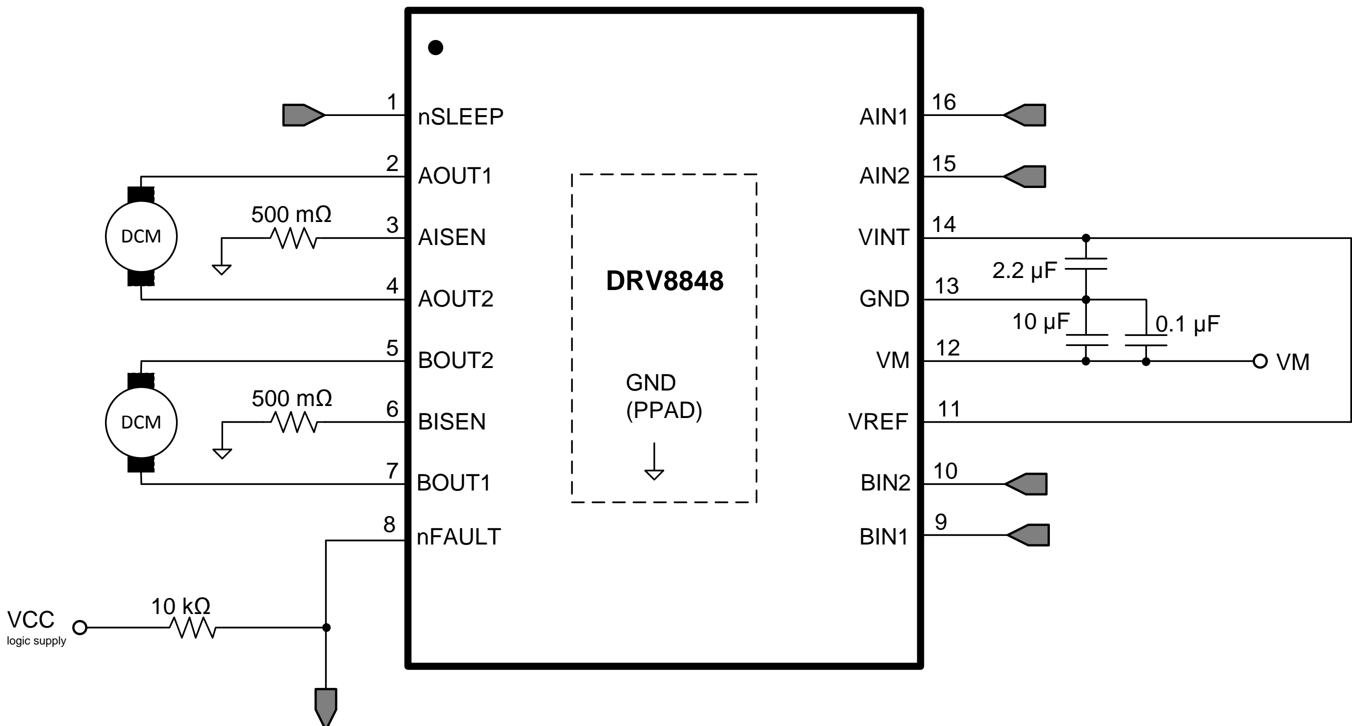

Figure 10. Typical Application Schematic

9.2.1 Design Requirements

Table 4 gives design input parameters for system design.

Table 4.

Design Parameter	Reference	Example Value
Nominal supply voltage	V_{VM}	12 V
Supply voltage range		4 to 18 V
Motor winding resistance	R_L	3 Ω/phase
Motor winding inductance	L_L	330 µH/phase
Target chopping current	I_{CHOP}	500 mA
Chopping current reference voltage	V_{VREF}	3.3 V

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9.2.2 Detailed Design Procedure

9.2.2.1 Current Regulation

The chopping current (I_{CHOP}) is the maximum current driven through either winding. This quantity depends on the sense resistor value (R_{XISEN}).

$$I_{CHOP} = \frac{V_{VREF}}{6.6 \times R_{XISEN}} \quad (2)$$

I_{CHOP} is set by a comparator which compares the voltage across R_{XISEN} to a reference voltage. Note that I_{CHOP} must follow Equation 3 to avoid saturating the motor.

$$I_{CHOP}\ (A) < \frac{V_{VM}\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega) + R_{XISEN}\ (\Omega)}$$

where

- V_{VM} is the motor supply voltage.
- R_L is the motor winding resistance. (3)

9.2.3 Application Curves

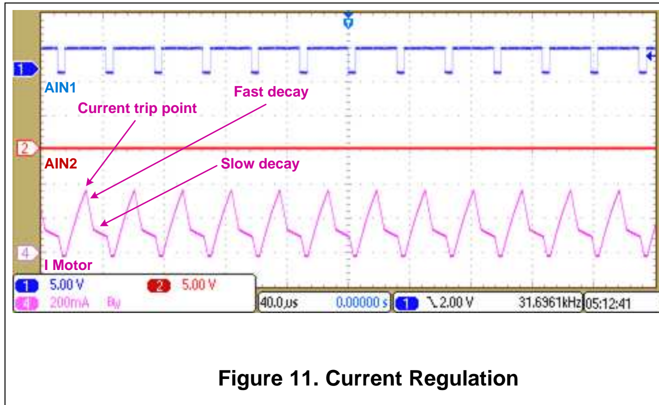

Figure 11. Current Regulation

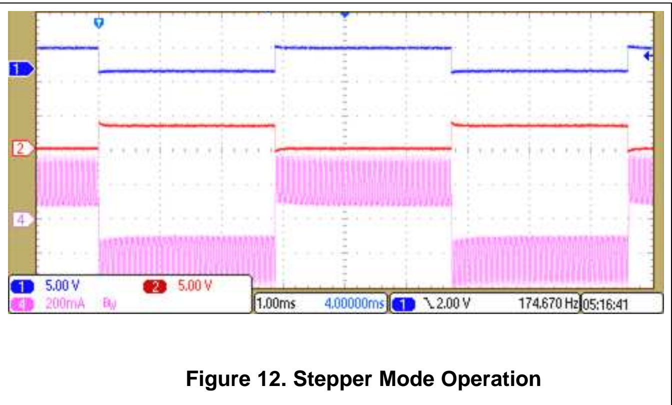

Figure 12. Stepper Mode Operation

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10 Power Supply Recommendations

The DRV8848 is designed to operate from an input voltage supply (V_{VM}) range between 4 and 18 V. Place a 0.1-μF ceramic capacitor rated for VM as close to the DRV8848 as possible. In addition, the user must include a bulk capacitor of at least 10 μF on VM.

10.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. It depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet provides a recommended minimum value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

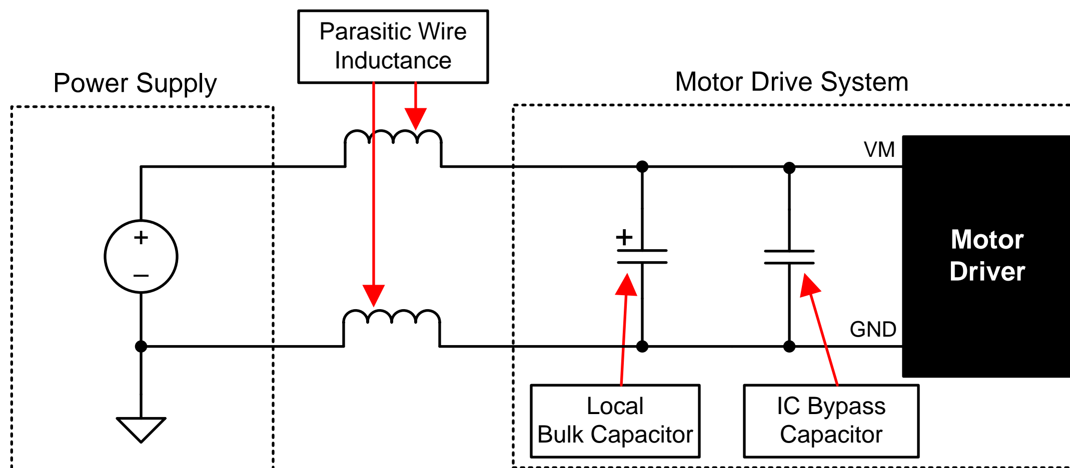

Figure 13. Setup of Motor Drive System With External Power Supply

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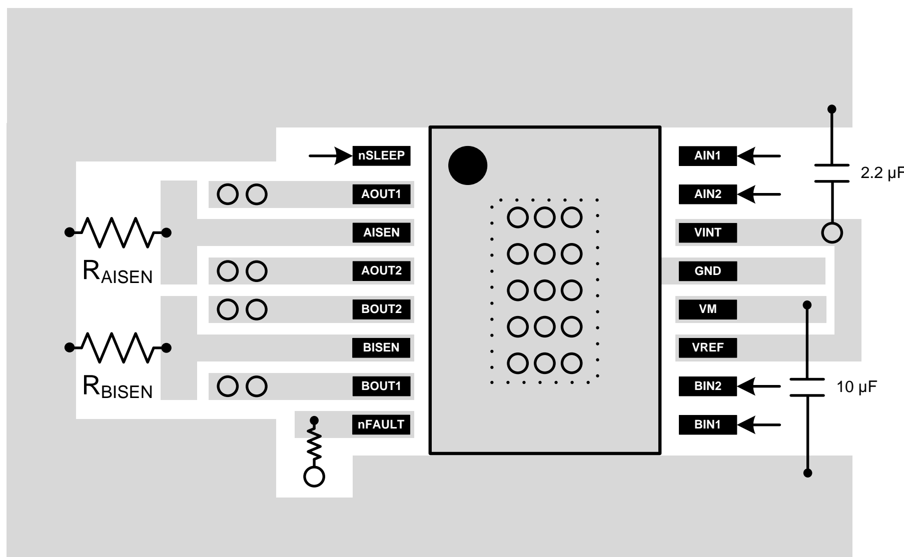
11 Layout

11.1 Layout Guidelines

Bypass the VM terminal to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10 µF rated for VM. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

Bypass VINT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

11.2 Layout Example



12 器件和文档支持

12.1 商标

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12.2 静电放电警告

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12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8848PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848	Samples
DRV8848PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848	Samples

(1) The marketing status values are defined as follows:
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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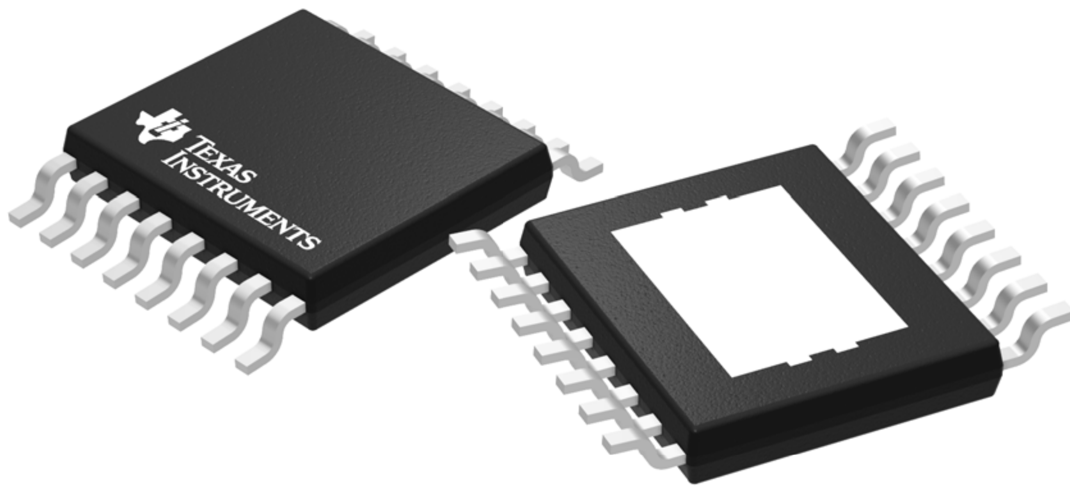
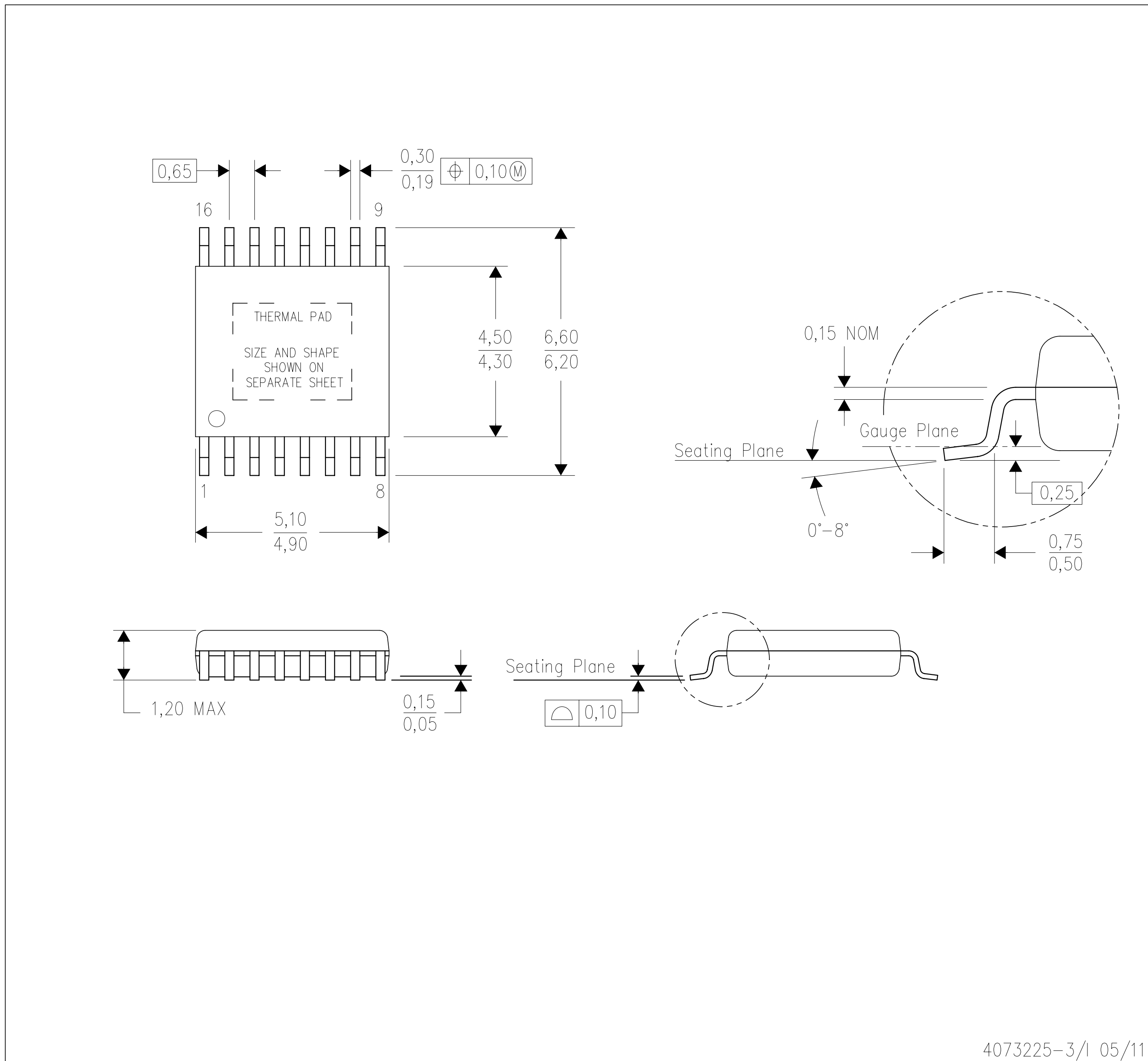
PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PWP (R-PDSO-G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

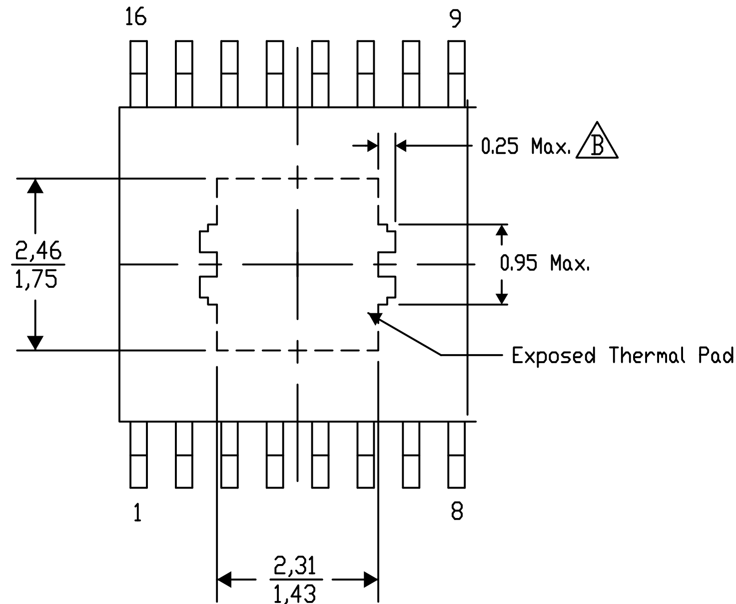
PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-6/AO 01/16

NOTE: A. All linear dimensions are in millimeters
B. Exposed tie strap features may not be present.

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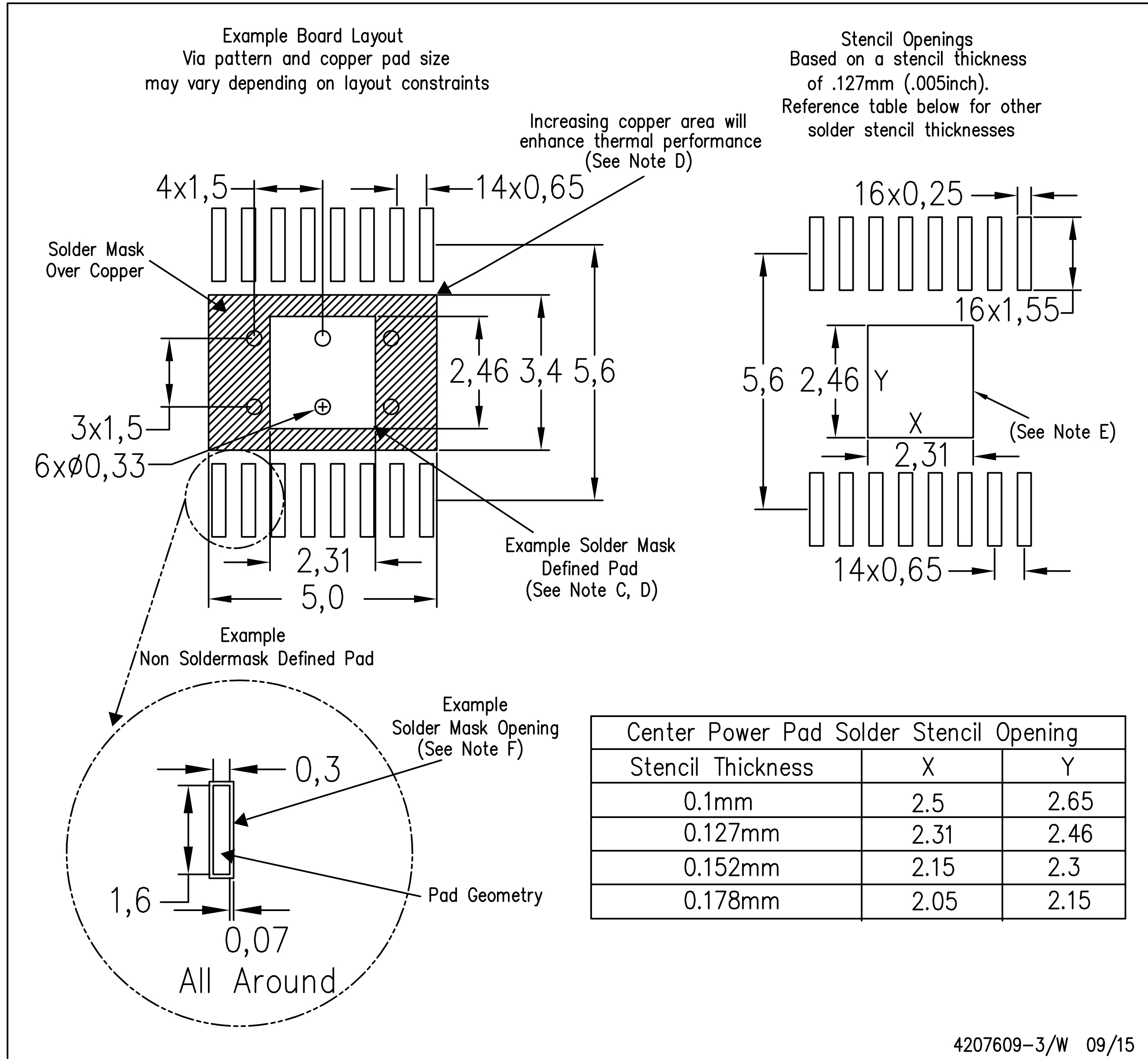
PWP (R-PDSO-G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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