DP83867E/IS/CS Robust, High Immunity, Small Form Factor 10/100/1000 Ethernet Physical Layer Transceiver

1 Features

- Extra low latency TX < 90 ns, RX < 290 ns
- Time Sensitive Network (TSN) compliant
- Low power consumption: 457 mW
- Exceeds 8000 V IEC 61000-4-2 ESD protection
- Meets EN55011 class B emission standards
- 16 programmable RGMII delay modes on RX/TX
- Integrated MDI termination resistors
- Programmable MAC interface termination impedance
- WoL (Wake-on-LAN) packet detection
- 25-MHz or 125-MHz synchronized clock output
- IEEE 1588 time stamp support
- RJ45 mirror mode
- Fully compatible to IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T Specification
- Cable diagnostics
- RGMII and SGMII MAC interface options
- Configurable I/O voltage (3.3 V, 2.5 V, 1.8 V)
- Fast link drop mode
- JTAG support

2 Applications

- Motor drives
- Industrial factory automation
- Field Bus Support
- Industrial embedded computing
- Wired and wireless communications infrastructure
- Test and measurement
- Consumer electronics

3 Description

The DP83867 device is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols. Optimized for ESD protection, the DP83867 exceeds 8-kV IEC 61000-4-2 (direct contact).

The DP83867 is designed for easy implementation of 10/100/1000 Mbps Ethernet LANs. It interfaces directly to twisted pair media through an external transformer. This device interfaces directly to the MAC layer through Reduced GMII (RGMII) or embedded clock Serial GMII (SGMII).

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

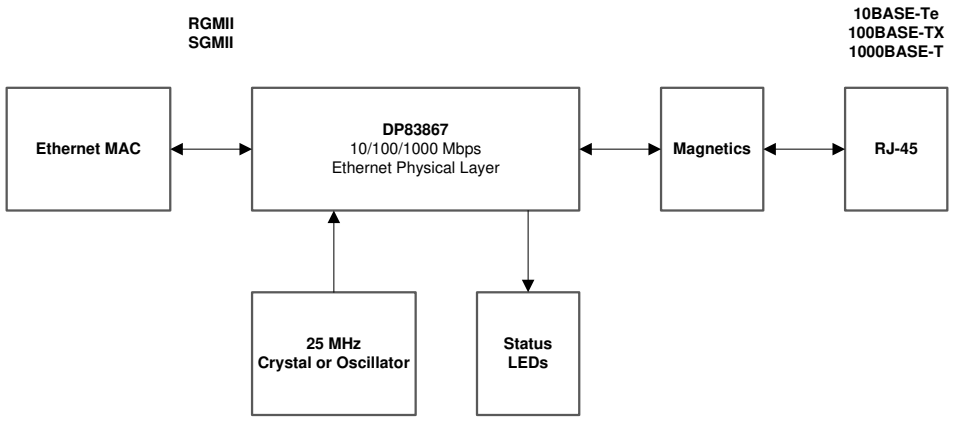
Designed for low power, the DP83867 consumes only 457 mW under full operating power. Wake-on-LAN can be used to lower system power consumption.

Device Information(1)

PART NUMBER	TEMPERATURE	PACKAGE	BODY SIZE (NOM)
DP83867CSRGZ	0°C to +70°C	VQFN (48)	7 mm × 7 mm
DP83867ISRGZ	–40°C to +85°C	VQFN (48)	7 mm × 7 mm
DP83867ERGZ	–40°C to +105°C	VQFN (48)	7 mm × 7 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

System Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

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- Added "Time Sensitive Network (TSN) Compliant" to Features ... 1
- Changed "Fast Link up / Link Drop Modes" to "Fast Link Drop Mode" in Features ... 1
- Added "Field Bus Support" to Applications ... 1
- Deleted "NOTE: Internal pullup and pulldown resistors on the IO pins are disabled when the device enters functional mode after power up." from Pin Functions ... 6
- Added XI pin voltage ratings to Absolute Maximum Ratings ... 9
- Added XI Input Voltage section to Electrical Characteristics ... 10
- Added SGMII Latency nominal values to SGMII Timing (4) ... 12
- Changed links to RGMII timing diagrams in RGMII Timing (5) ... 12
- Changed T_{holdR} parameter description in RGMII Timing (5) ... 13
- Added table note explaining how Duty Cycle % must be interpreted in RGMII Timing (5) ... 13
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- Changed suggestion to program '10M_SGMII_RATE_ADAPT' bit in Serial GMII (SGMII) ... 24
- Changed statement about PHY address in Serial Management Interface ... 27
- Deleted mentions of pin strapping to configure Auto-MDIX in Auto-MDIX Resolution ... 32
- Added Figure 19 ... 32
- Deleted "The BIST allows full control of the packet lengths and of the IPG." from BIST Configuration ... 33
- Deleted mention of ALCD from Cable Diagnostics ... 34
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- Changed all mentions of "Fast Link Down" to "Fast Link Drop" in Fast Link Drop (FLD) ... 35
- Added statement on disabling and re-enabling FLD in Fast Link Drop (FLD) ... 35
- Added sentence about the polarity of MDI signals in Mirror Mode ... 36

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Revision History (continued)

- Changed note after Table 6 to be a table note referenced within the table. ... 38
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- Deleted mention of MMD7 in PCS Restart ... 43
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- Deleted Advanced Link Cable Diagnostics Control Register (ALCD_CTRL) ... 44
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- Changed 'SGMII_EN' default in PHY Control Register (PHYCR) ... 57
- Changed 'MDI_CROSSOVER' default in PHY Control Register (PHYCR) ... 57
- Added PAP package default for 'SPEED_OPT_EN' in Configuration Register 2 (CFG2) ... 64
- Added Robust Auto MDIX Timer Configuration Register (AMDIX_TMR_CFG) ... 73
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- Changed pin 6 name in the pinout diagram from: VDDA1P0 to: VDD1P0 ... 5
- Changed $\overline{\text{INT}}$ / $\overline{\text{PWDN}}$ Interrupt description ... 7
- Changed RESERVED bit number from: 15:8 to: 15:9 ... 75
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- Added storage temperature to *Absolute Maximum Ratings* ... 9
- Updated parameter symbol from VIH to V_{IH} ... 10
- Added MDC toggling clarification to *Reset Timing*(2) ... 12
- Added *DP83867E Start of Frame Detection Timing* ... 13
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- Added section *SFD Latency Variation and Determinism* ... 22
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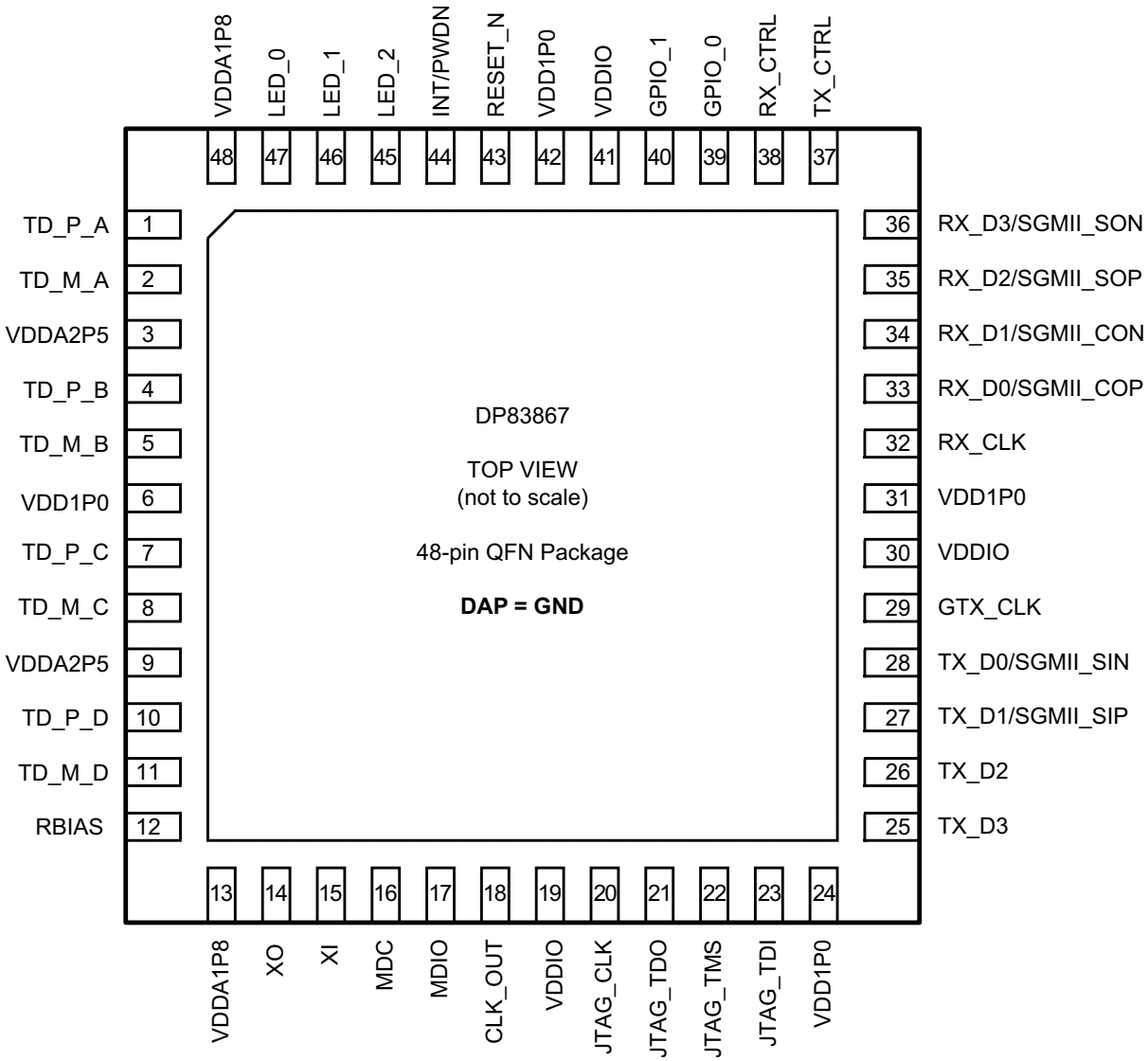
5 Device Comparison

Table 1. Device Features Comparison

DEVICE	MAC	TEMPERATURE RANGE		TEMPERATURE GRADE
DP83867CSRGZ	SGMII/RGMII	0°C	70°C	Commercial
DP83867ISRGZ	SGMII/RGMII	–40°C	85°C	Industrial
DP83867ERGZ	SGMII/RGMII	–40°C	105°C	Extended

6 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
MAC INTERFACES (SGMII, RGMII)			
TX_D3	25	I, PD	TRANSMIT DATA Bit 3: This signal carries data from the MAC to the PHY in RGMII mode. It is synchronous to the transmit clock GTX_CLK.
TX_D2	26	I, PD	TRANSMIT DATA Bit 2: This signal carries data from the MAC to the PHY in RGMII mode. It is synchronous to the transmit clock GTX_CLK.
SGMII_SIP	27	I, PD	Differential SGMII Data Input: This signal carries data from the MAC to the PHY in SGMII mode. It is synchronous to the differential SGMII clock input. This pin should be AC-coupled to the MAC through a 0.1-µF capacitor when operating in SGMII mode.
TX_D1	27	I, PD	TRANSMIT DATA Bit 1: This signal carries data from the MAC to the PHY in RGMII mode. It is synchronous to the transmit clock GTX_CLK.
SGMII_SIN	28	I, PD	Differential SGMII Data Input: This signal carries data from the MAC to the PHY in SGMII mode. It is synchronous to the differential SGMII clock input. This pin should be AC-coupled to the MAC through a 0.1-µF capacitor when operating in SGMII mode.
TX_D0	28	I, PD	TRANSMIT DATA Bit 0: This signal carries data from the MAC to the PHY in RGMII mode. It is synchronous to the transmit clock GTX_CLK.
GTX_CLK	29	I, PD	RGMII TRANSMIT CLOCK: This continuous clock signal is sourced from the MAC layer to the PHY. Nominal frequency is 125 MHz.
RX_CLK	32	O	RGMII RECEIVE CLOCK: Provides the recovered receive clocks for different modes of operation: 2.5 MHz in 10-Mbps mode. 25 MHz in 100-Mbps mode. 125 MHz in 1000-Mbps mode.
SGMII_COP	33	S, O	Differential SGMII Clock Output: This signal is a continuous 625-MHz clock signal driven by the PHY in SGMII mode. This pin should be AC-coupled to the MAC through a 0.1-µF capacitor when operating in SGMII mode.
RX_D0	33	S, O, PD	RECEIVE DATA Bit 0: This signal carries data from the PHY to the MAC in RGMII mode. It is synchronous to the receive clock RX_CLK.
SGMII_CON	34	S, O, PD	Differential SGMII Clock Output: This signal is a continuous 625-MHz clock signal driven by the MAC in SGMII mode. This pin should be AC-coupled to the MAC through a 0.1-µF capacitor when operating in SGMII mode.
RX_D1	34	O, PD	RECEIVE DATA Bit 1: This signal carries data from the PHY to the MAC in RGMII mode. It is synchronous to the receive clock RX_CLK.
SGMII_SOP	35	S, O, PD	Differential SGMII Data Output: This signal carries data from the PHY to the MAC in SGMII mode. It is synchronous to the differential SGMII clock output. This pin should be AC-coupled to the MAC through a 0.1-µF capacitor when operating in SGMII mode.
RX_D2	35	S, O, PD	RECEIVE DATA Bit 2: This signal carries data from the PHY to the MAC in RGMII mode. It is synchronous to the receive clock RX_CLK.
SGMII_SON	36	S, O, PD	Differential SGMII Data Output: This signal carries data from the PHY to the MAC in SGMII mode. It is synchronous to the differential SGMII clock output. This pin should be AC-coupled to the MAC through a 0.1-µF capacitor when operating in SGMII mode.
RX_D3	36	O, PD	RECEIVE DATA Bit 3: This signal carries data from the PHY to the MAC in RGMII mode. It is synchronous to the receive clock RX_CLK.

(1) The definitions below define the functionality of each pin.
(a) Type: I Input
(b) Type: O Output
(c) Type: I/O Input/Output
(d) Type: PD, PU Internal Pulldown/Pullup
(e) Type: S Configuration Pin
(f) Type: P Power or GND
(g) Type: A Analog pins

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
TX_CTRL	37	I, PD	TRANSMIT CONTROL: In RGMII mode, it combines the transmit enable and the transmit error signals of GMII mode using both clock edges.
RX_CTRL	38	S, O, PD	RECEIVE CONTROL: In RGMII mode, the receive data available and receive error are combined (RXDV_ER) using both rising and falling edges of the receive clock (RX_CLK).
GENERAL-PURPOSE I/O			
GPIO_0	39	S, O, PD	General-Purpose I/O: This signal provides a multi-function configurable I/O. Refer to the GPIO_MUX_CTRL register for details.
GPIO_1	40	S, O, PD	General-Purpose I/O: This signal provides a multi-function configurable I/O. Refer to the GPIO_MUX_CTRL register for details.
MANAGEMENT INTERFACE			
MDC	16	I, PD	MANAGEMENT DATA CLOCK: Synchronous clock to the MDIO serial management input and output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25 MHz and no minimum.
MDIO	17	I/O	MANAGEMENT DATA I/O: Bidirectional management instruction and data signal that may be sourced by the management station or the PHY. This pin requires pullup resistor. The IEEE specified resistor value is 1.5 kΩ, but a 2.2 kΩ is acceptable.
$\overline{\text{INT}}$ / $\overline{\text{PWDN}}$	44	I/O, PU	INTERRUPT / POWER DOWN: The default function of this pin is POWER DOWN. POWER DOWN: This is an Active Low Input. Asserting this signal low enables the power-down mode of operation. In this mode, the device powers down and consume minimum power. Register access is available through the Management Interface to configure and power up the device. INTERRUPT: When operating this pin as an interrupt, it is an open-drain architecture. TI recommends using an external 2.2-kΩ resistor connected to the VDDIO supply.
RESET			
RESET_N	43	I, PU	RESET: The active low RESET initializes or reinitializes the DP83867. All internal registers re-initialize to their default state upon assertion of RESET. The RESET input must be held low for a minimum of 1 µs.
CLOCK INTERFACE			
XI	15	I	CRYSTAL/OSCILLATOR INPUT: 25-MHz oscillator or crystal input (50 ppm)
XO	14	O	CRYSTAL OUTPUT: Second terminal for 25-MHz crystal. Must be left floating if a clock oscillator is used.
CLK_OUT	18	O	CLOCK OUTPUT: Output clock
JTAG INTERFACE			
JTAG_CLK	20	I, PU	JTAG TEST CLOCK: IEEE 1149.1 Test Clock input, primary clock source for all test logic input and output controlled by the testing entity.
JTAG_TDO	21	O	JTAG TEST DATA OUTPUT: IEEE 1149.1 Test Data Output pin, the most recent test results are scanned out of the device through TDO.
JTAG_TMS	22	I, PU	JTAG TEST MODE SELECT: IEEE 1149.1 Test Mode Select pin, the TMS pin sequences the Tap Controller (16-state FSM) to select the desired test instruction. TI recommends applying 3 clock cycles with JTAG_TMS high to reset the JTAG.
JTAG_TDI	23	I, PU	JTAG TEST DATA INPUT: IEEE 1149.1 Test Data Input pin, test data is scanned into the device through TDI.
LED INTERFACE			
LED_2	45	S, I/O, PD	LED_2: By default, this pin indicates receive or transmit activity. Additional functionality is configurable through LEDCR1[11:8] register bits.
LED_1	46	S, I/O, PD	LED_1: By default, this pin indicates that 1000BASE-T link is established. Additional functionality is configurable through LEDCR1[7:4] register bits.
LED_0	47	S, I/O, PD	LED_0: By default, this pin indicates that link is established. Additional functionality is configurable through LEDCR1[3:0] register bits.

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
MEDIA DEPENDENT INTERFACE			
TD_P_A	1	A	Differential Transmit and Receive Signals
TD_M_A	2	A	Differential Transmit and Receive Signals
TD_P_B	4	A	Differential Transmit and Receive Signals
TD_M_B	5	A	Differential Transmit and Receive Signals
TD_P_C	7	A	Differential Transmit and Receive Signals
TD_M_C	8	A	Differential Transmit and Receive Signals
TD_P_D	10	A	Differential Transmit and Receive Signals
TD_M_D	11	A	Differential Transmit and Receive Signals
OTHER PINS			
RBIAS	12	A	Bias Resistor Connection. A 11-kΩ ±1% resistor should be connected from RBIAS to GND.
POWER AND GROUND PINS			
VDDA2P5	3, 9	P	2.5-V Analog Supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
VDD1P0	6, 24, 31, 42	P	1-V Analog Supply (+15.5%, –5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
VDDA1P8	13, 48	P	1.8-V Analog Supply (±5%). No external supply is required for this pin. When unused, no connections should be made to this pin. For additional power savings, an external 1.8-V supply can be connected to these pins. When using an external supply, each pin requires a 1-µF and 0.1-µF capacitor to GND.
VDDIO	19, 30, 41	P	I/O Power: 1.8 V (±5%), 2.5 V (±5%) or 3.3 V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND
GND	Die Attach Pad	P	Ground

6.1 Unused Pins

DP83867 has internal pullups or pulldowns on most pins. The data sheet details which pins have internal pullups or pulldowns and which pins require external pull resistors.

Even though a device may have internal pullup or pulldown resistors, a good practice is to terminate unused inputs rather than allowing them to float. Floating inputs could result in unstable conditions. Except for VDDA1P8 pins, if they are not used then they should be left floating. It is considered a safer practice to pull an unused input pin high or low with a pullup or pulldown resistor. It is also possible to group together adjacent unused input pins, and as a group pull them up or down using a single resistor.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage	VDDA2P5		–0.3	3	V
	VDDA1P8		–0.3	2.1	
	(VDD1P0)		–0.3	1.3	
	VDDIO	3.3-V option	–0.3	3.8	
		2.5-V option	–0.3	3	
		1.8-V option	–0.3	2.1	
Pins	MDI		–0.3	6.5	V
	MAC interface, MDIO, MDC, GPIO		–0.3	VDDIO + 0.3	
	INT/PWDN, RESET		–0.3	VDDIO + 0.3	
	JTAG		–0.3	VDDIO + 0.3	
	XI (Oscillator Clock Input)		–0.3	2.1	V
Storage temperature, T_{stg}			–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
DP83867ERGZ and DP83867ISRGZ in the RGZ Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except 1, 2, 4, 5, 7, 8, 10, and 11	±2500	V
			Pins 1, 2, 4, 5, 7, 8, 10, and 11 (2)	±8000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)		±1500	
DP83867CSRGZ in the RGZ Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except 1, 2, 4, 5, 7, 8, 10, and 11	±2500	V
			Pins 1, 2, 4, 5, 7, 8, 10, and 11 (2)	±6000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±8 V and/or ± 2 V may actually have higher performance.
(2) MDI Pins tested as per IEC 61000-4-2 standards.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
Supply voltage	VDDA2P5		2.375	2.5	2.625	V
	VDDA1P8		1.71	1.8	1.89	
	VDD1P0		0.95	1	1.155	
	VDDIO	3.3-V option	3.15	3.3	3.45	
		2.5-V option	2.375	2.5	2.625	
		1.8-V option	1.71	1.8	1.89	

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Operating junction temperature	Commercial (DP83867CSRGZ)	0		90	°C
	Industrial (DP83867ISRGZ)	–40		105	
	Extended (DP83867ERGZ)	–40		125	
Operating free air temperature	Commercial (DP83867CSRGZ)	0	25	70	°C
	Industrial (DP83867ISRGZ)	–40	25	85	
	Extended (DP83867ERGZ)	–40	25	105	

7.4 Thermal Information

THERMAL METRIC(1)		DP83867xS, DP83867E RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.3-V V_{DDIO}						
V_{OH}	High level output voltage	I_{OH} = –4 mA	2			V
V_{OL}	Low level output voltage	I_{OL} = 4 mA			0.6	V
V_{IH}	High level input voltage		1.7			V
V_{IL}	Low level input voltage				0.7	V
2.5-V V_{VDDIO}						
V_{OH}	High level output voltage	I_{OH} = –4 mA	V_{DDIO} × 0.8			V
V_{OL}	Low level output voltage	I_{OL} = 4 mA			0.6	V
V_{IH}	High level input voltage		1.7			V
V_{IL}	Low level input voltage				0.7	V
1.8-V V_{DDIO}						
V_{OH}	High level output voltage	I_{OH} = –1 mA	V_{DDIO} – 0.2			V
V_{OL}	Low level output voltage	I_{OL} = 1 mA			0.2	V
V_{IH}	High level input voltage		0.7 × V_{DDIO}			V
V_{IL}	Low level input voltage				0.2 × VDDIO	V
XI INPUT VOLTAGE						
V_{OSC}	Input voltage for 25 MHz Oscillator		1.5		1.9	Vpp
V_{IH}	High level input voltage		1.4			V
V_{IL}	Low level input voltage				0.45	V
DC CHARACTERISTICS						

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Electrical Characteristics (continued)

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input high current	VIN = VDD, T_A = –40°C to +85°C				
		VIN = VDD, T_A = 85°C to +105°C				
I_{IL}	Input low current	VIN = GND, T_A = –40°C to +85°C				
		VIN = GND, T_A = 85°C to +105°C				
I_{OZ}	TRI-STATE output current	VOUT = VDD, VOUT = GND, T_A = –40°C to +85°C				
		VOUT = VDD, VOUT = GND, T_A = 85°C to +105°C				
C_{IN}	Input capacitance	See (1)			5	pF
PMD OUTPUTS						
V_{OD-10}	MDI	ERGZ/ISRGZ	1.54	1.75	1.96	V Peak Differential
		CSRGZ		1.75		
V_{OD-100}	MDI	ERGZ/ISRGZ	0.95	1	1.05	V Peak Differential
		CSRGZ		1		
$V_{OD-1000}$	MDI	ERGZ/ISRGZ	0.67	0.745	0.82	V Peak Differential
		CSRGZ		0.745		
POWER CONSUMPTION						
P1000	RGMII power consumption (2)(3)(4)	2 supplies		495		mW
		Optional 3rd supply		457		
IDD25	Supply current	2 supplies		137		mA
IDD10				108		mA
IDDIO (1.8 V)				24		mA
IDD25	Supply current	Optional 3rd supply		86		mA
IDD10				108		mA
IDD18				50		mA
IDDIO (1.8 V)				24		mA

(1) Ensured by production test, characterization, or design.
(2) Power consumption represents total operational power for 1000BASE-T.
(3) See *Power Supply Recommendations* for details on 2-supply and 3-supply configuration.
(4) For detailed information about DP83867 power consumption for specific supplies under a wide set of conditions, see the *DP83867E/IS/CS/IR/CR RGZ Power Consumption Data* application report (SNLA241).

7.6 Power-Up Timing (1)

See Figure 1.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T1	Post power-up stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization.		200		ms
T2	Hardware configuration latch-in time from power up	Hardware Configuration Pins are described in *Strap Configuration*.		200		ms
T3	Hardware configuration pins transition to output drivers			64		ns

(1) Ensured by production test, characterization, or design.

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7.7 Reset Timing(1)

See Figure 2.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T1	Post RESET stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization. MDC may toggle during this period when MDIO remains high.		195		µs
T2	Hardware configuration latch-in time from the deassertion of RESET (either soft or hard)	Hardware Configuration Pins are described in *Strap Configuration*.		120		ns
T3	Hardware configuration pins transition to output drivers			64		ns
T4	RESET pulse width	X1 Clock must be stable for a minimum of 1 µs during RESET pulse low time	1			µs

(1) Ensured by production test, characterization, or design.

7.8 MII Serial Management Timing(1)

See Figure 3.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T1	MDC to MDIO (output) delay time		0		10	ns
T2	MDIO (input) to MDC setup time		10			ns
T3	MDIO (input) to MDC hold time		10			ns
T4	MDC frequency			2.5	25	MHz

(1) Ensured by production test, characterization, or design.

7.9 SGMII Timing(1)

See Figure 4.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T1	SGMII Clock Output Duty Cycle		48%		52%	
T2	Setup time	See (2)	100			ps
T3	Clock to Data relationship from either edges of the clock to valid data	See (3)	250		550	ps
T_R	VOD fall time	20% - 80%	100		200	ps
T_F	VOD rise time	20% - 80%	100		200	ps
T_{hold}	Hold time	See (2)	100			ps
T_{TXLAT}	SGMII to MDI Latency	See (4)		201		ns
T_{RXLAT}	MDI to SGMII Latency	See (4)		289		ns

(1) Ensured by production test, characterization, or design.
(2) Setup and hold time are measured at 50% of the transition.
(3) T3 is measured at 0 V differential.
(4) Operating in 1000Base-T

7.10 RGMII Timing(1)

See Figure 5 and Figure 6.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T_{skewT}	Data to Clock output Skew (at Transmitter)	See (2)	–500	0	500	ps
T_{skewR}	Data to Clock input Skew (at Receiver)	See (2)	1	1.8	2.6	ns

(1) Ensured by production test, characterization, or design.
(2) When operating without RGMII internal delay, the PCB design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

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RGMII Timing[1] (continued)

See Figure 5 and Figure 6.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T_{setupT}	Data to Clock output Setup (at Transmitter – internal delay)	See [3]	1.2	2		ns
T_{holdT}	Clock to Data output Hold (at Transmitter – internal delay)	See [3]	1.2	2		ns
T_{setupR}	Data to Clock input Setup (at Reciever – internal delay)	See [3]	1	2		ns
T_{holdR}	Clock to Data input Hold (at Receiver – internal delay)	See [3]	1	2		ns
T_{cyc}	Clock Cycle Duration	See [4]	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit	See [5][6]	45	50	55%	
Duty_T	Duty Cycle for 10/100T	See [5][6]	40	50	60%	
T_R	Rise Time (20% to 80%)				0.75	ns
T_F	Fall Time (20% to 80%)				0.75	ns
T_{TXLAT}	RGMII to MDI Latency	See [7]		88		ns
T_{RXLAT}	MDI to RGMII Latency	See [7]		288		ns

(3) Device may operate with or without internal delay.
(4) For 10-Mbps and 100-Mbps, Tcyc will scale to 400 ns ± 40 ns and 40 ns ± 4 ns.
(5) Duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more that three Tcyc of the lowest speed transitioned between.
(6) Duty cycle values are defined in percentages of the nominal clock speed. For example, the minimum Gigabit RGMII clock pulse duration is 45 % of 8 ns.
(7) Operating in 1000Base-T .

7.11 DP83867E Start of Frame Detection Timing

See Figure 7.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T1	Transmit SFD variation[1][2]	1000-Mb Master	0		0	ns
		1000-Mb Slave	0		0	ns
		100-Mb	0		8	ns
T2	Receive SFD variation[1][2]	1000-Mb Master	–4		4	ns
		1000-Mb Slave	0		0	ns
		100-Mb	0		0	ns

(1) A larger variation may be seen on SFD pulses than the variation specified here. To achieve the determinism specification listed, see the *SFD Latency Variation and Determinism* section for a method to compensate for variation in the SFD pulses.
(2) Variation of SFD pulses occurs from link-up to link-up. Packet to packet variation is fixed using the estimation method in *SFD Latency Variation and Determinism*.

7.12 DP83867IS/CS Start of Frame Detection Timing

See Figure 8.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T1	Transmit SFD variation[1][2]	1000-Mb Master	0		0	ns
		1000-Mb Slave	0		0	ns
		100-Mb	0		16	ns
T2	Receive SFD variation[1][2]	1000-Mb Master	–8		8	ns
		1000-Mb Slave	–8		8	ns
		100-Mb	0		0	ns

(1) A larger variation may be seen on SFD pulses than the variation specified here. To achieve the determinism specification listed, see the *SFD Latency Variation and Determinism* section for a method to compensate for variation in the SFD pulses.
(2) Variation of SFD pulses occurs from link-up to link-up. Packet to packet variation is fixed using the estimation method in *SFD Latency Variation and Determinism*.

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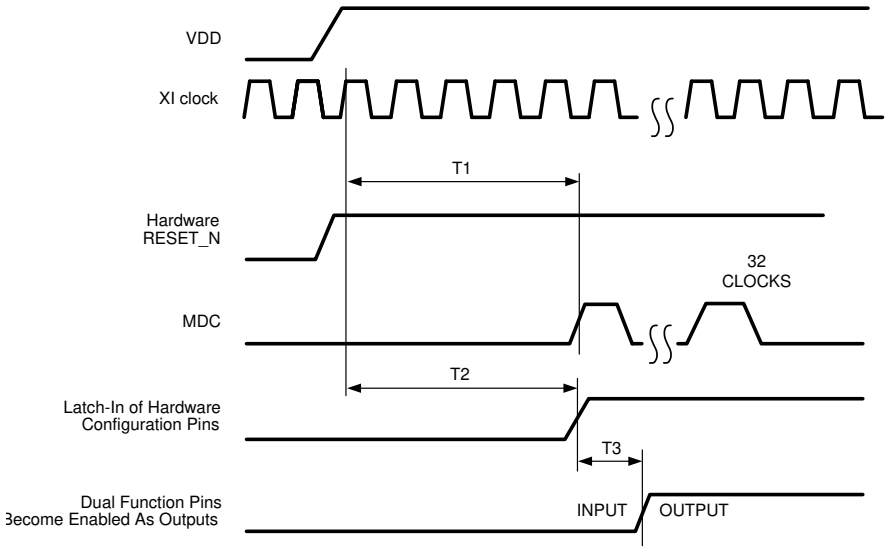

Figure 1. Power-Up Timing

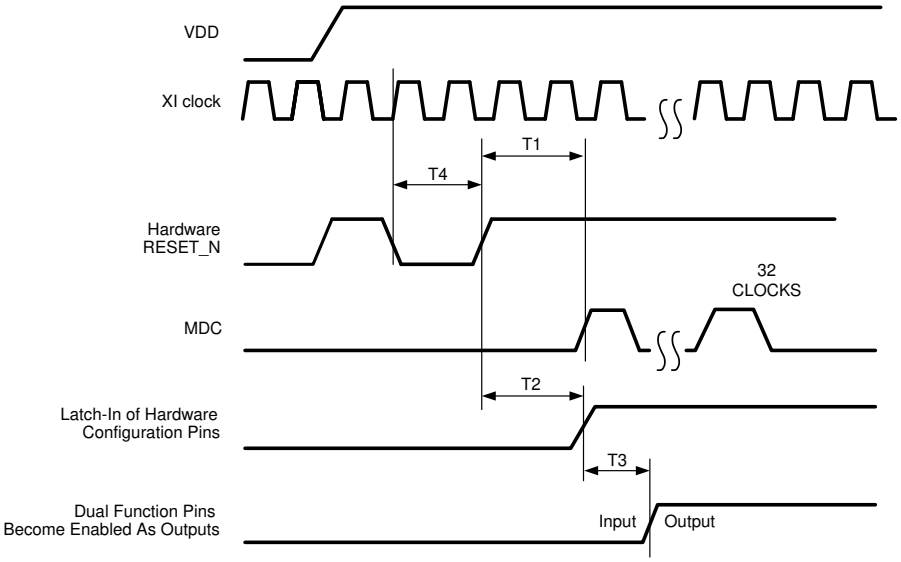

Figure 2. Reset Timing

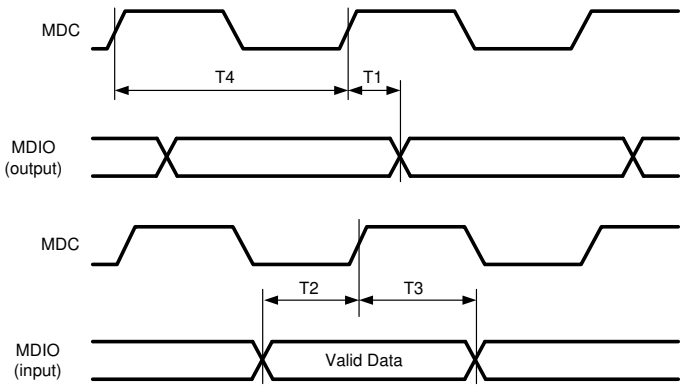

Figure 3. MII Serial Management Timing

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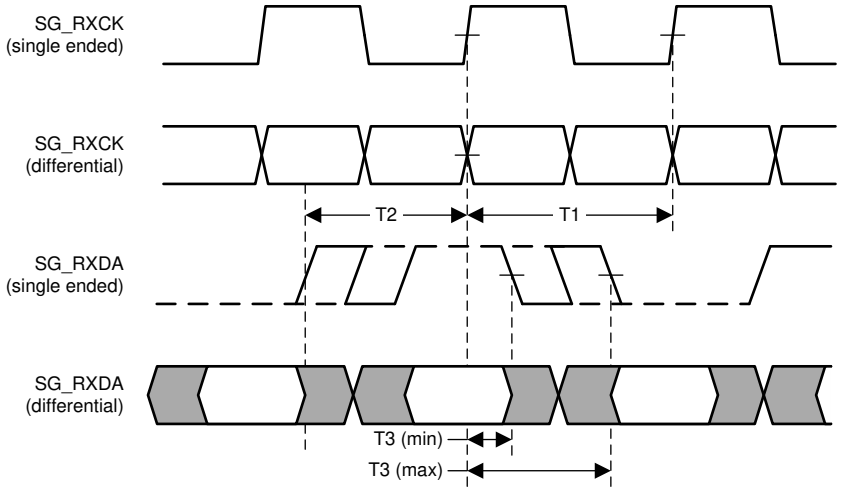

Figure 4. SGMII Timing

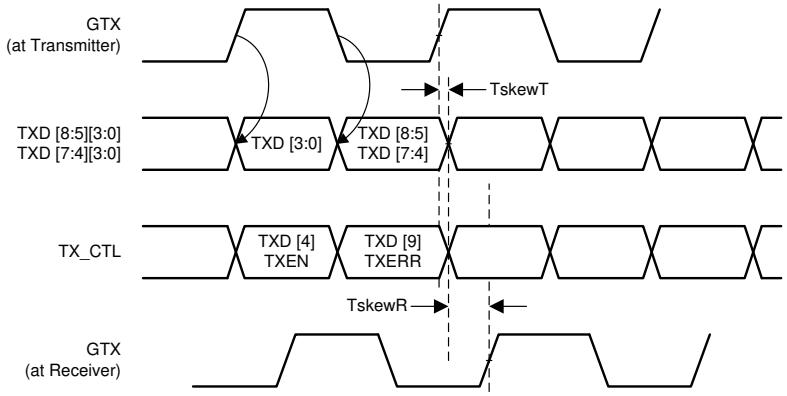

Figure 5. RGMII Transmit Multiplexing and Timing Diagram

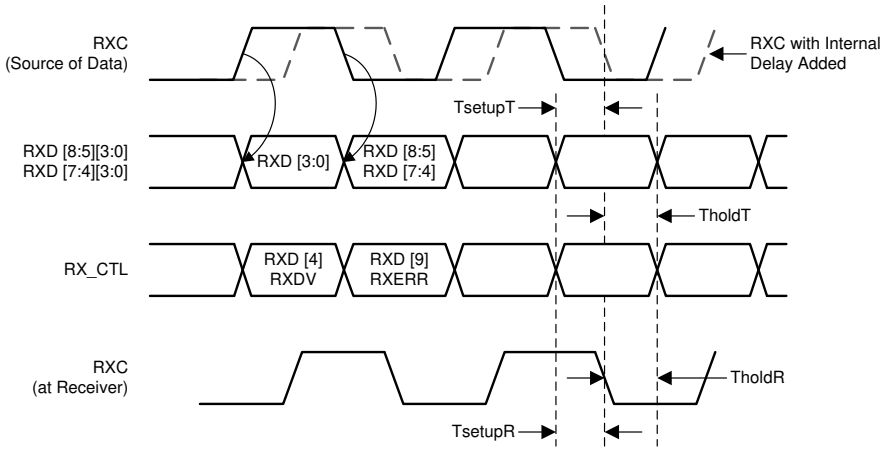

Figure 6. RGMII Receive Multiplexing and Timing Diagram

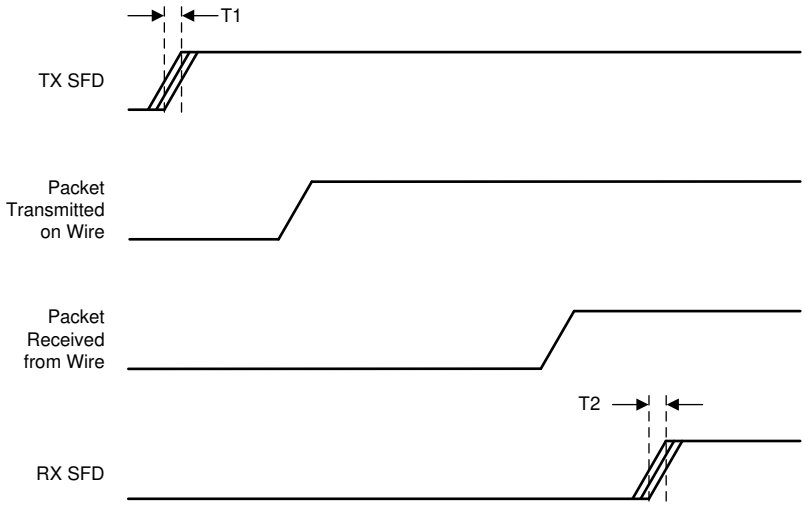

Figure 7. DP83867E Start of Frame Delimiter Timing

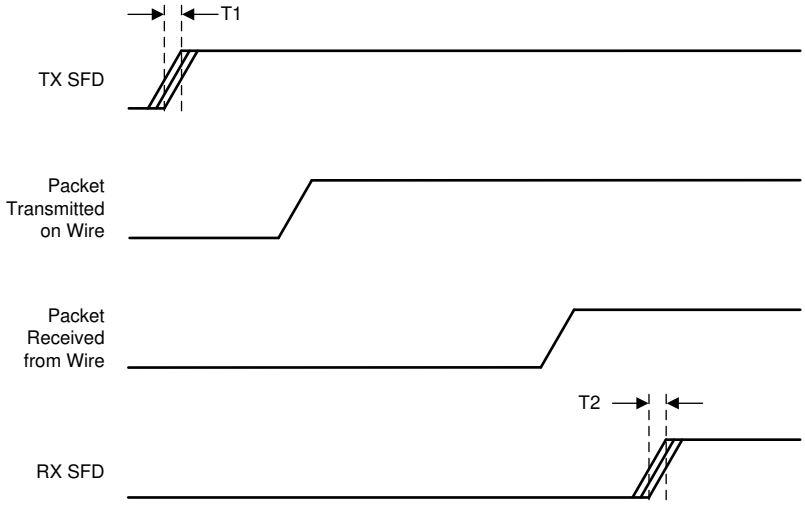

Figure 8. DP83867IS/CS Start of Frame Delimiter Timing

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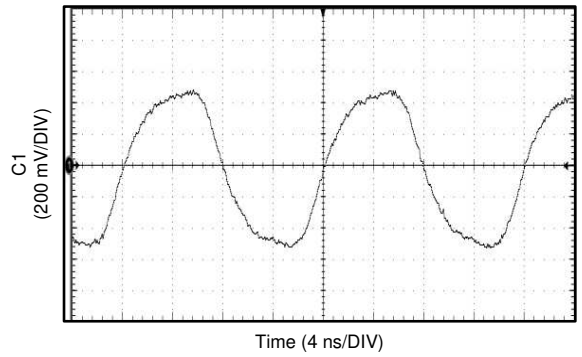
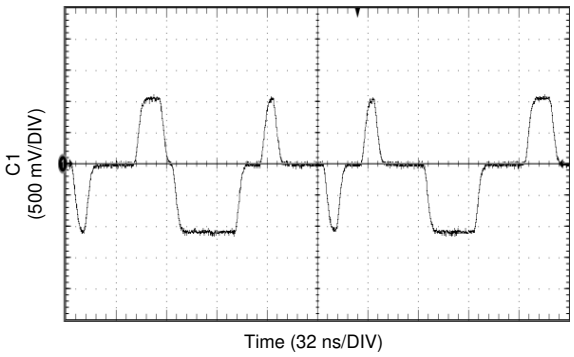
7.13 Typical Characteristics



1000Base-T Signaling
(Test Mode TM2 Output)

Figure 9. 1000Base-T Signaling



100Base-TX Signaling
(Scrambled Idles)

Figure 10. 100Base-TX Signaling

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8 Detailed Description

8.1 Overview

The DP83867 is a fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols.

The DP83867 is designed for easy implementation of 10-,100-, and 1000-Mbps Ethernet LANs. It interfaces directly to twisted pair media through an external transformer. This device interfaces directly to the MAC layer through the Reduced GMII (RGMII) or embedded clock Serial GMII (SGMII).

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low jitter, low latency and provides IEEE 1588 Start of Frame Detection for time sensitive protocols.

The DP83867 offers innovative diagnostic features including dynamic link quality monitoring for fault prediction during normal operation. It can support up to 130-m cable length.

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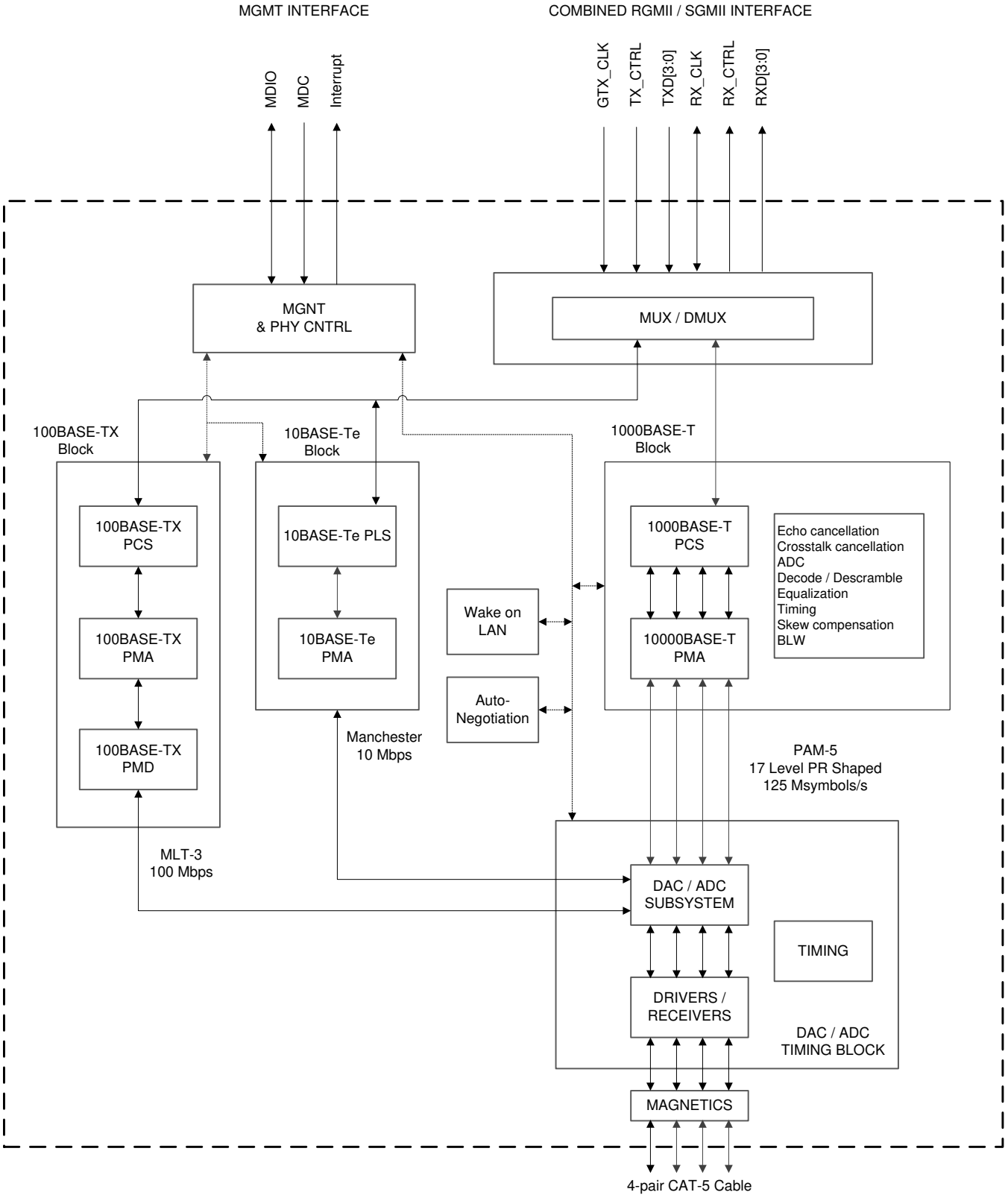
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 WoL (Wake-on-LAN) Packet Detection

Wake-on-LAN provides a mechanism for bringing the DP83867 out of a low-power state using a special Ethernet packet called a Magic Packet. The DP83867 can be configured to generate an interrupt to wake up the MAC when a qualifying packet is received. An option is also available to generate a signal on a GPIO when a qualifying signal is received.

NOTE

Please ensure that BMCR (register address 0x0000) bit[10] is disabled, when using the WoL feature. This bit enables the MII ISOLATE function used to disable the MAC interface of the PHY, also disabling the WoL interrupt on this PHY. If the WoL feature is needed while MII ISOLATE is enabled please use TI's DP83869HM PHY instead.

The Wake-on-LAN feature includes the following functionality:

- Identification of magic packets in all supported speeds (1000BASE-T, 100BASE-TX, 10BASE-Te)
- Wakeup interrupt generation upon receiving a valid magic packet
- CRC checking of magic packets to prevent interrupt generation for invalid packets

In addition to the basic magic packet support, the DP83867 also supports:

- Magic packets that include secure-on password
- Pattern match – one configurable 64 byte pattern of that can wake up the MAC similar to magic packet
- Independent configuration for Wake on Broadcast and Unicast packet types.

8.3.1.1 Magic Packet Structure

When configured for Magic Packet mode, the DP83867 scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

NOTE

The Magic Packet should be byte aligned.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station’s IEEE address or a BROADCAST address), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions, followed by secure-on password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of FFh.

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Feature Description (continued)

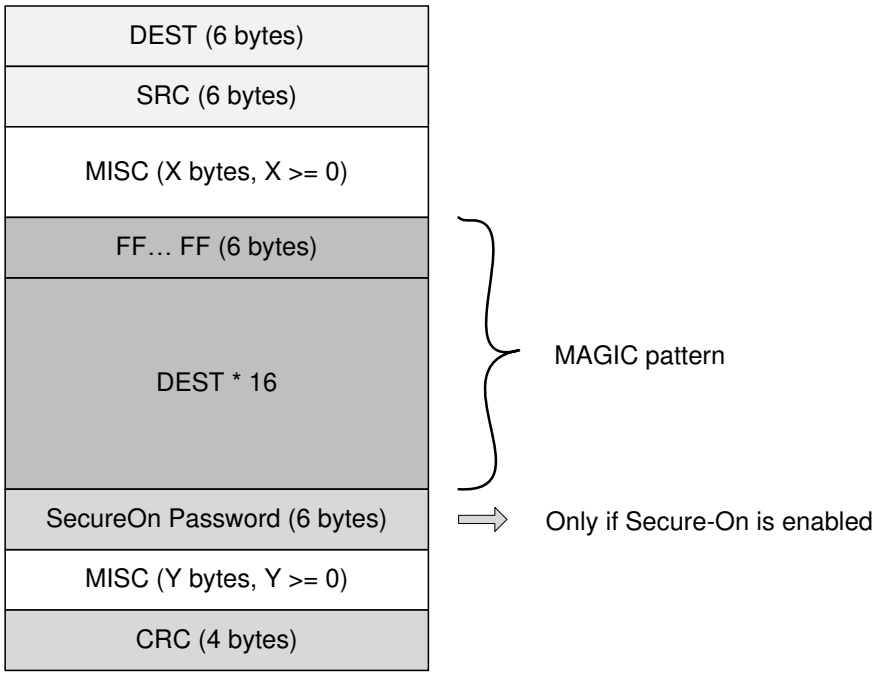

Figure 11. Magic Packet Structure

8.3.1.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a SecureOn Password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
  DESTINATION SOURCE MISC FF FF FF FF FF FF 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44
 55 66 11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

8.3.1.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the RXFCFG register (address 0x0134). Wake-on-LAN status is reported in the RXFSTS register (address 0x0135).

8.3.2 Start of Frame Detect for IEEE 1588 Time Stamp

The DP83867 supports an IEEE 1588 indication pulse at the SFD (start frame delimiter) for the receive and transmit paths. The pulse can be delivered to various pins. The pulse indicates the actual time the symbol is presented on the lines (for transmit), or the first symbol received (for receive). The exact timing of the pulse can be adjusted through register. Each increment of phase value is an 8-ns step.

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Feature Description (continued)

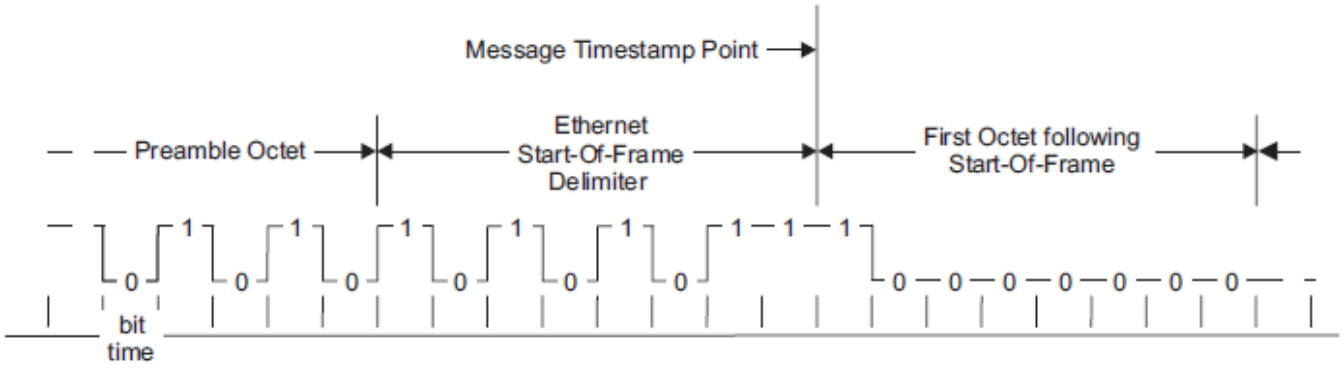

Figure 12. IEEE 1588 Message Timestamp Point

The SFD pulse output can be configured using the GPIO Mux Control registers, GPIO_MUX_CTRL1 (register address 0x0171) and GPIO_MUX_CTRL2 (register address 0x0172). The ENHANCED_MAC_SUPPORT bit in RXCFG (register address 0x0134) must also be set to allow output of the SFD.

For more information about configuring the DP83867's SFD feature, see the *How to Configure DP83867 Start of Frame* application report (SNLA242).

8.3.2.1 SFD Latency Variation and Determinism

Time stamping packet transmission and reception using the RX_CTRL and TX_CTRL signals of RGMII is not accurate enough for latency sensitive protocols. SFD pulses offers system designers a method to improve the accuracy of packet time stamping. The SFD pulse, while varying less than RGMII signals inherently, still exhibits latency variation due to the defined architecture of 1000BASE-T. This section provides a method to determine when an SFD latency variation has occurred and how to compensate for the variation in system software to improve timestamp accuracy.

In the following section the terms baseline latency and SFD variation are used. Baseline latency is the time measured between the TX_SFD pulse to the RX_SFD pulse of a connected link partner, assuming an Ethernet cable with all 4 pairs perfectly matched in propagation time. In the scenario where all 4 pairs being perfectly matched, a 1000BASE-T PHY will not have to align the 4 received symbols on the wire and will not introduce extra latency due to alignment.

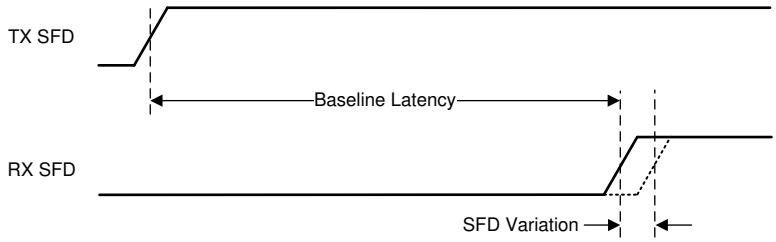

Figure 13. Baseline Latency and SFD Variation in Latency Measurement

SFD variation is additional time added to the baseline latency before the RX_SFD pulse when the PHY must introduce latency to align the 4 symbols from the Ethernet cable. Variation can occur when a new link is established either by cable connection, auto-negotiation restart, PHY reset, or other external system effects. During a single, uninterrupted link, the SFD variation will remain constant.

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Feature Description (continued)

The DP83867 can limit and report the variation applied to the SFD pulse while in the 1000-Mb operating mode. Before a link is established in 1000-Mb mode, the Sync FIFO Control Register (register address 0x00E9) must be set to value 0xDF22. The below SFD variation compensation method can only be applied after the Sync FIFO Control Register has been initialized and a new link has been established. It is acceptable to set the Sync FIFO Control register value and then perform a software restart by setting the SW_RESTART bit[14] in the Control Register (register address 0x001F) if a link is already present.

8.3.2.1.1 1000-Mb SFD Variation in Master Mode

When the DP83867 is operating in 1000-Mb master mode, variation of the RX_SFD pulse can be estimated using the Skew FIFO Status register (register address 0x0055) bit[7:4]. The value read from the Skew FIFO Status register bit[7:4] must be multiplied by 8 ns to estimate the RX_SFD variation added to the baseline latency.

Example: While operating in master 1000-Mb mode, a value of 0x2 is read from the Skew FIFO register bit[7:4]. 2 × 8 ns = 16 ns is subtracted from the TX_SFD to RX_SFD measurement to determine the baseline latency.

8.3.2.1.2 1000-Mb SFD Variation in Slave Mode

When the DP83867 is operating in 1000-Mb slave mode, the variation of the RX_SFD pulse can be determined using the Skew FIFO Status register (register address 0x0055) bit[3:0].The value read from the Skew FIFO Status register bit[3:0] should be multiplied by 8ns to estimate the RX_SFD variation added to the baseline latency.

Example: While operating in slave 1000-Mb mode, a value of 0x1 is read from the Skew FIFO register bit[3:0]. 1 × 8 ns = 8 ns is subtracted from the TX_SFD to RX_SFD measurement to determine the baseline latency.

8.3.2.1.3 100-Mb SFD Variation

The latency variation in 100-Mb mode of operation is determined by random process and does not require any register readout or system level compensation of SFD pulses.

8.3.3 Clock Output

The DP83867 has several internal clocks, including the local reference clock, the Ethernet transmit clock, and the Ethernet receive clock. An external crystal or oscillator provides the stimulus for the local reference clock. The local reference clock acts as the central source for all clocking in the device.

The local reference clock is embedded into the transmit network packet traffic and is recovered from the network packet traffic at the receiver node. The receive clock is recovered from the received Ethernet packet data stream and is locked to the transmit clock in the partner.

Using the I/O Configuration register (address 0x0170), the DP83867 can be configured to output these internal clocks through the CLK_OUT pin. By default, the output clock is synchronous to the XI oscillator / crystal input. The default output clock is suitable for use as the reference clock of another DP83867 device. Through registers, the output clock can be configured to be synchronous to the receive data at the 125-MHz data rate or at the divide by 5 rate of 25 MHz. It can also be configured to output the line driver transmit clock. When operating in 1000Base-T mode, the output clock can be configured for any of the four transmit or receive channels.

The output clock can be disabled using the CLK_O_DISABLE bit of the I/O Configuration register.

8.4 Device Functional Modes

8.4.1 MAC Interfaces

The DP83867 supports connection to an Ethernet MAC through the following interfaces: SGMII and RGMII.

The SGMII Enable (LED_0) strap allows the user to turn the SGMII MAC interface on or off. The SGMII Enable strap corresponds to the SGMII Enable (bit 11) in the PHYCR register (address 0x0010).

The SGMII enable has higher priority than the RGMII enable. Table 2 is the configuration table for the MAC interfaces:

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Device Functional Modes (continued)

Table 2. Configuration Table for the MAC Interfaces

SGMII ENABLE (REGISTER 0x0010, BIT 11)	RGMII ENABLE (REGISTER 0x0032, BIT 7)	DEVICE FUNCTIONAL MODE
0x1	0x1	SGMII
0x1	0x0	SGMII
0x0	0x1	RGMII

The initial strap values for the SGMII enable and the RGMII disable are also available in the Strap Configuration Status Register 1 (STRAP_STS1).

8.4.1.1 Serial GMII (SGMII)

The Serial Gigabit Media Independent Interface (SGMII) provides a means of conveying network data and port speed between a 100/1000 PHY and a MAC with significantly less signal pins (4 or 6 pins) than required for GMII (24 pins) or RGMII (12 pins). The SGMII interface uses 1.25-Gbps LVDS differential signaling which has the added benefit of reducing EMI emissions relative to GMII or RGMII.

Because the internal clock and data recovery circuitry (CDR) of DP83867 can detect the transmit timing of the SGMII data, TX_CLK is not required. SGMII interface is capable of working as a 4-wire or 6-wire SGMII interface. The default SGMII connection is through four wires. Two differential pairs are used for the transmit and receive connections. Clock and data recovery are performed in the MAC and in the PHY, so no additional differential pair is required for clocking. Alternately, if the MAC is not capable of recovering the clock from the SGMII receive data, the DP83867 can be configured to provide the SGMII receive clock through a differential pair.

The 1.25-Gbps rate of SGMII is excessive for 100-Mbps operation. When operating in 100-Mbps mode, the PHY *elongates* the frame by replicating each frame byte 10 times. This frame elongation takes place *above* the IEEE 802.3 PCS layer, thus the start of frame delimiter only appears once per frame.

The SGMII interface includes Auto-Negotiation capability. Auto-Negotiation provides a mechanism for control information to be exchanged between the PHY and the MAC. This allows the interface to be automatically configured based on the media speed mode resolution on the MDI side. In MAC loopback mode, the SGMII speed is determined by the MDI speed selection. The SGMII interface works in both Auto-Negotiation and forced speed mode during the MAC loopback operation. SGMII Auto-Negotiation is the default mode of the operation.

The SGMII Auto-Negotiation process can be disabled and the SGMII speed mode can be forced to the MDI resolved speed. The SGMII forced speed mode can be enabled with the MDI auto-negotiation or MDI manual speed mode. SGMII Auto-Negotiation can be disabled through the SGMII_AUTONEG_EN register bit in the CFG2 register (address 0x0014).

The 10M_SGMII_RATE_ADAPT bit (bit 7) does not need to be changed for 10M speed as the PHY will automatically adapt the rate of SGMII.

SGMII is enabled through a resistor strap option. See *Strap Configuration* for details.

All SGMII connections must be AC-coupled through an 0.1-µF capacitor.

The connection diagrams for 4-wire SGMII and 6-wire SGMII are shown in Figure 14 and Figure 15.

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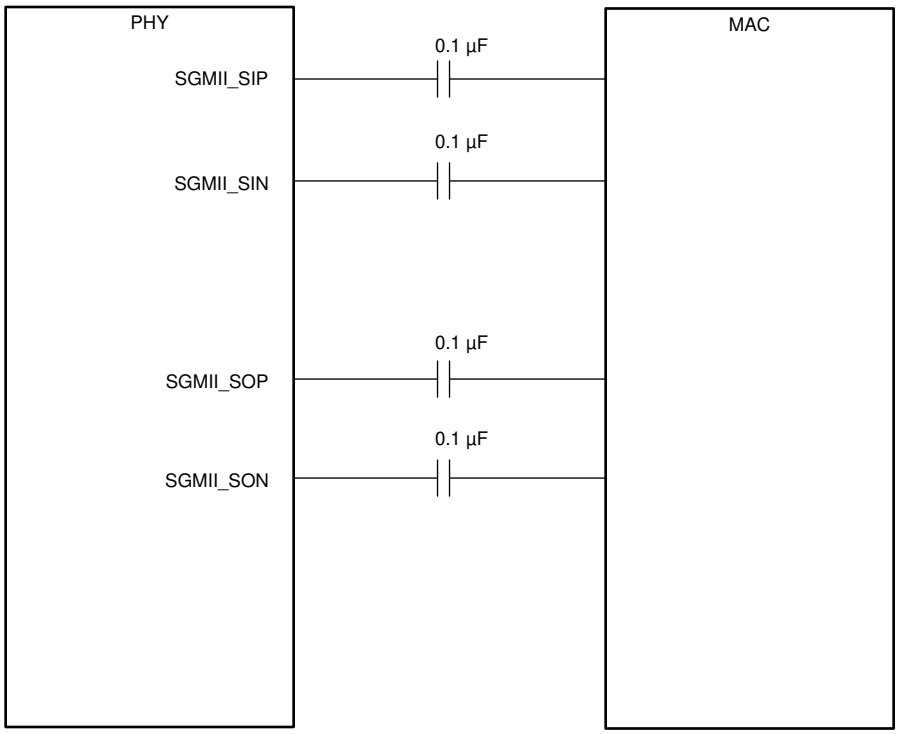

Figure 14. SGMII 4-Wire Connections

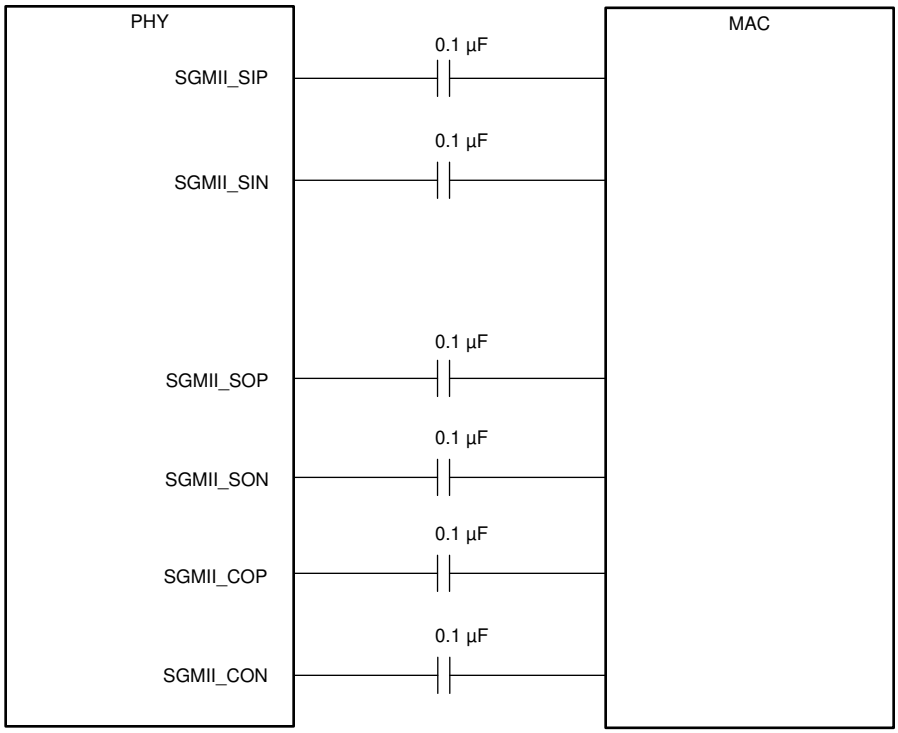

Figure 15. SGMII 6-Wire Connections

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8.4.1.2 Reduced GMII (RGMII)

The Reduced Gigabit Media Independent Interface (RGMII) is designed to reduce the number of pins required to interconnect the MAC and PHY (12 pins for RGMII relative to 24 pins for GMII). To accomplish this goal, the data paths and all associated control signals are reduced and are multiplexed. Both rising and trailing edges of the clock are used. For Gigabit operation the GTX_CLK and RX_CLK clocks are 125 MHz, and for 10- and 100-Mbps operation, the clock frequencies are 2.5 MHz and 25 MHz, respectively.

For more information about RGMII timing, see the *RGMII Interface Timing Budgets* application report (SNLA243).

8.4.1.2.1 1000-Mbps Mode Operation

All RGMII signals are positive logic. The 8-bit data is multiplexed by taking advantage of both clock edges. The lower 4 bits are latched on the positive clock edge and the upper 4 bits are latched on trailing clock edge. The control signals are multiplexed into a single clock cycle using the same technique.

To reduce power consumption of RGMII interface, TXEN_ER and RXDV_ER are encoded in a manner that minimizes transitions during normal network operation. This is done by following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock. In RGMII mode, GMII_TX_ER is presented on TX_CTRL at the falling edge of the GTX_CLK clock. RX_CTRL coding is implemented the same fashion.

When receiving a valid frame with no error, *RX_CTRL = True* is generated as a logic high on the rising edge of RX_CLK and *RX_CTRL = False* is generated as a logic high at the falling edge of RX_CLK. When no frame is being received, *RX_CTRL = False* is generated as a logic low on the rising edge of RX_CLK and *RX_CTRL = False* is generated as a logic low on the falling edge of RX_CLK.

TX_CTRL is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of GTX_CLK and during the period between frames where no error is indicated, the signal stays low for both edges.

8.4.1.2.2 1000-Mbps Mode Timing

The DP83867 provides configurable clock skew for the GTX_CLK and RX_CLK to optimize timing across the interface. The transmit and receive paths can be optimized independently. Both the transmit and receive path support 16 programmable RGMII delay modes through register configuration. Strap configuration can also be used to configure 8 programmable RGMII modes for both the transmit and receive paths. See *Strap Configuration* for details.

The timing paths can either be configured for Aligned mode or Shift mode. In Aligned mode, no clock skew is introduced. In Shift mode, the clock skew can be introduced in 0.5-ns increments (through strap configuration) or in 0.25-ns increments (through register configuration). Configuration of the Aligned mode or Shift mode is accomplished through the RGMII Control Register (RGMIICTL), address 0x0032. In Shift mode, the clock skew can be adjusted using the RGMII Delay Control Register (RGMIIDCTL), address 0x0086.

8.4.1.2.3 10- and 100-Mbps Mode

When the RGMII interface is operating in the 100-Mbps mode, the Ethernet Media Independent Interface (MII) is implemented by reducing the clock rate to 25 MHz. For 10-Mbps operation, the clock is further reduced to 2.5 MHz. In the RGMII 10/100 mode, the transmit clock RGMII TX_CLK is generated by the MAC and the receive clock RGMII RX_CLK is generated by the PHY. During the packet receiving operation, the RGMII RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the free-running clock to a data synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitch is allowed on the clock signals during clock speed transitions.

This interface operates at 10- and 100-Mbps speeds the same way it does at 1000-Mbps mode with the exception that the data may be duplicated on the falling edge of the appropriate clock.

The MAC holds the RGMII TX_CLK low until it has ensured that it is operating at the same speed as the PHY.

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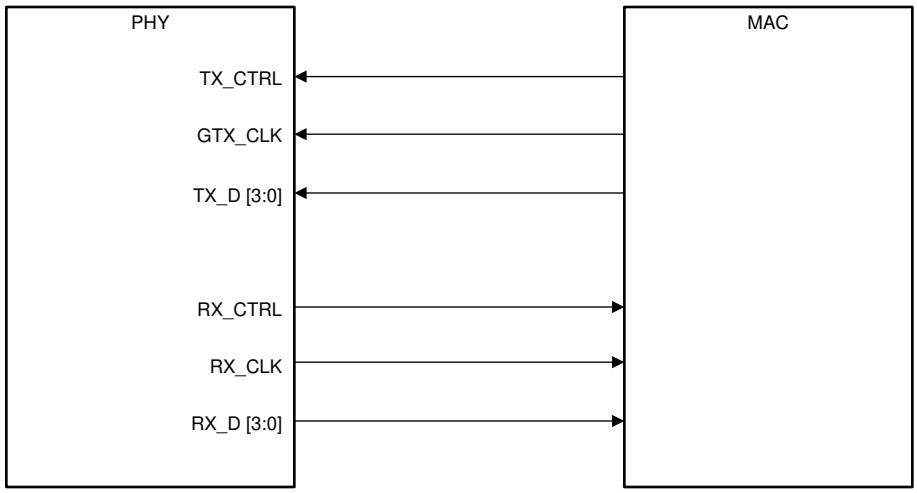

Figure 16. RGMII Connections

8.4.2 Serial Management Interface

The Serial Management Interface (SMI), provides access to the DP83867 internal register space for status information and configuration. The SMI is compatible with IEEE 802.3-2002 clause 22. The implemented register set consists of the registers required by the IEEE 802.3, plus several others to provide additional visibility and controllability of the DP83867 device.

The SMI includes the MDC management clock input and the management MDIO data pin. The MDC clock is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 25 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

The MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC clock. The MDIO pin requires a pullup resistor (2.2 kΩ) which, during IDLE and turnaround, pulls MDIO high.

Up to 16 PHYs can share a common SMI bus. To distinguish between the PHYs, a 4-bit address is used. During power-up reset, the DP83867 latches the PHY_ADD configuration pins to determine its address. The DP83867IRPAP 64-pin variant can support up to 32 PHYs and uses a 5-bit address.

The management entity must not start an SMI transaction in the first cycle after power-up reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83867 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. Figure 17 shows the timing relationship between MDC and the MDIO as driven and received by the Station (STA) and the DP83867 (PHY) for a typical register read access.

For write transactions, the station-management entity writes data to the addressed DP83867, thus eliminating the requirement for MDIO turnaround. The turnaround time is filled by the management entity by inserting <10>. Figure 17 shows the timing relationship for a typical MII register write access. The frame structure and general read and write transactions are shown in Table 3, Figure 17, and Figure 18.

Table 3. Typical MDIO Frame Format

TYPICAL MDIO FRAME FORMAT	<idle><start><op code><device addr><reg addr><turnaround><data<idle>
Read Operation	<idle><01><10><AAAA><RRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01<01><AAAA><RRRR><10><xxxx xxxx xxxx xxxx><idle>

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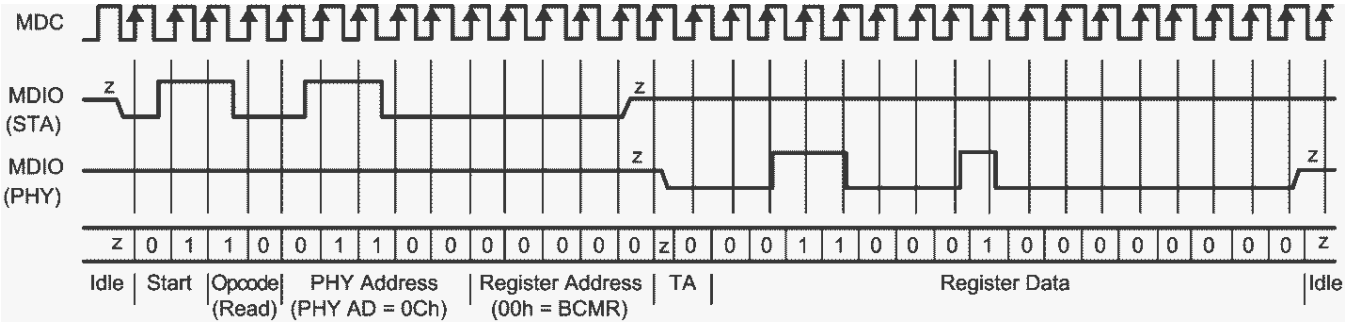

Figure 17. Typical MDC/MDIO Read Operation

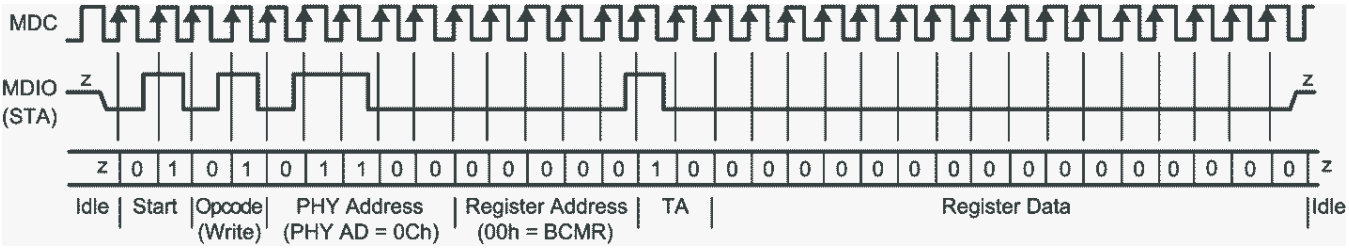

Figure 18. Typical MDC/MDIO Write Operation

8.4.2.1 Extended Address Space Access

The DP83867 SMI function supports read or write access to the extended register set using registers REGCR (0x000Dh) and ADDAR (0x000Eh) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for clause 22 for accessing the clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR (0x000Dh) and ADDAR (0x000Eh) which is accessed only using the normal MDIO transaction. The SMI function ignores indirect accesses to these registers.

REGCR (0x000Dh) is the MDIO Manageable MMD access control. In general, register REGCR(4:0) is the device address DEVAD that directs any accesses of ADDAR (0x000Eh) register to the appropriate MMD.

The DP83867 supports one MMD device address. The vendor-specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.

All accesses through registers REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address and data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:1] is 00, then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to 00, accesses to register ADDAR modify the extended register set address register. This address register must always be initialized to access any of the registers within the extended register set.
- When REGCR[15:14] is set to 01, accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to 10, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to 11, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

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The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111).

8.4.2.1.1 Write Address Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

8.4.2.1.2 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

8.4.2.1.3 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note: steps (1) and (2) can be skipped if the address register was previously configured.

8.4.2.1.4 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

Note: steps (1) and (2) can be skipped if the address register was previously configured.

8.4.2.1.5 Write (Post Increment) Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address from register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11. DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.4.2.1.6 Read (Post Increment) Operation

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) to

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register REGCR.

4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.4.2.1.7 Example of Read Operation Using Indirect Register Access

Read register 0x0170.

1. Write register 0x0D to value 0x001F.
2. Write register 0x0E to value 0x0170
3. Write register 0x0D to value 0x401F.
4. Read register 0x0E.

The expected default value is 0x0C10.

8.4.2.1.8 Example of Write Operation Using Indirect Register Access

Write register 0x0170 to value 0x0C50.

1. Write register 0x0D to value 0x001F.
2. Write register 0x0E to value 0x0170
3. Write register 0x0D to value 0x401F.
4. Write register 0x0E to value 0x0C50.

This write disables the output clock on the CLK_OUT pin.

8.4.3 Auto-Negotiation

All 1000BASE-T PHYs are required to support Auto-Negotiation. The Auto-Negotiation function in 1000BASE-T has three primary purposes:

- Auto-Negotiation of Speed and Duplex Selection
- Auto-Negotiation of Master or Slave Resolution
- Auto-Negotiation of Pause or Asymetrical Pause Resolution

8.4.3.1 Speed and Duplex Selection - Priority Resolution

The Auto-Negotiation function provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging Fast Link Pulses (FLP). FLPs are burst pulses that provide the signalling used to communicate the abilities between two devices at each end of a link segment. For further details regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3 specification. The DP83867 supports 1000BASE-T, 100BASE-TX, and 1000BASE-T modes of operation. The process of Auto-Negotiation ensures that the highest performance protocol is selected (that is, priority resolution) based on the advertised abilities of the Link Partner and the local device.

8.4.3.2 Master and Slave Resolution

If 1000BASE-T mode is selected during the priority resolution, the second goal of Auto-Negotiation is to resolve Master or Slave configuration. The Master mode priority is given to the device that supports multiport nodes, such as switches and repeaters. Single node devices such as DTE or NIC card takes lower Master mode priority.

8.4.3.3 Pause and Asymmetrical Pause Resolution

When Full-Duplex operation is selected during priority resolution, the Auto-Negotiation also determines the Flow Control capabilities of the two link partners. Flow control was originally introduced to force a busy station's Link Partner to stop transmitting data in Full-Duplex operation. Unlike Half-Duplex mode of operation where a link partner could be forced to back off by simply generating collisions, the Full-Duplex operation needed a mechanism to slow down transmission from a link partner in the event that the receiving station's buffers are becoming full. A new MAC control layer was added to handle the generation and reception of Pause Frames. Each MAC Controller has to advertise whether it is capable of processing Pause Frames. In addition, the MAC Controller advertises if Pause frames can be handled in both directions, that is, receive and transmit. If the MAC Controller only generates Pause frames but does not respond to Pause frames generated by a link partner, it is

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called Asymmetrical Pause. The advertisement of Pause and Asymmetrical Pause capabilities is enabled by writing 1 to bits 10 and 11 of ANAR (register address 0x0004). The link partner's Pause capabilities is stored in ANLPAR (register address 0x0005) bits 10 and 11. The MAC Controller has to read from ANLPAR to determine which Pause mode to operate. The PHY layer is not involved in Pause resolution other than simply advertising and reporting of Pause capabilities.

8.4.3.4 Next Page Support

The DP83867 supports the Auto-Negotiation Next Page protocol as required by IEEE 802.3 clause 28.2.4.1.7. The ANNPTR 0x07 allows for the configuration and transmission of the Next Page. Refer to clause 28 of the IEEE 802.3 standard for detailed information regarding the Auto-Negotiation Next Page function.

8.4.3.5 Parallel Detection

The DP83867 supports the Parallel Detection function as defined in the IEEE 802.3 specification. Parallel Detection requires the 10/100-Mbps receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation, yet is transmitting link signals that the 10BASE-Te or 100BASE-X PMA recognize as valid link signals.

If the DP83867 completes Auto-Negotiation as a result of Parallel Detection, without Next Page operation, bits 5 and 7 of ANLPAR (register address 0x0005) are set to reflect the mode of operation present in the Link Partner. Note that bits 4:0 of the ANLPAR are also set to 00001 based on a successful parallel detection to indicate a valid 802.3 selector field. Software may determine that the negotiation is completed through Parallel Detection by reading 0 in bit 0 of ANER (register address 0x006) after Auto-Negotiation Complete, bit 5 of BMSR (register address 0x0001), is set. If the PHY is configured for parallel detect mode and any condition other than a good link occurs, the parallel detect fault, bit 4 of ANER (register address 0x06), sets.

8.4.3.6 Restart Auto-Negotiation

If a link is established by successful Auto-Negotiation and then lost, the Auto-Negotiation process resumes to determine the configuration for the link. This function ensures that a link can be re-established if the cable becomes disconnected and reconnected. After Auto-Negotiation is completed, it may be restarted at any time by writing 1 to bit 9 of the BMCR (register address 0x0000). A restart Auto-Negotiation request from any entity, such as a management agent, causes DP83867 to halt data transmission or link pulse activity until the break_link_timer expires. Consequently, the Link Partner goes into link fail mode and the resume Auto-Negotiation. The DP83867 resumes Auto-Negotiation after the break_link_timer has expired by transmitting FLP (Fast Link Pulse) bursts.

8.4.3.7 Enabling Auto-Negotiation Through Software

If Auto-Negotiation is disabled by MDIO access, and the user desires to restart Auto-Negotiation, this could be accomplished by software access. Bit 12 of BMCR (register address 0x00) should be cleared and then set for Auto-Negotiation operation to take place.

If Auto-Negotiation is disabled by strap option, Auto-Negotiation can not be reenabled.

8.4.3.8 Auto-Negotiation Complete Time

Parallel detection and Auto-Negotiation typically take 2-3 seconds to complete. In addition, Auto-Negotiation with next page exchange takes approximately 2-3 seconds to complete, depending on the number of next pages exchanged. Refer to Clause 28 of the IEEE 802.3 standard for a full description of the individual timers related to Auto-Negotiation

8.4.3.9 Auto-MDIX Resolution

The DP83867 can determine if a *straight* or *crossover* cable is used to connect to the link partner. It can automatically re-assign channel A and B to establish link with the link partner, (and channel C and D in 1000BASE-T mode). Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2. It is not a required implementation for 10BASE-Te and 100BASE-TX.

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Auto-MDIX can be enabled or disabled by register configuration, using bit 6 of the PHYCR register (address 0x0010). When Auto-MDIX is disabled, the PMA is forced to either MDI (*straight*) or MDIX (*crossed*). Manual configuration of MDI or MDIX can also be accomplished by register configuration, using bit 5 of the PHYCR register.

For 10/100, Auto-MDIX is independent of Auto-Negotiation. Auto-MDIX works in both Auto-Negotiation mode and manual forced speed mode.

8.4.4 Loopback Mode

There are several options for Loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths. Generally, the DP83867 may be configured to one of the Near-end loopback modes or to the Far-end (reverse) loopback. MII Loopback is configured using the BMCR (register address 0x0000). All other loopback modes are enabled using the BISCR (register address 0x16). Except where otherwise noted, loopback modes are supported for all speeds (10/100/1000) and all MAC interfaces (SGMII and RGMII).

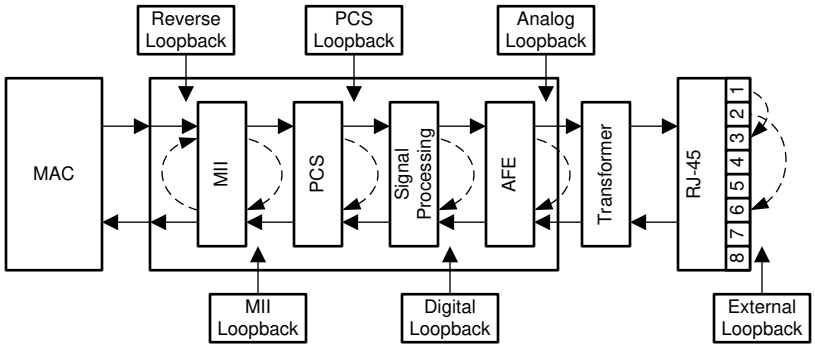

Figure 19. Loopbacks

The availability of Loopback depends on the operational mode of the PHY. The Link Status in these loopback modes is also affected by the operational mode. Table 4 lists out the availability of Loopback Modes and their corresponding Link Status indication.

Table 4. Loopback Availability

LOOPBACK MODE	MAC INTERFACE	1000M		100M		10M	
		AVAILABILITY	LINK STATUS	AVAILABILITY	LINK STATUS	AVAILABILITY	LINK STATUS
MII	RGMII	Yes	No	Yes	No	Yes	No
PCS	RGMII	Yes	No	Yes	Yes	No	No
Digital	RGMII	Yes	Yes	Yes	Yes	Yes	Yes
Analog	RGMII	Yes	Yes	Yes	Yes	Yes	Yes
External	RGMII	No	No	Yes	Yes	Yes	Yes
MII	SGMII	Yes	No	Yes	No	No	No
Digital	SGMII	Yes	Yes	Yes	Yes	No	No
IO	SGMII	Yes	Yes	Yes	Yes	No	No

8.4.4.1 Near-End Loopback

Near-end loopback provides the ability to loop the transmitted data back to the receiver through the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits with several options being provided.

When configuring loopback modes, the Loopback Configuration Register (LOOPCR), address 0x00FE, should be set to 0xE720.

To maintain the desired operating mode, Auto-Negotiation should be disabled before selecting the Near-End Loopback mode. This constraint does not apply for external-loopback mode.

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Auto-MDIX should be disabled before selecting the Near-End Loopback mode. MDI or MDIX configuration should be manually configured.

8.4.4.1.1 MII Loopback

MII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. While in MII Loopback mode the data is looped back, and can also be configured through register to transmit onto the media.

8.4.4.1.2 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

8.4.4.1.3 Digital Loopback

Digital Loopback includes the entire digital transmit – receive path. Data is looped back prior to the analog circuitry.

8.4.4.1.4 Analog Loopback

Analog Loopback includes the entire analog transmit-receive path.

8.4.4.2 External Loopback

When operating in 10BASE-Te or 100Base-T mode, signals can be looped back at the RJ-45 connector by wiring the transmit pins to the receive pins. Due to the nature of the signaling in 1000Base-T mode, this type of external loopback is not supported. Analog loopback provides a way to loop data back in the analog circuitry when operating in 1000Base-T mode. For proper operation in Analog Loopback mode, attach 100-Ω terminations to the RJ45 connector.

8.4.4.3 Far-End (Reverse) Loopback

Far-end (Reverse) Loopback is a special test mode to allow testing the PHY from the link-partner side. In this mode, data that is received from the link partner passes through the PHY's receiver, is looped back at the MAC interface and is transmitted back to the link partner. While in Reverse Loopback mode, all data signals that come from the MAC are ignored. Through register configuration, data can also be transmitted onto the MAC Interface.

8.4.5 BIST Configuration

The device incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. The BIST can be performed using both internal loopback (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines.

The BIST is implemented with independent transmit and receive paths, with the transmit block generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for the BIST. The received data is compared to the generated pseudo-random data by the BIST Linear Feedback Shift Register (LFSR) to determine the BIST pass or fail status. The number of error bytes that the PRBS checker received is stored in the BICSR2 register (0x0072). The status of whether the PRBS checker is locked to the incoming receive bit stream, whether the PRBS has lost sync, and whether the packet generator is busy, can be read from the STS2 register (0x0017h). While the lock and sync indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the BICSR2 register (0x0072). The number of received bytes are stored in BICSR1 (0x0071).

The PRBS test can be put in a continuous mode by using bit 14 of the BISCR register (0x0016h). In continuous mode, when one of the PRBS counters reaches the maximum value, the counter starts counting from zero again. Packet transmission can be configured for one of two types, 64 and 1518 bytes, through register bit 13 of the BISCR register (0x0016).

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8.4.6 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for reliable, comprehensive and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies, and connectors deployed results in the need to non-intrusively identify and report cable faults. The TI cable-diagnostic unit provides extensive information about cable integrity. The DP83867 offers, Time Domain Reflectometry (TDR) capability in its Cable Diagnostic tools kit.

8.4.6.1 TDR

The DP83867 uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts, and any other discontinuities along the cable.

The DP83867 transmits a test pulse of known amplitude (1 V or 2.5 V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, bad connector, and from the end of the cable itself. After the pulse transmission, the DP83867 measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors), improperly-terminated cables, and crossed pairs wires with ±1-m accuracy.

The DP83867 also uses data averaging to reduce noise and improve accuracy. The DP83867 can record up to five reflections within the tested pair. If more than 5 reflections are recorded, the DP83867 saves the first 5 of them. If a cross fault is detected, the TDR saves the first location of the cross fault and up to 4 reflections in the tested channel. The DP83867 TDR can measure cables beyond 100 m in length.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition, and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the DP83867 in the following scenarios:

- While Link partner is disconnected – cable is unplugged at the other side
- Link partner is connected but remains *quiet* (for example, in power-down mode)
- TDR could be automatically activated when the link fails or is dropped by setting bit 7 of register 0x0009 (CFG1). The results of the TDR run after the link fails are saved in the TDR registers.

Software could read these registers at any time to apply post processing on the TDR results. This mode is designed for cases when the link dropped due to cable disconnections; after link failure, for instance, the line is quiet to allow a proper function of the TDR.

8.4.6.2 Energy Detect

The energy-detector module provides signal-strength indication in various scenarios. Because it is based on an IIR filter, this robust energy detector has excellent reaction time and reliability. The filter output is compared to predefined thresholds to decide the presence or absence of an incoming signal. The energy detector also implements hysteresis to avoid jittering in signal-detect indication. Additionally, it has fully-programmable thresholds and listening-time periods, enabling shortening of the reaction time if required.

8.4.6.3 Fast Link Drop (FLD)

The DP83867 includes advanced link-drop capabilities that support various real-time applications. The link drop mechanism is configurable and includes enhanced modes that allow extremely fast reaction times to link drops.

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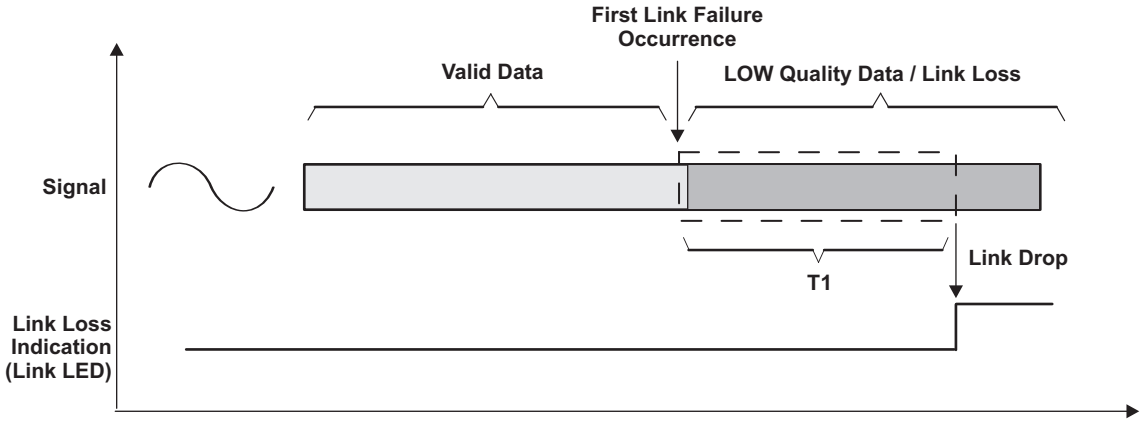

Figure 20. Fast Link Drop Mechanism

As described in Figure 20, the link loss mechanism is based on a time window search period in which the signal behavior is monitored. The T1 window is set by default to reduce typical link drops to less than 1 ms in 100=M and 0.5 ms in 1000-M mode.

The DP83867 supports enhanced modes that shorten the window called Fast Link Drop mode. In this mode, the T1 window is shortened significantly, in most cases less than 10 μs. In this period of time, there are several criteria allowed to generate link loss event and drop the link:

1. Loss of descrambler sync
2. Receive errors
3. MLT3 errors
4. Mean Squared Error (MSE)
5. Energy loss

The Fast Link Drop functionality allows the use of each of these options separately or in any combination. Note that because this mode enables extremely quick reaction time, it is more exposed to temporary bad link quality scenarios.

NOTE

When Fast Link Drop functionality is enabled on both the DUT and LP (link partner) and Link Drop is detected, it is essential to disable FLD using bit 14 of the FLD_CFG register (address 0x002D) for the link to re-establish. Once the link is up FLD can be enabled again using the same bit (FLD_CFG bit[14]).

8.4.6.4 Fast Link Detect

Several advanced modes are available for fast link establishment. Unlike the Auto-Negotiation and Auto-MDIX mechanisms defined by the IEEE 802.3 specification, these modes are specific to the DP83867. Take care when implementing these modes. For best operation, TI recommends implementing these modes with a DP83867 on both ends of the link.

These advanced link and crossover modes depend on the speed selected for the link. Some modes are intended for use in 1000Base-T operation. Others are intended for use in 100Base-TX operation.

Fast Link Detect functionality can be configured using the Configuration Register 3 (CFG3), address 0x001E.

8.4.6.5 Speed Optimization

Speed optimization, also known as link downshift, enables fallback to 100-M operation after multiple consecutive failed attempts at Gigabit link establishment. Such a case could occur if cabling with only four wires (two twisted pairs) were connected instead of the standard cabling with eight wires (four twisted pairs).

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The number of failed link attempts before falling back to 100-M operation is configurable. By default, four failed link attempts are required before falling back to 100 M.

In enhanced mode, fallback to 100 M can occur after one failed link attempt if energy is not detected on the C and D channels. Speed optimization also supports fallback to 10 M if link establishment fails in Gigabit and in 100-M mode.

Speed optimization can be enabled through register configuration.

8.4.6.6 Mirror Mode

In some multiport applications, RJ-45 ports may be mirrored relative to one another. This mirroring can require crossing board traces. The DP83867 can resolve this issue by implementing mirroring of the ports inside the device.

In 10/100 operation, the mapping of the port mirroring is:

MDI MODE	MIRROR PORT CONFIGURATION
MDI	A → D
	B → C
MDIX	A → D
	B → C

In Gigabit operation, the mapping of the port mirroring is:

MDI MODE	MIRROR PORT CONFIGURATION
MDI or MDIX	A → D
	B → C
	C → B
	D → A

Mirror mode can be enabled through strap or through register configuration using the Port Mirror Enable bit in the CFG4 register (address 0x0031). In Mirror mode, the polarity of the signals is also reversed.

8.4.6.7 Interrupt

The DP83867 can be configured to generate an interrupt when changes of internal status occur. The interrupt allows a MAC to act upon the status in the PHY without polling the PHY registers. The interrupt source can be selected through the interrupt registers, MICR (register address 0x0012) and ISR (register address 0x0013).

8.4.6.8 IEEE 802.3 Test Modes

IEEE 802.3 specification for 1000BASE-T requires that the PHY layer be able to generate certain well defined test patterns on TX outputs. Clause 40 section 40.6.1.1.2 *Test Modes* describes these tests in detail. There are four test modes as well as the normal operation mode. These modes can be selected by writing to the CFG1 register (address 0x0009).

See IEEE 802.3 section 40.6.1.1.2 *Test modes* for more information on the nature of the test modes. The DP83867 provides a test clock synchronous to the IEEE test patterns. The test patterns are output on the MDI pins of the device and the transmit clock is output on the CLK_OUT pin.

For more information about configuring the DP83867 for IEEE 802.3 compliance testing, see the *How to Configure DP838XX for Ethernet Compliance Testing* application report (SNLS239).

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8.5 Programming

8.5.1 Strap Configuration

The DP83867 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below. The functional pin name is indicated in parentheses.

The strap pins supported are 4-level straps, which are described in greater detail below.

NOTE

Because strap pins may have alternate functions after reset is deasserted, they should not be connected directly to VDD or GND.

Configuration of the device may be done through the 4-level strap pins or through the management register interface. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the 4-level strap pin input and the supply to select one of the possible selected modes.

The MAC interface pins must support I/O voltages of 3.3 V, 2.5 V, and 1.8 V. As the strap inputs are implemented on these pins, the straps must also support operation at 3.3-V, 2.5-V, and 1.8-V supplies.

For more information about configuring 4-level straps, see the *Configuring Ethernet Devices with 4-Level Straps* application report (SNLA258).

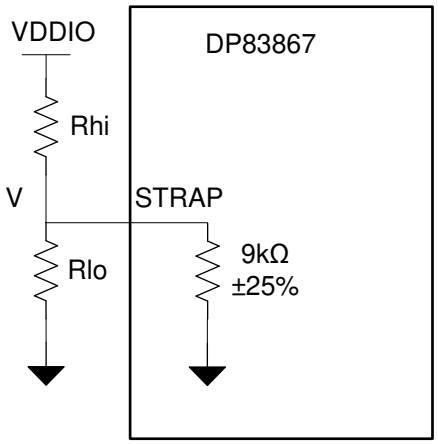

Figure 21. Strap Circuit

Table 5. 4-Level Strap Resistor Ratios

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

For SGMII Mode 4 strap, TI recommends using Rhi = 4 kΩ and Rlo = 10 kΩ on RX_D0 and RX_D1 , RX_D2 and RX_D3.

All straps have a 9 kΩ ±25% internal pulldown resistor. The voltage at strap pins should be between the Vmin and Vmax mentioned in the *Target Voltage* column in Table 5. Strap resistors with 1% tolerance are recommended.

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The following tables describes the DP83867 configuration straps:

Table 6. 4-Level Strap Pins

PIN NAME	48 VQFN PIN #	DEFAULT	STRAP FUNCTION		
RX_D0	33	[00]	**MODE**	PHY_ADD1	PHY_ADD0
			1	0	0
			2	0	1
			3	1	0
			4	1	1
RX_D2	35	[00]	**MODE**	PHY_ADD3	PHY_ADD2
			1	0	0
			2	0	1
			3	1	0
			4	1	1
RX_CTRL (1)	38	[00]	**MODE**		Autoneg Disable
			1		N/A
			2		N/A
			3		0
			4		1
GPIO_0 (2)	39	[00]	**MODE**	RGMII Clock Skew RX[0]	
			1	0	
			2	Not Applicable	
			3	1	
			4	Not Applicable	
GPIO_1	40	[00]	**MODE**	RGMII Clock Skew RX[2]	RGMII Clock Skew RX[1]
			1	0	0
			2	0	1
			3	1	0
			4	1	1
LED_2	45	[00]	**MODE**	RGMII Clock Skew TX[1]	RGMII Clock Skew TX[0]
			1	0	0
			2	0	1
			3	1	0
			4	1	1

(1) Strap modes 1 and 2 are not applicable for RX_CTRL. The RX_CTRL strap must be configured for strap mode 3 or strap mode 4. If the RX_CTRL pin cannot be strapped to mode 3 or mode 4, bit[7] of Configuration Register 4 (address 0x0031) must be cleared to 0. Autoneg Disable should always be set to 0 when using gigabit Ethernet.
(2) Only Mode 1 and 3 are valid for GPIO_0. Mode 2 and 4 are not applicable and should not be used.

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Table 6. 4-Level Strap Pins (continued)

PIN NAME	48 VQFN PIN #	DEFAULT	STRAP FUNCTION		
LED_1	46	[00]	**MODE**	ANEG_SEL	RGMII Clock Skew TX[2]
			1	0	0
			2	0	1
			3	1	0
			4	1	1
LED_0	47	[00]	**MODE**	Mirror Enable	SGMII Enable
			1	0	0
			2	0	1
			3	1	0
			4	1	1

NOTE

RX_D1 is not a strap input, but this pin must be populated with the same strap resistors chosen for RX_D0. RX_D0 and RX_D1 form an SGMII differential pair. The dummy straps on RX_D1 are required to provide a balanced load for this SGMII differential pair.

NOTE

RX_D3 is not a strap input, but this pin must be populated with the same strap resistors chosen for RX_D2. RX_D2 and RX_D3 form an SGMII differential pair. The dummy straps on RX_D3 are required to provide a balanced load for this SGMII differential pair.

Table 7. Auto-Negotiation Select Strap Details

MODE	ANEG_SEL	REMARKS
10/100/1000	0	advertise ability of 10/100/1000
100/1000	1	advertise ability of 100/1000 only

Table 8. RGMII Transmit Clock Skew Details

MODE	RGMII CLOCK SKEW TX[2]	RGMII CLOCK SKEW TX[1]	RGMII CLOCK SKEW TX[0]	RGMII TX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

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Table 9. RGMII Receive Clock Skew Details

MODE	RGMII CLOCK SKEW RX[2]	RGMII CLOCK SKEW RX[1]	RGMII CLOCK SKEW RX[0]	RGMII RX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

8.5.2 LED Configuration

The DP83867 supports four configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2. A GPIO pin can also be configured to operate as LED_3. Several functions can be multiplexed onto the LEDs for different modes of operation. The LED operation mode can be selected using the LEDCR1 register (address 0x0018).

Because the LED output pins are also used as straps, the external components required for strapping and LED usage must be considered to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding AN input upon power up or reset.

If a given strap input is resistively pulled low then the corresponding output is configured as an active high driver. In the context of the 4-level straps, this occurs for modes 1, 2, and 3. Conversely, if a given strap input is resistively pulled high, then the corresponding output is configured as an active low driver. In the context of the 4-level straps, this occurs only for mode 4.

Refer to Figure 22 for an example of strap connections to external components. In this example, the strapping results in Mode 1 for LED_0 and Mode 4 for LED_1.

The adaptive nature of the LED outputs helps to simplify potential implementation issues of these dual purpose pins.

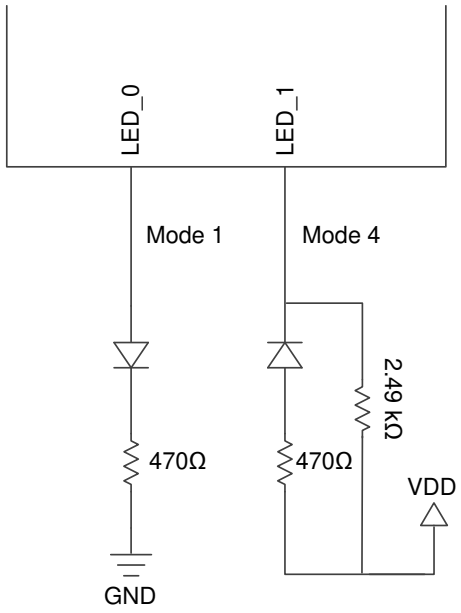

Figure 22. Example Strap Connections

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8.5.3 LED Operation From 1.8-V I/O VDD Supply

Operation of LEDs from a 1.8-V supply results in dim LED lighting. For best results, the recommendation is to operate from a higher supply (2.5 V or 3.3 V). Refer to Figure 23 for a possible implementation of this functionality.

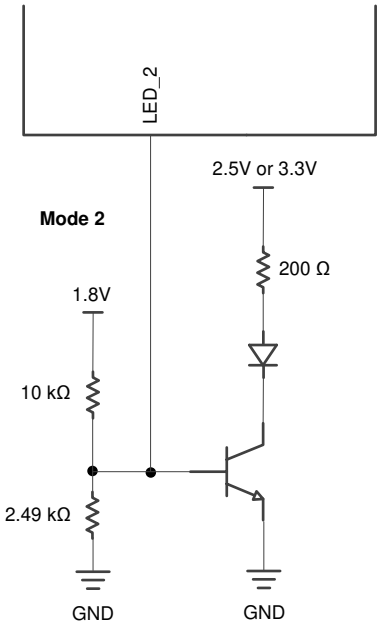

Figure 23. LED Operation From 1.8-V I/O VDD Supply

8.5.4 PHY Address Configuration

The DP83867 can be set to respond to any of 16 possible PHY addresses through strap pins. The information is latched into the device at a device power up or hardware reset. Each DP83867 or port sharing an MDIO bus in a system must have a unique physical address. The DP83867 supports PHY address strapping values 0 (<0000>) through 15 (<1111>).

For further detail relating to the latch-in timing requirements of the PHY Address pins, as well as the other hardware configuration pins, refer to *Reset Operation*.

Based on the default strap configuration of PHY_ADD[3:0], the DP83867 PHY address initializes to 0x00 without any external strap configuration.

Refer to Figure 24 for an example of a PHY address connection to external components. In this example, the pins are configured as follows: RX_D2 = Strap Mode 3 and RX_D0 = Strap Mode 2. Therefore, the PHY address strapping results in address 1001 (09h).

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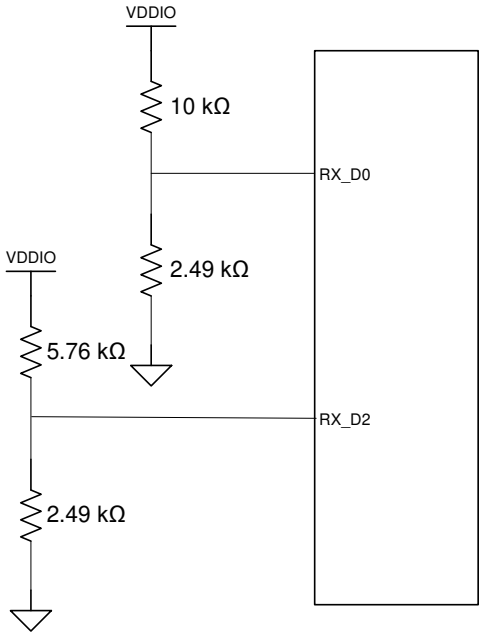

Figure 24. PHY Address Strapping Example

When operating in SGMII mode, dummy straps must be added to provide a balanced load for the SGMII differential pairs. Therefore, for SGMII applications with the straps shown in Figure 24, the corresponding connections for RX_D1 and RX_D3 are shown in Figure 25.

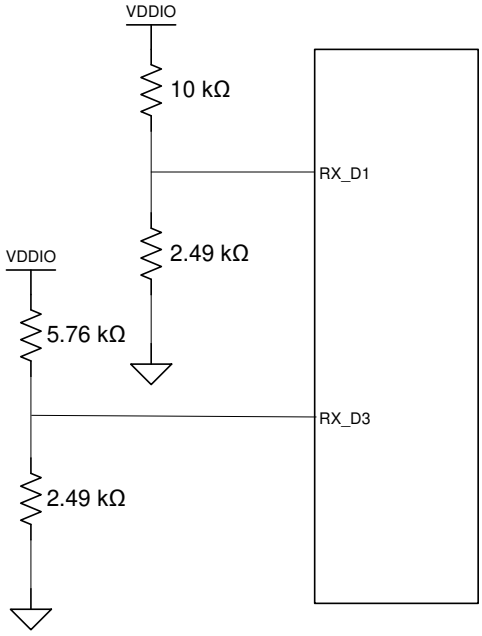

Figure 25. PHY Address Strapping Example for SGMII

8.5.5 Reset Operation

The DP83867 includes an internal power-on-reset (POR) function and therefore does not need to be explicitly reset for normal operation after power up. If required during normal operation, the device can be reset by a hardware or software reset.

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8.5.5.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse, with a duration of at least 1 μs, to the RESET_N pin. This resets the device such that all registers are reinitialized to default values and the hardware configuration values are re-latched into the device (similar to the power up or reset operation).

8.5.5.2 IEEE Software Reset

An IEEE registers software reset is accomplished by setting the reset bit (bit 15) of the BMCR register (address 0x0000). This bit resets the IEEE-defined standard registers.

8.5.5.3 Global Software Reset

A global software reset is accomplished by setting bit 15 of register CTRL (address 0x001F) to 1. This bit resets all the internal circuits in the PHY including IEEE-defined registers and all the extended registers. The global software reset resets the device such that all registers are reset to default values and the hardware configuration values are maintained.

8.5.5.4 Global Software Restart

A global software restart is accomplished by setting bit 14 of register CTRL (0x001F) to 1. This action resets all the PHY circuits except the registers in the Register File.

8.5.5.5 PCS Restart

A PCS reset is accomplished by setting bit 15 of register MMD3_PCS_CTRL (MMD3 register 0x0000). Setting this bit resets the MMD3 register. This bit subsequently cause a soft reset through the BMCR RESET bit (bit 15 of register address 0x0000).

8.5.6 Power-Saving Modes

DP83867 supports 4 power saving modes. The details are provided below.

8.5.6.1 IEEE Power Down

The PHY is powered down but access to the PHY through MDIO-MDC pins is retained. This mode can be activated by asserting external PWDN pin or by setting bit 11 of BMCR (Register 0x00).

The PHY can be taken out of this mode by a power cycle, software reset, or by clearing the bit 11 in BMCR register. However, the external PWDN pin should be deasserted. If the PWDN pin is kept asserted then the PHY remains in power down.

8.5.6.2 Deep Power-Down Mode

This same as IEEE power down but the XI pad is also turned off. This mode can be activated by asserting the external PWDN pin or by setting bit 11 of BMCR (Register 0x00). Before activating this mode, it is required to set bit 7 for PHYCR (Register 0x10).

The PHY can be taken out of this mode by a power cycle, software reset or by clearing the bit 11 in BMCR register. However, the external PWDN pin should be de-asserted. If the PWDN pin is kept asserted then the PHY remains in power down.

8.5.6.3 Active Sleep

In this mode, all the digital and analog blocks are powered down. The PHY is automatically powered up when a link partner is detected. This mode is useful for saving power when the link partner is down or inactive, but PHY cannot be powered down. In Active Sleep mode, the PHY still routinely sends NLP to the link partner. This mode can be active by writing binary 10 to bits [9:8] for PHYCR (Register 0x10).

8.5.6.4 Passive Sleep

This is just like Active sleep except the PHY does not send NLP. This mode can be activated by writing binary 11 to bits [9:8] PHYCR (Register 0x10).

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8.6 Register Maps

In the register definitions under the 'Default' heading, the following definitions hold true:

RW Read Write access

SC Register sets on event occurrence and Self-Clears when event ends

RW/SC ReadWrite access/Self Clearing bit

RO Read Only access

COR COR = Clear On Read

RO/COR Read Only, Clear On Read

RO/P Read Only, Permanently set to a default value

LL Latched Low and held until read, based upon the occurrence of the corresponding event

LH Latched High and held until read, based upon the occurrence of the corresponding event

Strap Default value loaded from bootstrap pin after reset

8.6.1 Basic Mode Control Register (BMCR)

Table 10. Basic Mode Control Register (BMCR), Address 0x0000

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESET	0, RW/SC	Reset: 1 = Initiate software Reset / Reset in Process. 0 = Normal operation. This bit, which is self-clearing, returns a value of one until the reset process is complete. The configuration is restrapped.
14	LOOPBACK	0, RW	Loopback: 1 = Loopback enabled. 0 = Normal operation. The loopback function enables MAC transmit data to be routed to the MAC receive data path. Setting this bit may cause the descrambler to lose synchronization and produce a 500-µs dead time before any valid data will appear at the MII receive outputs.
13	SPEED SELECTION LSB	0, RW	Speed Select (Bits 6, 13): When auto-negotiation is disabled writing to this bit allows the port speed to be selected. 11 = Reserved 10 = 1000 Mbps 1 = 100 Mbps 0 = 10 Mbps
12	AUTO-NEGOTIATION ENABLE	Strap, RW	Auto-Negotiation Enable: Strap controls initial value at reset. 1 = Auto-Negotiation Enabled - bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled - bits 8 and 13 determine the port speed and duplex mode.
11	POWER DOWN	0, RW	Power Down: 1 = Power down. 0 = Normal operation. Setting this bit powers down the PHY. Only the register block is enabled during a power down condition. This bit is ORd with the input from the PWRDOWN_INT pin. When the active low PWRDOWN_INT pin is asserted, this bit will be set.

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Register Maps (continued)

Table 10. Basic Mode Control Register (BMCR), Address 0x0000 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
10	ISOLATE	0, RW	Isolate: 1 = Isolates the Port from the MII with the exception of the serial management. 0 = Normal operation.
9	RESTART AUTO-NEGOTIATION	0, RW/SC	Restart Auto-Negotiation: 1 = Restart Auto-Negotiation. Reinitiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal operation.
8	DUPLEX MODE	Strap, RW	Duplex Mode: When auto-negotiation is disabled writing to this bit allows the port Duplex capability to be selected. 1 = Full Duplex operation. 0 = Half Duplex operation.
7	COLLISION TEST	0, RW	Collision Test: 1 = Collision test enabled. 0 = Normal operation. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN within 512-bit times. The COL signal will be deasserted within 4-bit times in response to the deassertion of TX_EN.
6	SPEED SELECTION MSB	1, RW	Speed Select: See description for bit 13.
5:0	RESERVED	0 0000, RO	RESERVED: Write ignored, read as 0.

8.6.2 Basic Mode Status Register (BMSR)

Table 11. Basic Mode Status Register (BMSR), Address 0x0001

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100BASE-T4	0, RO/P	100BASE-T4 Capable: 0 = Device not able to perform 100BASE-T4 mode.
14	100BASE-TX FULL DUPLEX	1, RO/P	100BASE-TX Full Duplex Capable: 1 = Device able to perform 100BASE-TX in full duplex mode.
13	100BASE-TX HALF DUPLEX	1, RO/P	100BASE-TX Half Duplex Capable: 1 = Device able to perform 100BASE-TX in half duplex mode.
12	10BASE-Te FULL DUPLEX	1, RO/P	10BASE-Te Full Duplex Capable: 1 = Device able to perform 10BASE-Te in full duplex mode.
11	10BASE-Te HALF DUPLEX	1, RO/P	10BASE-Te Half Duplex Capable: 1 = Device able to perform 10BASE-Te in half duplex mode.
10	100BASE-T2 FULL DUPLEX	0, RO/P	100BASE-T2 Full Duplex Capable: 0 = Device not able to perform 100BASE-T2 in full duplex mode.
9	100BASE-T2 HALF DUPLEX	0, RO/P	100BASE-T2 Half Duplex Capable: 0 = Device not able to perform 100BASE-T2 in half duplex mode.
8	EXTENDED STATUS	1, RO/P	1000BASE-T Extended Status Register: 1 = Device supports Extended Status Register 0x0F.
7	RESERVED	0, RO	RESERVED: Write as 0, read as 0.
6	MF PREAMBLE SUPPRESSION	1, RO/P	Preamble Suppression Capable: 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. 0 = Normal management operation.
5	AUTO-NEGOTIATION COMPLETE	0, RO	Auto-Negotiation Complete: 1 = Auto-Negotiation process complete. 0 = Auto-Negotiation process not complete.
4	REMOTE FAULT	0, RO/LH	Remote Fault: 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far-End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected.
3	AUTO-NEGOTIATION ABILITY	1, RO/P	Auto Negotiation Ability: 1 = Device is able to perform Auto-Negotiation. 0 = Device is not able to perform Auto-Negotiation.
2	LINK STATUS	0, RO/LL	Link Status: 1 = Valid link established. 0 = Link not established. The criteria for link validity is implementation specific. The occurrence of a link failure condition will causes the Link Status bit to clear. Once cleared, this bit may only be set by establishing a good link condition and a read through the management interface.

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Table 11. Basic Mode Status Register (BMSR), Address 0x0001 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
1	JABBER DETECT	0, RO/LH	Jabber Detect: This bit only has meaning in 10-Mbps mode. 1 = Jabber condition detected. 0 = No Jabber. This bit is implemented with a latching function, such that the occurrence of a jabber condition causes it to set until it is cleared by a read to this register by the management interface or by a reset.
0	EXTENDED CAPABILITY	1, RO/P	Extended Capability: 1 = Extended register capabilities. 0 = Basic register set capabilities only.

8.6.3 PHY Identifier Register #1 (PHYIDR1)

The PHY Identifier Registers #1 and #2 together form a unique identifier for the DP83867. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. Texas Instruments' IEEE assigned OUI is 080028h.

Table 12. PHY Identifier Register #1 (PHYIDR1), Address 0x0002

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	OUI_MSB	0010 0000 0000 0000, RO/P	OUI Most Significant Bits: Bits 3 to 18 of the OUI (080028h,) are stored in bits 15 to 0 of this register. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

8.6.4 PHY Identifier Register #2 (PHYIDR2)

Table 13. PHY Identifier Register #2 (PHYIDR2), Address 0x0003

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	OUI_LSB	1010 00, RO/P	OUI Least Significant Bits: Bits 19 to 24 of the OUI (080028h) are mapped from bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	10 0011, RO/P	Vendor Model Number: The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	0001, RO/P	Model Revision Number: Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

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8.6.5 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-Negotiation. Any writes to this register prior to completion of Auto-Negotiation (as indicated in the Basic Mode Status Register (address 01h) Auto-Negotiation Complete bit, BMSR[5]) should be followed by a renegotiation. This will ensure that the new values are properly used in the Auto-Negotiation.

Table 14. Auto-Negotiation Advertisement Register (ANAR), Address 0x0004

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	Next Page Indication: 0 = Next Page Transfer not desired. 1 = Next Page Transfer desired.
14	RESERVED	0, RO/P	RESERVED by IEEE: Writes ignored, Read as 0.
13	RF	0, RW	Remote Fault: 1 = Advertises that this device has detected a Remote Fault. 0 = No Remote Fault detected.
12	RESERVED	0, RW	RESERVED for Future IEEE use: Write as 0, Read as 0
11	ASM_DIR	0, RW	Asymmetric PAUSE Support for Full Duplex Links: The ASM_DIR bit indicates that asymmetric PAUSE is supported. Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12]. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0 = No MAC based full duplex flow control.
10	PAUSE	0, RW	PAUSE Support for Full Duplex Links: The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12]. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0 = No MAC based full duplex flow control.
9	T4	0, RO/P	100BASE-T4 Support: 1 = 100BASE-T4 is supported by the local device. 0 = 100BASE-T4 not supported.
8	TX_FD	Strap, RW	100BASE-TX Full Duplex Support: 1 = 100BASE-TX Full Duplex is supported by the local device. 0 = 100BASE-TX Full Duplex not supported.
7	TX	Strap, RW	100BASE-TX Support: 1 = 100BASE-TX is supported by the local device. 0 = 100BASE-TX not supported.
6	10_FD	Strap, RW	10BASE-Te Full Duplex Support: 1 = 10BASE-Te Full Duplex is supported by the local device. 0 = 10BASE-Te Full Duplex not supported.

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Table 14. Auto-Negotiation Advertisement Register (ANAR), Address 0x0004 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
5	10BASETe_EN	Strap, RW	10BASE-Te Support: 1 = 10BASE-Te is supported by the local device. 0 = 10BASE-Te not supported.
4:0	SELECTOR	0 0001, RW	Protocol Selection Bits: These bits contain the binary encoded protocol selector supported by this port. <00001> indicates that this device supports IEEE 802.3u.

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8.6.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page)

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation. The content changes after the successful Auto-Negotiation if Next pages are supported.

Table 15. Auto-Negotiation Link Partner Ability Register (ANLPAR), Address 0x0005

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	Next Page Indication: 0 = Link Partner does not desire Next Page Transfer. 1 = Link Partner desires Next Page Transfer.
14	ACK	0, RO	Acknowledge: 1 = Link Partner acknowledges reception of the ability data word. 0 = Not acknowledged. The Auto-Negotiation state machine will automatically control this bit based on the incoming FLP bursts.
13	RF	0, RO	Remote Fault: 1 = Remote Fault indicated by Link Partner. 0 = No Remote Fault indicated by Link Partner.
12	RESERVED	0, RO	RESERVED for Future IEEE use: Write as 0, read as 0.
11	ASM_DIR	0, RO	ASYMMETRIC PAUSE: 1 = Asymmetric pause is supported by the Link Partner. 0 = Asymmetric pause is not supported by the Link Partner.
10	PAUSE	0, RO	PAUSE: 1 = Pause function is supported by the Link Partner. 0 = Pause function is not supported by the Link Partner.
9	T4	0, RO	100BASE-T4 Support: 1 = 100BASE-T4 is supported by the Link Partner. 0 = 100BASE-T4 not supported by the Link Partner.
8	TX_FD	0, RO	100BASE-TX Full Duplex Support: 1 = 100BASE-TX Full Duplex is supported by the Link Partner. 0 = 100BASE-TX Full Duplex not supported by the Link Partner.
7	TX	0, RO	100BASE-TX Support: 1 = 100BASE-TX is supported by the Link Partner. 0 = 100BASE-TX not supported by the Link Partner.
6	10_FD	0, RO	10BASE-Te Full Duplex Support: 1 = 10BASE-Te Full Duplex is supported by the Link Partner. 0 = 10BASE-Te Full Duplex not supported by the Link Partner.
5	10	0, RO	10BASE-Te Support: 1 = 10BASE-Te is supported by the Link Partner. 0 = 10BASE-Te not supported by the Link Partner.
4:0	SELECTOR	0 0000, RO	Protocol Selection Bits: Link Partner's binary encoded protocol selector.

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8.6.7 Auto-Negotiate Expansion Register (ANER)

This register contains additional Local Device and Link Partner status information.

Table 16. Auto-Negotiate Expansion Register (ANER), Address 0x0006

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:7	RESERVED	0, RO	RESERVED: Writes ignored, Read as 0.
6	RX_NEXT_PAGE_LOC_ABLE	1, RO	Receive Next Page Location Able: 1 = Received Next Page storage location is specified by bit 6.5. 0 = Received Next Page storage location is not specified by bit 6.5.
5	RX_NEXT_PAGE_STOR_LOC	1, RO	Receive Next Page Storage Location: 1 = Link Partner Next Pages are stored in register 8. 0 = Link Partner Next Pages are stored in register 5.
4	PDF	0, RO	Parallel Detection Fault: 1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected.
3	LP_NP_ABLE	0, RO	Link Partner Next Page Able: 1 = Link Partner does support Next Page. 0 = Link Partner does not support Next Page.
2	NP_ABLE	1, RO/P	Next Page Able: 1 = Indicates local device is able to send additional Next Pages.
1	PAGE_RX	0, RO/COR	Link Code Word Page Received: 1 = Link Code Word has been received, cleared on a read. 0 = Link Code Word has not been received.
0	LP_AN_ABLE	0, RO	Link Partner Auto-Negotiation Able: 1 = Indicates that the Link Partner supports Auto-Negotiation. 0 = Indicates that the Link Partner does not support Auto-Negotiation.

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8.6.8 Auto-Negotiation Next Page Transmit Register (ANNPTR)

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 17. Auto-Negotiation Next Page Transmit Register (ANNPTR), Address 0x0007

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	Next Page Indication: 0 = No other Next Page Transfer desired. 1 = Another Next Page desired.
14	ACK	0, RO	Acknowledge: 1 = Acknowledge reception of link code word 0 = Do not acknowledge of link code word.
13	MP	1, RW	Message Page: 1 = Current page is a Message Page. 0 = Current page is an Unformatted Page.
12	ACK2	0, RW	Acknowledge2: 1 = Will comply with message. 0 = Cannot comply with message. Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	TOG_TX	0, RO	Toggle: 1 = Value of toggle bit in previously transmitted Link Code Word was 0. 0 = Value of toggle bit in previously transmitted Link Code Word was 1. Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	000 0000 0001, RW	Code: This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page", as defined in Annex 28C of IEEE 802.3u. Otherwise, the code shall be interpreted as an "Unformatted Page", and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

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8.6.9 Auto-Negotiation Next Page Receive Register (ANNPRR)

This register contains the next page information sent by the Link Partner during Auto-Negotiation.

Table 18. Auto-Negotiation Next Page Transmit Register (ANNPTR), Address 0x0008

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	Next Page Indication: 0 = No other Next Page Transfer desired by the link partner. 1 = Another Next Page desired by the link partner.
14	ACK	0, RO	Acknowledge: 1 = Acknowledge reception of link code word by the link partner. 0 = Link partner does not acknowledge reception of link code word.
13	MP	1, RW	Message Page: 1 = Received page is a Message Page. 0 = Received page is an Unformatted Page.
12	ACK2	0, RW	Acknowledge2: 1 = Link partner sets the ACK2 bit. 0 = Link partner coes not set the ACK2 bit. Acknowledge2 is used by the next page function to indicate that link partner has the ability to comply with the message received.
11	TOG_TX	0, RO	Toggle: 1 = Value of toggle bit in previously transmitted Link Code Word was 0. 0 = Value of toggle bit in previously transmitted Link Code Word was 1. Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	000 0000 0001, RW	Code: This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page", as defined in Annex 28C of IEEE 802.3u. Otherwise, the code shall be interpreted as an "Unformatted Page", and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

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8.6.10 1000BASE-T Configuration Register (CFG1)

Table 19. Configuration Register 1 (CFG1), Address 0x0009

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	TEST MODE	000, RW	Test Mode Select: 111 = Test Mode 7 - Repetitive {Pulse, 63 zeros} 110 = Test Mode 6 - Repetitive 0001 sequence 101 = Test Mode 5 - Scrambled MLT3 Idles 100 = Test Mode 4 - Transmit Distortion Test 011 = Test Mode 3 - Transmit Jitter Test (Slave Mode) 010 = Test Mode 2 - Transmit Jitter Test (Master Mode) 001 = Test Mode 1 - Transmit Waveform Test 000 = Normal Mode
12	MASTER / SLAVE MANUAL CONFIGURATION	0, RW	Enable Manual Master / Slave Configuration: 1 = Enable Manual Master/Slave Configuration control. 0 = Disable Manual Master/Slave Configuration control. Using the manual configuration feature may prevent the PHY from establishing link in 1000Base-T mode if a conflict with the link partner's setting exists.
11	MASTER / SLAVE CONFIGURATION VALUE	0, RW	Manual Master / Slave Configuration Value: 1 = Set PHY as MASTER when register 09h bit 12 = 1. 0 = Set PHY as SLAVE when register 09h bit 12 = 1. Using the manual configuration feature may prevent the PHY from establishing link in 1000Base-T mode if a conflict with the link partner's setting exists.
10	PORT TYPE	0, RW	Advertise Device Type: Multi or single port: 1 = Multi-port device. 0 = Single-port device.
9	1000BASE-T FULL DUPLEX	RGZ: 1, RW PAP: Strap, RW	Advertise 1000BASE-T Full Duplex Capable: 1 = Advertise 1000Base-T Full Duplex ability. 0 = Do not advertise 1000Base-T Full Duplex ability.
8	1000BASE-T HALF DUPLEX	1, RW	Advertise 1000BASE-T Half Duplex Capable: 1 = Advertise 1000Base-T Half Duplex ability. 0 = Do not advertise 1000Base-T Half Duplex ability.
7	TDR AUTO RUN	0, RW	Automatic TDR on Link Down: 1 = Enable execution of TDR procedure after link down event. 0 = Disable automatic execution of TDR.
6:0	RESERVED	000 0000, RO	RESERVED: Write ignored, read as 0.

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8.6.11 Status Register 1 (STS1)

Table 20. Status Register 1 (STS1) Address 0x000A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	MASTER / SLAVE CONFIGURATION FAULT	0, RO, LH, COR	Master / Slave Manual Configuration Fault Detected: 1 = Manual Master/Slave Configuration fault detected. 0 = No Manual Master/Slave Configuration fault detected.
14	MASTER / SLAVE CONFIGURATION RESOLUTION	0, RO	Master / Slave Configuration Results: 1 = Configuration resolved to MASTER. 0 = Configuration resolved to SLAVE.
13	LOCAL RECEIVER STATUS	0, RO	Local Receiver Status: 1 = Local receiver is OK. 0 = Local receiver is not OK.
12	REMOTE RECEIVER STATUS	0, RO	Remote Receiver Status: 1 = Remote receiver is OK. 0 = Remote receiver is not OK.
11	1000BASE-T FULL DUPLEX	0, RO	Link Partner 1000BASE-T Full Duplex Capable: 1 = Link Partner capable of 1000Base-T Full Duplex. 0 = Link partner not capable of 1000Base-T Full Duplex.
10	1000BASE-T HALF DUPLEX	0, RO	Link Partner 1000BASE-T Half Duplex Capable: 1 = Link Partner capable of 1000Base-T Half Duplex. 0 = Link partner not capable of 1000Base-T Half Duplex.
9:8	RESERVED	00, RO	RESERVED by IEEE: Writes ignored, read as 0.
7:0	IDLE ERROR COUNTER	0000 0000, RO, COR	1000BASE-T Idle Error Counter

8.6.12 Extended Register Addressing

REGCR (0x000D) and ADDAR (0x000E) allow read/write access to the extended register set (addresses above 0x001F) using indirect addressing.

- **REGCR [15:14]** = 00: A write to ADDAR modifies the extended register set address register. This address register must be initialized to access any of the registers within the extended register set.
- •**REGCR [15:14]** = 01: A read or write to ADDAR operates on the register within the extended register set selected (pointed to) by the value in the address register. The address register contents (pointer) remain unchanged.
- **REGCR [15:14]** = 10: A read or write to ADDAR operates on the register within the extended register set selected (pointed to) by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- **REGCR [15:14]** = 11: A read or write to ADDAR operates on the register within the extended register set selected (pointed to) by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

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8.6.12.1 Register Control Register (REGCR)

This register is the MDIO Manageable MMD access control. In general, register REGCR (4:0) is the device address DEVAD that directs any accesses of the ADDAR (0x000E) register to the appropriate MMD. REGCR also contains selection bits for auto increment of the data register. This register contains the device address to be written to access the extended registers. Write 0x1F into bits 4:0 of this register. REGCR also contains selection bits (15:14) for the address auto-increment mode of ADDAR.

Table 21. Register Control Register (REGCR), Address 0x000D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	Function	0, RW	00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13:5	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
4:0	DEVAD	0, RW	Device Address: In general, these bits [4:0] are the device address DEVAD that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. Specifically, the DP83867 uses the vendor specific DEVAD [4:0] = 11111 for accesses. All accesses through registers REGCR and ADDAR should use this DEVAD. Transactions with other DEVAD are ignored.

8.6.12.2 Address or Data Register (ADDAR)

This register is the address/data MMD register. ADDAR is used in conjunction with REGCR register (0x000D) to provide the access by indirect read/write mechanism to the extended register set.

Table 22. Address or Data Register (ADDAR) address 0x000E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	Address / Data	0, RW	If REGCR register 15:14 = 00, holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data register

8.6.13 1000BASE-T Status Register (1KSCR)

Table 23. 1000BASE-T Status Register (1KSCR) address 0x000F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	1000BASE-X FULL DUPLEX	0, RO/P	1000BASE-X Full Duplex Support: 1 = 1000BASE-X Full Duplex is supported by the local device. 0 = 1000BASE-X Full Duplex is not supported by the local device.
14	1000BASE-X HALF DUPLEX	0, RO/P	1000BASE-X Half Duplex Support: 1 = 1000BASE-X Half Duplex is supported by the local device. 0 = 1000BASE-X Half Duplex is not supported by the local device.
13	1000BASE-T FULL DUPLEX	1, RO/P	1000BASE-T Full Duplex Support: 1 = 1000BASE-T Full Duplex is supported by the local device. 0 = 1000BASE-T Full Duplex is not supported by the local device.
12	1000BASE-T HALF DUPLEX	1, RO/P	1000BASE-T Half Duplex Support: 1 = 1000BASE-T Half Duplex is supported by the local device. 0 = 1000BASE-T Half Duplex is not supported by the local device.
11:0	RESERVED	00, RO	RESERVED by IEEE: Writes ignored, read as 0.

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8.6.14 PHY Control Register (PHYCR)

Table 24. PHY Control Register (PHYCR), Address 0x0010

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	TX FIFO Depth	1, RW	TX FIFO Depth: 11 = 8 bytes/nibbles (1000Mbps/Other Speeds) 10 = 6 bytes/nibbles (1000Mbps/Other Speeds) 01 = 4 bytes/nibbles (1000Mbps/Other Speeds) 00 = 3 bytes/nibbles (1000Mbps/Other Speeds) Note: FIFO is enabled only in the following modes: 1000BaseT + GMII 10BaseT/100BaseTX/1000BaseT + SGMII
13:12	RX FIFO Depth	1, RW	RX FIFO Depth: 11 = 8 bytes/nibbles (1000 Mbps/Other Speeds) 10 = 6 bytes/nibbles (1000 Mbps/Other Speeds) 01 = 4 bytes/nibbles (1000 Mbps/Other Speeds) 00 = 3 bytes/nibbles (1000 Mbps/Other Speeds) Note: FIFO is enabled only in SGMII
11	SGMII_EN	Strap, RW	SGMII Enable: 1 = Enable SGMII 0 = Disable SGMII
10	FORCE_LINK_GOOD	0, RW	Force Link Good: 1 = Force link good according to the selected speed. 0 = Normal operation
9:8	POWER_SAVE_MODE	0, RW	Power-Saving Modes: 11 = Passive Sleep mode: Power down all digital and analog blocks. 10 =Active Sleep mode: Power down all digital and analog blocks. Automatic power-up is performed when link partner is detected. Link pulses are transmitted approximately once per 1.4 Sec in this mode to wake up any potential link partner. 01 = IEEE mode: power down all digital and analog blocks. Note: If DISABLE_CLK_125 (bit [4]of this register) is set to zero, the PLL is also powered down. 00 = Normal mode
7	DEEP_POWER_DOWN_EN	0, RW	Deep power-down mode enable 1 = When power down is initiated through assertion of the external power-down pin or through the POWER_DOWN bit in the BMCR, the device enters a deep power-down mode. 0 = Normal operation.
6:5	MDI_CROSSOVER	RGZ: 10, RW PAP: Strap, RW	MDI Crosssover Mode: 1x = Enable automatic crossover 01 = Manual MDI-X configuration 00 = Manual MDI configuration
4	DISABLE_CLK_125	0, RW	Disable 125MHz Clock: This bit may be used in conjunction with POWER_SAVE_MODE (bits 9:8 of this register). 1 = Disable CLK125. 0 = Enable CLK125.
3	RESERVED	1, RO	RESERVED: Writes ignored, read as 1.
2	STANDBY_MODE	0, RW	Standby Mode: 1 = Enable standby mode. Digital and analog circuitry are powered up, but no link can be established. 0 = Normal operation.
1	LINE_DRIVER_INV_EN	0, RW	Line Driver Inversion Enable: 1 = Invert Line Driver Transmission. 0 = Normal operation.
0	DISABLE_JABBER	0, RW	Disable Jabber 1 = Disable Jabber function. 0 = Enable Jabber function.

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8.6.15 PHY Status Register (PHYSTS)

This register provides a single location within the register set for quick access to commonly accessed information.

Table 25. PHY Status Register (PHYSTS), Address 0x0011

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	SPEED SELECTION	0, RO	Speed Select Status: These two bits indicate the speed of operation as determined by Auto-Negotiation or as set by manual configuration. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	DUPLEX MODE	0, RO	Duplex Mode Status: 1 = Full Duplex 0 = Half Duplex.
12	PAGE RECEIVED	0, RO, LH, COR	Page Received: This bit is latched high and will be cleared upon a read. 1 = Page received. 0 = No page received.
11	SPEED DUPLEX RESOLVED	0, RO	Speed Duplex Resolution Status: 1 = Auto-Negotiation has completed or is disabled. 0 = Auto-Negotiation is enabled and has not completed.
10	LINK_STATUS	0, RO	Link Status: 1 = Link is up. 0 = Link is down.
9	MDI_X_MODE_CD	0, RO	MDI/MDIX Resolution Status for C and D Line Driver Pairs: 1 = Resolved as MDIX 0 = Resolved as MDI.
8	MDI_X_MODE_AB	0, RO	MDI/MDIX Resolution Status for A and B Line Driver Pairs: 1 = Resolved as MDIX 0 = Resolved as MDI.
7	SPEED_OPT_STATUS	0, RO	Speed Optimization Status: 1 = Auto-Negotiation is currently being performed with Speed Optimization masking 1000BaseT abilities (Valid only during Auto-Negotiation). 0 = Auto-Negotiation is currently being performed without Speed Optimization.
6	SLEEP_MODE	0, RO	Sleep Mode Status: 1 = Device currently in sleep mode. 0 = Device currently in active mode.
5:2	WIRE_CROSS	0, RO	Crossed Wire Indication: Indicates channel polarity in 1000BASE-T linked status. Bits [5:2] correspond to channels [D,C,B,A], respectively. 1 = Channel polarity is reversed. 0 = Channel polarity is normal.

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Table 25. PHY Status Register (PHYSTS), Address 0x0011 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
1	POLARITY STATUS	1, RO	10BASE-Te Polarity Status: 1 = Correct Polarity detected. 0 = Inverted Polarity detected.
0	JABBER DETECT	0, RO	Jabber Detect: This bit only has meaning in 10 Mbps mode. This bit is a duplicate of the Jabber Detect bit in the BMSR register, except that it is not cleared upon a read of the PHYSTS register. 1 = Jabber condition detected. 0 = No Jabber.

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8.6.16 MII Interrupt Control Register (MICR)

This register implements the Interrupt PHY Specific Control register. The individual interrupt events must be enabled by setting bits in the MII Interrupt Control Register (MICR). If the corresponding enable bit in the register is set, an interrupt is generated if the event occurs.

Table 26. MII Interrupt Control Register (MICR), Address 0x0012

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	AUTONEG_ERR_INT_EN	0, RW	Enable Auto-Negotiation Error Interrupt: 1 = Enable Auto-Negotiation Error interrupt. 0 = Disable Auto-Negotiation Error interrupt.
14	SPEED_CHNG_INT_EN	0, RW	Enable Speed Change Interrupt: 1 = Enable Speed Change interrupt. 0 = Disable Speed Change interrupt.
13	DUPLEX_MODE_CHNG_INT_EN	0, RW	Enable Duplex Mode Change Interrupt: 1 = Enable Duplex Mode Change interrupt. 0 = Disable Duplex Mode Change interrupt.
12	PAGE_RECEIVED_INT_EN	0, RW	Enable Page Received Interrupt: 1 = Enable Page Received Interrupt. 0 = Disable Page Received Interrupt.
11	AUTONEG_COMP_INT_EN	0, RW	Enable Auto-Negotiation Complete Interrupt: 1 = Enable Auto-Negotiation Complete Interrupt. 0 = Disable Auto-Negotiation Complete Interrupt.
10	LINK_STATUS_CHNG_INT_EN	0, RW	Enable Link Status Change Interrupt: 1 = Enable Link Status Change interrupt. 0 = Disable Link Status Change interrupt.
9	RESERVED	0, RO	RESERVED
8	FALSE_CARRIER_INT_EN	0, RW	Enable False Carrier Interrupt: 1 = Enable False Carrier interrupt. 0 = Disable False Carrier interrupt.
7	RESERVED	0, RO	RESERVED
6	MDI_CROSSOVER_CHNG_INT_EN	0, RW	Enable MDI Crossover Change Interrupt: 1 = Enable MDI Crossover Change interrupt. 0 = Disable MDI Crossover Change interrupt.
5	SPEED_OPT_EVENT_INT_EN	0, RW	Enable Speed Optimization Event Interrupt: 1 = Enable Speed Optimization Event Interrupt. 0 = Disable Speed Optimization Event Interrupt.
4	SLEEP_MODE_CHNG_INT_EN	0, RW	Enable Sleep Mode Change Interrupt: 1 = Enable Sleep Mode Change Interrupt. 0 = Disable Sleep Mode Change Interrupt.
3	WOL_INT_EN	0, RW	Enable Wake-on-LAN Interrupt: 1 = Enable Wake-on-LAN Interrupt. 0 = Disable Wake-on-LAN Interrupt.

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Table 26. MII Interrupt Control Register (MICR), Address 0x0012 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
2	XGMII_ERR_INT_EN	0, RW	Enable xGMII Error Interrupt: 1 = Enable xGMII Error Interrupt. 0 = Disable xGMII Error Interrupt.
1	POLARITY_CHNG_INT_EN	0, RW	Enable Polarity Change Interrupt: 1 = Enable Polarity Change interrupt. 0 = Disable Polarity Change interrupt.
0	JABBER_INT_EN	0, RW	Enable Jabber Interrupt: 1 = Enable Jabber interrupt. 0 = Disable Jabber interrupt.

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8.6.17 Interrupt Status Register (ISR)

This register contains event status for the interrupt function. If an event has occurred since the last read of this register, the corresponding status bit will be set. The status indications in this register will be set even if the interrupt is not enabled.

Table 27. Interrupt Status Register (ISR), Address 0x0013

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	AUTONEG_ERR_INT	0, RO, LH, COR	Auto-Negotiation Error Interrupt: 1 = Auto-Negotiation Error interrupt is pending and is cleared by the current read. 0 = No Auto-Negotiation Error interrupt.
14	SPEED_CHNG_INT	0, RO, LH, COR	Speed Change Interrupt: 1 = Speed Change interrupt is pending and is cleared by the current read. 0 = No Speed Change interrupt.
13	DUPLEX_MODE_CHNG_INT	0, RO, LH, COR	Duplex Mode Change Interrupt: 1 = Duplex Mode Change interrupt is pending and is cleared by the current read. 0 = No Duplex Mode Change interrupt.
12	PAGE_RECEIVED_INT	0, RO, LH, COR	Page Received Interrupt: 1 = Page Received Interrupt is pending and is cleared by the current read. 0 = No Page Received Interrupt is pending.
11	AUTONEG_COMP_INT	0, RO, LH, COR	Auto-Negotiation Complete Interrupt: 1 = Auto-Negotiation Complete Interrupt is pending and is cleared by the current read. 0 = No Auto-Negotiation Complete Interrupt is pending.
10	LINK_STATUS_CHNG_INT	0, RO, LH, COR	Link Status Change Interrupt: 1 = Link Status Change interrupt is pending and is cleared by the current read. 0 = No Link Status Change interrupt is pending.
9	RESERVED	0, RO	RESERVED
8	FALSE_CARRIER_INT	0, RO, LH, COR	False Carrier Interrupt: 1 = False Carrier interrupt is pending and is cleared by the current read. 0 = No False Carrier interrupt is pending.
7	RESERVED	0, RO	RESERVED
6	MDI_CROSSOVER_CHNG_INT	0, RO, LH, COR	MDI Crossover Change Interrupt: 1 = MDI Crossover Change interrupt is pending and is cleared by the current read. 0 = No MDI Crossover Change interrupt is pending.

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Table 27. Interrupt Status Register (ISR), Address 0x0013 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
5	SPEED_OPT_EVENT_INT	0, RO, LH, COR	Speed Optimization Event Interrupt: 1 = Speed Optimization Event Interrupt is pending and is cleared by the current read. 0 = No Speed Optimization Event Interrupt is pending.
4	SLEEP_MODE_CHNG_INT	0, RO, LH, COR	Sleep Mode Change Interrupt: 1 = Sleep Mode Change Interrupt is pending and is cleared by the current read. 0 = No Sleep Mode Change Interrupt is pending.
3	WOL_INT	0, RO, LH, COR	Wake-on-LAN Interrupt: 1 = Wake-on-LAN Interrupt is pending. 0 = No Wake-on-LAN Interrupt is pending.
2	XGMII_ERR_INT (1)	0, RO, LH, COR	xGMII Error Interrupt: 1 = xGMII Error Interrupt is pending and is cleared by the current read. 0 = No xGMII Error Interrupt is pending.
1	POLARITY_CHNG_INT	0, RO, LH, COR	Polarity Change Interrupt: 1 = Polarity Change interrupt is pending and is cleared by the current read. 0 = No Polarity Change interrupt is pending.
0	JABBER_INT	0, RO, LH, COR	Jabber Interrupt: 1 = Jabber interrupt is pending and is cleared by the current read. 0 = No Jabber interrupt is pending.

(1) xGMII: RGMII or SGMII

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8.6.18 Configuration Register 2 (CFG2)

Table 28. Configuration Register 2 (CFG2), Address 0x0014

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
13	INTERRUPT_POLARITY	1, RW	Configure Interrupt Polarity: 1 = Interrupt pin is active low. 0 = Interrupt pin is active high.
12	RESERVED	0, RO	RESERVED
11:10	SPEED_OPT_ATTEMPT_CNT	10, RO	Speed Optimization Attempt Count: Selects the number of 1000BASE-T link establishment attempt failures prior to performing Speed Optimization. 11 = 8 10 = 4 01 = 2 00 = 1
9	SPEED_OPT_EN	RGZ: 0, RW PAP: Strap, RW	Speed Optimization Enable: 1 = Enable Speed Optimization. 0 = Disable Speed Optimization.
8	SPEED_OPT_ENHANCED_EN	1, RW	Speed Optimization Enhanced Mode Enable: In enhanced mode, speed is optimized if energy is not detected in channels C and D. 1 = Enable Speed Optimization enhanced mode. 0 = Disable Speed Optimization enhanced mode.
7	SGMII_AUTONEG_EN	1, RW	SGMII Auto-Negotiation Enable: 1 = Enable SGMII Auto-Negotaition. 0 = Disable SGMII Auto-Negotaition.
6	SPEED_OPT_10M_EN	1, RW	Enable Speed Optimization to 10BASE-Te: 1 = Enable speed optimization to 10BASE-Te if link establishment fails in 1000BASE-T and 100BASE-TX . 0 = Disable speed optimization to 10BASE-Te.
5:0	RESERVED	0 0111, RO	RESERVED

8.6.19 Receiver Error Counter Register (RECR)

Table 29. Receiver Error Counter Register (RECR), Address 0x0015

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	RXERCNT[15:0]	0, RO, WSC	RX_ER Counter: Receive error counter. This register saturates at the maximum value of 0xFFFF. It is cleared by dummy write to this register.

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8.6.20 BIST Control Register (BISCR)

This register is used for Build-In Self Test (BIST) configuration. The BIST functionality provides Pseudo Random Bit Stream (PRBS) mechanism including packet generation generator and checker. Selection of the exact loopback point in the signal chain is also done in this register.

Table 30. BIST Control Register (BISCR), Address 0x0016

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	PRBS_COUNT_MODE	0, RW	PRBS Continuous Mode: 1 = Continuous mode enabled. When one of the PRBS counters reaches the maximum value, a pulse is generated and the counter starts counting from zero again. This bit must be set for proper PRBS operation. 0 = PRBS continuous mode disabled. PRBS operation is not supported for this setting.
14	GEN_PRBS_PACKET	0, RW	Generated PRBS Packets: 1 = When the packet generator is enabled, it will generate continuous packets with PRBS data. When the packet generator is disabled, the PRBS checker is still enabled. 0 = When the packet generator is enabled, it will generate a single packet with constant data. PRBS generation and checking is disabled.
13	PACKET_GEN_64BIT_MODE	0, RW	BIST Packet Size: 1 = Transmit 64 byte packets in packet generation mode. 0 = Transmit 1518 byte packets in packet generation mode
12	PACKET_GEN_EN	0, RW	Packet BIST Enable: 1 = Enable packet/PRBS generator 0 = Disable packet/PRBS generator
11:8	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
7	REV_LOOP_RX_DATA_CTRL	0, RW	Reverse Loopback Receive Data Control: This bit may only be set in Reverse Loopback mode. 1 = Send RX packets to MAC in reverse loop 0 = Suppress RX packets to MAC in reverse loop
6	MII_LOOP_TX_DATA_CTRL	0, RW	MII Loopback Transmit Data Control: This bit may only be set in MII Loopback mode. 1 = Transmit data to MDI in MII loop 0 = Suppress data to MDI in MII loop
5:2	LOOPBACK_MODE	0, RW	Loopback Mode Select: PCS Loopback must be disabled (Bits [1:0] =00) prior to selecting the loopback mode. 1000: Reverse loop 0100: External loop 0010: Analog loop 0001: Digital loop

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Table 30. BIST Control Register (BISCR), Address 0x0016 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
1:0	PCS_LOOPBACK	0, RW	PCS Loopback Select: When configured for 100Base-TX: 11: Loop after MLT3 encoder (full TX/RX path) 10: Loop after scrambler, before MLT3 encoder 01: Loop before scrambler When configured for 1000Base-T: x1: Loop before 1000Base-T signal processing.

8.6.21 Status Register 2 (STS2)

Table 31. Status Register 2 (STS2), Address 0x0017

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
11	PRBS_LOCK	0, RO	PRBS Lock Status: 1 = PRBS checker is locked to the received byte stream. 0 = PRBS checker is not locked.
10	PRBS_LOCK_LOST	0, RO, LH, COR	PRBS Lock Lost: 1 = PRBS checker has lost lock. 0 = PRBS checker has not lost lock.
9	PKT_GEN_BUSY	0, RO	Packet Generator Busy: 1 = Packet generation is in process. 0 = Packet generation is not in process.
8	SCR_MODE_MASTER_1G	0, RO	Gigabit Master Scramble Mode: 1 = 1G PCS (master) is in legacy encoding mode. 0 = 1G PCS (master) is in normal encoding mode..
7	SCR_MODE_MASTER_1G	0, RO	Gigabit Slave Scramble Mode: 1 = 1G PCS (slave) is in legacy encoding mode. 0 = 1G PCS (slave) is in normal encoding mode..
6	CORE_PWR_MODE	0, RO	Core Power Mode: 1 = Core is in normal power mode. 0 = Core is power-down mode or in sleep mode.
5:0	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.

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8.6.22 LED Configuration Register 1 (LEDCR1)

This register maps the LED functions to the corresponding pins.

Table 32. LED Configuration Register 1 (LEDCR1), Address 0x0018

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	LED_GPIO_SEL	RW, 0110	Source of the GPIO LED_3: 1111: Reserved 1110: Receive Error 1101: Receive Error or Transmit Error 1100: RESERVED 1011: Link established, blink for transmit or receive activity 1010: Full duplex 1001: 100/1000BT link established 1000: 10/100BT link established 0111: 10BT link established 0110: 100 BTX link established 0101: 1000BT link established 0100: Collision detected 0011: Receive activity 0010: Transmit activity 0001: Receive or Transmit activity 0000: Link established
11:8	LED_2_SEL	RW, 0001	Source of LED_2: 1111: Reserved 1110: Receive Error 1101: Receive Error or Transmit Error 1100: RESERVED 1011: Link established, blink for transmit or receive activity 1010: Full duplex 1001: 100/1000BT link established 1000: 10/100BT link established 0111: 10BT link established 0110: 100 BTX link established 0101: 1000BT link established 0100: Collision detected 0011: Receive activity 0010: Transmit activity 0001: Receive or Transmit activity 0000: Link established

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Table 32. LED Configuration Register 1 (LEDCR1), Address 0x0018 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
7:4	LED_1_SEL	RW, 0101	Source of LED_1: 1111: Reserved 1110: Receive Error 1101: Receive Error or Transmit Error 1100: RESERVED 1011: Link established, blink for transmit or receive activity 1010: Full duplex 1001: 100/1000BT link established 1000: 10/100BT link established 0111: 10BT link established 0110: 100 BTX link established 0101: 1000BT link established 0100: Collision detected 0011: Receive activity 0010: Transmit activity 0001: Receive or Transmit activity 0000: Link established
3:0	LED_0_SEL	RW, 0000	Source of LED_0: 1111: Reserved 1110: Receive Error 1101: Receive Error or Transmit Error 1100: RESERVED 1011: Link established, blink for transmit or receive activity 1010: Full duplex 1001: 100/1000BT link established 1000: 10/100BT link established 0111: 10BT link established 0110: 100 BTX link established 0101: 1000BT link established 0100: Collision detected 0011: Receive activity 0010: Transmit activity 0001: Receive or Transmit activity 0000: Link established

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8.6.23 LED Configuration Register 2 (LEDCR2)

This register provides the ability to directly control any or all LED outputs.

Table 33. LED Configuration Register 2 (LEDCR2), Address 0x0019

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
14	LED_GPIO_POLARITY	1, RW	GPIO LED Polarity: 1 = Active high 0 = Active low
13	LED_GPIO_DRV_VAL	0, RW	GPIO LED Drive Value: Value to force on GPIO LED This bit is only valid if enabled through LED_GPIO_DRV_EN.
12	LED_GPIO_DRV_EN	0, RW	GPIO LED Drive Enable: 1 = Force the value of the LED_GPIO_DRV_VAL bit onto the GPIO LED. 0 = Normal operation
11	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
10	LED_2_POLARITY	1, RW	LED_2 Polarity: 1 = Active high 0 = Active low
9	LED_2_DRV_VAL	0, RW	LED_2 Drive Value: Value to force on LED_2 This bit is only valid if enabled through LED_2_DRV_EN.
8	LED_2_DRV_EN	0, RW	LED_2 Drive Enable: 1 = Force the value of the LED_2_DRV_VAL bit onto LED_2. 0 = Normal operation
7	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
6	LED_1_POLARITY	1, RW	LED_1 Polarity: 1 = Active high 0 = Active low
5	LED_1_DRV_VAL	0, RW	LED_1 Drive Value: Value to force on LED_1 This bit is only valid if enabled through LED_1_DRV_EN.
4	LED_1_DRV_EN	0, RW	LED_1 Drive Enable: 1 = Force the value of the LED_1_DRV_VAL bit onto LED_1. 0 = Normal operation
3	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
2	LED_0_POLARITY	1, RW	LED_0 Polarity: 1 = Active high 0 = Active low
1	LED_0_DRV_VAL	0, RW	LED_0 Drive Value: Value to force on LED_0 This bit is only valid if enabled through LED_0_DRV_EN.
0	LED_0_DRV_EN	0, RW	LED_0 Drive Enable: 1 = Force the value of the LED_0_DRV_VAL bit onto LED_0. 0 = Normal operation

8.6.24 LED Configuration Register (LEDCR3)

This register controls the LED blink rate and stretching.

Table 34. LED Configuration Register 3 (LEDCR3), Address 0x001A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:3	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
2	LEDS_BYPASS_STRETCHING	0, RW	Bypass LED Stretching: 1 = Bypass LED Stretching 0 = Normal operation

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Table 34. LED Configuration Register 3 (LEDCR3), Address 0x001A (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
1:0	LEDS_BLINK_RATE	10, RW	LED Blink Rate: 11: 2 Hz (500 ms) 10: 5 Hz (200 ms) 01: 10 Hz (100 ms) 00 = 20 Hz (50 ms)

8.6.25 Configuration Register 3 (CFG3)

Table 35. Configuration Register 3 (CFG3), Address 0x001E

<table>
<tr><th>BIT</th><th>BIT NAME</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>15</td><td>Fast Link-Up in Parallel Detect</td><td>0, RW</td><td>Fast Link-Up in Parallel Detect Mode:
1 = Enable Fast Link-Up time During Parallel Detection
0 = Normal Parallel Detection link establishment
In Fast Auto MDI-X this bit is automatically set.</td></tr>
<tr><td>14</td><td>Fast AN Enable</td><td>0, RW</td><td>Fast Auto-Negotiation Enable:
1 = Enable Fast Auto-Negotiation mode – The PHY auto-negotiates using Timer setting according to Fast AN Sel bits
0 = Disable Fast Auto-Negotiation mode – The PHY auto-negotiates using normal Timer setting
Adjusting these bits reduces the time it takes to Auto-negotiate between two PHYs. Note: When using this option care must be taken to maintain proper operation of the system. While shortening these timer intervals may not cause problems in normal operation, there are certain situations where this may lead to problems.</td></tr>
<tr><td>13:12</td><td>Fast AN Sel</td><td>0, RW</td><td>Fast Auto-Negotiation Select bits:
<table>
<tr><th>Fast AN Select</th><th>Break Link Timer(ms)</th><th>Link Fall Inhibit Timer(ms)</th><th>Auto-Neg Wait Timer(ms)</th></tr>
<tr><td><00></td><td>80</td><td>50</td><td>35</td></tr>
<tr><td><01></td><td>120</td><td>75</td><td>50</td></tr>
<tr><td><10></td><td>240</td><td>150</td><td>100</td></tr>
<tr><td><11></td><td>NA</td><td>NA</td><td>NA</td></tr>
</table>
Adjusting these bits reduces the time it takes to auto-negotiate between two PHYs. In Fast AN mode, both PHYs should be configured to the same configuration. These 2 bits define the duration for each state of the Auto-Negotiation process according to the table above. The new duration time must be enabled by setting Fast AN En - bit 4 of this register. Note: Using this mode in cases where both link partners are not configured to the same Fast Auto-Negotiation configuration might produce scenarios with unexpected behavior.</td></tr>
</table>

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Table 35. Configuration Register 3 (CFG3), Address 0x001E (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
11	Extended FD Ability	0, RW	Extended Full-Duplex Ability: 1 = Force Full-Duplex while working with link partner in forced 100B-TX. When the PHY is set to Auto-Negotiation or Force 100B-TX and the link partner is operated in Force 100B-TX, the link is always Full Duplex 0 = Disable Extended Full Duplex Ability. Decision to work in Full Duplex or Half Duplex mode follows IEEE specification.
10	RESERVED	0, RO	RESERVED
9	Robust Auto-MDIX	0, RW	Robust Auto-MDIX: 1 =Enable Robust Auto MDI/MDIX resolution 0 = Normal Auto MDI/MDIX mode If link partners are configured to operational modes that are not supported by normal Auto MDI/MDIX mode (like Auto-Neg versus Force 100Base-TX or Force 100Base-TX versus Force 100Base-TX), this Robust Auto MDI/MDIX mode allows MDI/MDIX resolution and prevents deadlock.
8	Fast Auto-MDIX	0, RW	Fast Auto MDI/MDIX: 1 = Enable Fast Auto MDI/MDIX mode 0 = Normal Auto MDI/MDIX mode If both link partners are configured to work in Force 100Base-TX mode (Auto-Negotiation is disabled), this mode enables Automatic MDI/MDIX resolution in a short time.
7	INT_OE	0, RW	Interrupt Output Enable: 1 = INTN/PWDNN Pad is an Interrupt Output. 0 = INTN/PWDNN Pad in a Power-Down Input.
6	FORCE_INTERRUPT	0, RW	Force Interrupt: 1 = Assert interrupt pin. 0 = Normal interrupt mode.
5:3	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
2	TDR_FAIL	0, RO	TDR Failure: 1 = TDR failed. 0 = Normal TDR operation.
1	TDR_DONE	1, RO	TDR Done: 1 = TDR has completed. 0 = TDR has not completed.
0	TDR_START	0, RW	TDR Start: 1 = Start TDR. 0 = Normal operation

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8.6.26 Control Register (CTRL)

Table 36. Control Register (CTRL), Address 0x001F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	SW_RESET	0, RW, SC	Software Reset: 1 = Perform a full reset, including registers. 0 = Normal operation.
14	SW_RESTART	0, RW, SC	Software Restart: 1 = Perform a full reset, not including registers. . 0 = Normal operation.
13:0	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.

8.6.27 Testmode Channel Control (TMCH_CTRL)

Table 37. Testmode Channel Control (TMCH_CTRL), Address 0x0025

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0x04	RESERVED
7:5	TM_CH_SEL	0x0	Test mode Channel Select. If bit 7 is set then Test mode is driven on all 4 channels. If bit 7 is cleared then test modes are driven according to bits 6:5 as follows: 00: Channel A 01: Channel B 10: Channel C 11: Channel D
4:0	RESERVED	0x00	RESERVED

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8.6.28 Robust Auto MDIX Timer Configuration Register (AMDIX_TMR_CFG)

In order to use this register the Robust AMDIX feature must be enabled.

Table 38. Robust Auto MDIX Timer Configuration Register (RAMDIX_TMR_CFG), Address 0x002C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:4	RESERVED	0x141, RW	RESERVED
3:0	RAMDIX_TMR	0xF, RW	Robust Auto MDIX Timer 0000: 32 ms 0001: 64 ms 0010: 96 ms . . 1111: 480 ms

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8.6.29 Fast Link Drop Configuration Register (FLD_CFG)

Table 39. Fast Link Drop Configuration Register (FLD_CFG), Address 0x002D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	FORCE_DROP	0, RW	Force Drop Link Forces the link partner to drop the link when no signal is received. 1 = Drops link 0 = Normal operation
14	FLD_EN	0, RW	1000BASE-T Fast Link Drop: This bit must be set to 0 during the link up process. After the link is established set this bit to 1 to enable FLD. 1 = Enable FLD 0 = Normal operation
13	RESERVED	0, RO	RESERVED
12:8	FLD_STS	0, RO, LH	Fast Link Drop Status: Status Registers that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming this criterion was enabled): Bit 12: Descrambler Loss Sync Bit 11: RX Errors Bit 10: MLT3 Errors Bit 9: SNR level Bit 8: Signal/Energy Lost
7:5	RESERVED	0, RO	RESERVED
4:0	FLD_SRC_CFG	0, RW	Fast Link Drop Source Configuration: The following FLD sources can be configured independently: Bit 4: Descrambler Loss Sync Bit 3: RX Errors Bit 2: MLT3 Errors Bit 1: SNR level Bit 0: Signal/Energy Lost

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8.6.30 Fast Link Drop Threshold Configuration Register (FLD_THR_CFG)

Table 40. Fast Link Drop Threshold Configuration Register (FLD_THR_CFG), Address 0x002E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	RESERVED	0, RO	RESERVED
10:8	RESERVED	0x2, RW	RESERVED
7	RESERVED	0, RO	RESERVED
6:4	RESERVED	0x2, RW	RESERVED
3	RESERVED	0, RO	RESERVED
2:0	ENERGY_LOST_FLD_THR	0x1, RW	Energy Lost Threshold for FLD Energy Lost Mode ENERGY_LOST_FLD_THR will be asserted if energy detector accumulator falls below this threshold. When using strap to enable FLD feature, this bit defaults to 0x2. Register write is needed to change it to 0x1. Changing the field to other value is not advised.

8.6.31 Configuration Register 4 (CFG4)

Table 41. Configuration Register 4 (CFG4), Address 0x0031

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:9	RESERVED	0, RO	RESERVED
8	RESERVED	0, RW	RESERVED
7	INT_TST_MODE_1	Strap, RW	Internal Test Mode 1. This needs to be disabled. The RX_DV/RX_CTRL strap must be configured for strap mode 3 or strap mode 4. If the RX_CTRL pin cannot be strapped to mode 3 or mode 4, if not this bit must be cleared to 0 through register configuration. 1: Internal Test Mode 1, this bit must be cleared 0: Normal Operation
6:5	SGMII_AUTONEG_TIMER	01, RW	SGMII Auto-Negotiation Timer Duration: 11: 11 ms 10: 800 µs 01: 2 µs 00: 16 ms
4:1	RESERVED	1000, RO	RESERVED: Writes ignored, read as 1000.
0	PORT_MIRROR_EN	Strap, RW	Port Mirror Enable: 1 = Enable port mirroring. 0 = Normal operation

8.6.32 RGMII Control Register (RGMIICTL)

This register provides access to the RGMII controls.

Table 42. RGMII Control Register (RGMIICTL), Address 0x0032

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
7	RGMII_EN	RGZ: 1, RW PAP: Strap, RW	RGMII Enable: 1 = Enable RGMII interface. 0 = Disable RGMII interface.
6:5	RGMII_RX_HALF_FULL_THR	10, RW	RGMII Receive FIFO Half Full Threshold: This field controls the RGMII receive FIFO half full threshold.
4:3	RGMII_TX_HALF_FULL_THR	10, RW	RGMII Transmit FIFO Half Full Threshold: This field controls the RGMII transmit FIFO half full threshold.
2	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
1	RGMII_TX_CLK_DELAY	0, RW	RGMII Transmit Clock Delay: 1 = RGMII transmit clock is shifted relative to transmit data. 0 = RGMII transmit clock is aligned to transmit data.

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Table 42. RGMII Control Register (RGMIICTL), Address 0x0032 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
0	RGMII_RX_CLK_DELAY	0, RW	RGMII Receive Clock Delay: 1 = RGMII receive clock is shifted relative to receive data. 0 = RGMII receive clock is aligned to receive data.

8.6.33 RGMII Control Register 2 (RGMIICTL2)

Table 43. RGMII Control Register 2 (RGMIICTL2), Address 0x0033

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:5	RESERVED	0, RO	RESERVED
4	RGMII_AF_BYPASS_EN	0, RW	RGMII Async FIFO Bypass Enable:
			1 = Enable RGMII Async FIFO Bypass.
			0 = Normal operation.
3	RGMII_AF_BYPASS_DLY_EN	0, RW	RGMII Async FIFO Bypass Delay Enable: 1 = Delay RX_CLK when operating in 10/100 with RGMII. 0 = Normal operation.
2	LOW_LATENCY_10_100_EN	0, RW	Low Latency 10/100 Enable: 1 = Enable low latency in 10/100 operation. 0 = Normal operation.
1:0	RESERVED	0, RO	RESERVED

8.6.34 SGMII Auto-Negotiation Status (SGMII_ANEG_STS)

Table 44. SGMII Auto-Negotiation Status (SGMII_ANEG_STS)), address 0x0037

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:2	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
1	SGMII_PAGE_RX	0, RO	SGMII Page Received: 1 = SGMII page has been received. 0 = SGMII page has not been received.
0	SGMII_AUTONEG_COMPLETE	0, RO	SGMII Auto-Negotiation Complete: 1 = SGMII Auto-Negotiation process complete. 0 = SGMII Auto-Negotiation process not complete.

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8.6.35 100BASE-TX Configuration (100CR)

Table 45. 100BASE-TX Configuration Register (100CR), Address 0x0043

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0, RO	RESERVED
11	DESCRAM_TIMEOUT_DIS	0, RW	Disable 100Base-TX Descrambler Timeout: 1 = Disable packet reception when received packet violates the descrambler timeout. This occurs when the packet is longer than 1.5 ms. 0 = Stops packet reception when received packet violates the descrambler timeout. This occurs when the packet is longer than 1.5 ms.
10:7	DESCRAM_TIMEOUT	1111, RW	Descrambler Timeout: Adjust the descrambler time out value. This value refers to the recovery time due to descrambler unlock. Timer is in ms units.
6	FORCE_100_OK	0, RW	Force 100-Mbps Good Link: 1 = Forces 100-Mbps good link. 0 = Normal operation.
5	ENH_MLT3_DET_EN	1, RW	Enhanced MLT-3 Detection Enable: 1 = Enable enhanced MLT-3 Detection. 0 = Normal operation.
4	ENH_IPG_DET_EN	0, RW	Enhanced Interpacket Gap Detection Enable: 1 = Enable enhanced interpacket gap detection. 0 = Normal operation.
3	RESERVED	0, RO	RESERVED
2	SCR_DIS	0, RW	Disable Scrambler: 1 = Disable scrambler. 0 = Normal operation.
1	ODD_NIBBLE_DETECT	0, RW	Enable Odd Nibble Detection: 1 = Detect when an odd number of nibbles is received. 0 = Normal operation.
0	FAST_RX_DV	0, RW	Fast RX_DV Enable: 1 = Enable fast RX_DV. 0 = Normal operation.

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8.6.36 Viterbi Module Configuration (VTM_CFG)

Table 46. Viterbi Module Configuration (VTM_CFG), Address 0x0053

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:4	RESERVED	0x205, RO	RESERVED
3:0	VTM_IDLE_CHECK_CNT_THR	0x5, RW	Viterbi Detector Idle Count Threshold Threshold for consecutive amount of Idle symbols for Viterbi Idle detector to assert Idle Mode. Default value 0x5 is for IPG >= 12. Set this field to 0x4: for IPG < 12. Please verify new register settings through system level tests if this field is changed.

8.6.37 Skew FIFO Status (SKEW_FIFO)

Table 47. Skew FIFO Status (SKEW_FIFO), Address 0x0055

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	RESERVED
7:4	CH_B_SKEW	0, RO	Skew of RX channel B to align symbols in # of clock cycles.
3:0	CH_A_SKEW	0, RO	Skew of RX channel A to align symbols in # of clock cycles.

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8.6.38 Strap Configuration Status Register 1 (STRAP_STS1)

Table 48. Strap Configuration Status Register 1 (STRAP_STS1), Address 0x006E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	STRAP_MIRROR_EN	Strap, RO	Mirror Enable Strap: 1 = Port mirroring strapped to enable. 0 = Port mirroring strapped to disable.
14	STRAP_LINK_DOWNSHIFT_EN	Strap, RO	Link Downshift Enable Strap: 1 = Link Downshift strapped to enable. 0 = Link Downshift strapped to disable.
13	STRAP_CLK_OUT_DIS	Strap, RO	Clock Output Disable Strap: 1 = Clock output strapped to disable. 0 = Clock output strapped to enable.
12	STRAP_RGMII_DIS	Strap, RO	RGMII Disable Strap: 1 = RGMII strapped to disable. 0 = RGMII strapped to enable.
11	STRAP_SGMII_EN	Strap, RO	SGMII Enable Strap: 1 = SGMII strapped to enable. 0 = SGMII strapped to disable.
10	STRAP_AMDIX_DIS	Strap, RO	Auto-MDIX Disable Strap: 1 = Auto-MDIX strapped to disable. 0 = Auto-MDIX strapped to enable.
9	STRAP_FORCE_MDI_X	Strap, RO	Force MDI/X Strap: 1 = Force MDIX strapped to enable. 0 = Force MDI strapped to enable.
8	STRAP_HD_EN	Strap, RO	Half Duplex Enable Strap: 1 = Half Duplex strapped to enable. 0 = Full Duplex strapped to enable.
7	STRAP_ANEG_DIS	Strap, RO	Auto-Negotiation Disable Strap: 1 = Auto-Negotiation strapped to disable. 0 = Auto-Negotiation strapped to enable.
6	RESERVED	0, RO	RESERVED
5	STRAP_ANEG_SEL	Strap, RO	ANEG_SEL value from strap. See Auto-Negotiation Select Strap Details table.
4	RESERVED	0, RO	RESERVED
3:0	STRAP_PHY_ADD	Strap, RO	PHY Address Strap: PHY address value from straps.

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8.6.39 Strap Configuration Status Register 2 (STRAP_STS2)

Table 49. Strap Configuration Status Register 2 (STRAP_STS2), Address 0x006F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	RESERVED	0, RO	RESERVED
10	STRAP_ FLD	Strap, RO	Fast Link Drop (FLD) Enable Strap: 1 = FLD strapped to enable. 0 = FLD strapped to disable.
9	RESERVED	0, RO	RESERVED
8	RESERVED	0, RO	RESERVED
7	RESERVED	0, RO	RESERVED
6:4	STRAP_RGMII_CLK_SKEW_TX	Strap, RO	RGMII Transmit Clock Skew Strap: RGMII_TX_DELAY_CTRL[2:0] values from straps. See RGMII Transmit Clock Skew Details table for more information.
3	RESERVED	0, RO	RESERVED
2:0	STRAP_RGMII_CLK_SKEW_RX	Strap, RO	RGMII Receive Clock Skew Strap: RGMII_RX_DELAY_CTRL[2:0] values from straps. See Table 8 for more information.

8.6.40 BIST Control and Status Register 1 (BICSR1)

Table 50. BIST Control and Status Register 1 (BICSR1), Address 0x0071

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PRBS_BYTE_CNT	0x0000, RO	Holds the number of total bytes received by the PRBS checker. Value in this register is locked when write is done to register BICSR2 bit[0] or bit[1]. The count stops at 0xFFFF when PRBS_COUNT_MODE in BISCR register (0x0016) is set to 0.

8.6.41 BIST Control and Status Register 2 (BICSR2)

Table 51. BIST Control and Status Register 2 (BICSR2), Address 0x0072

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	Reserved	0x00, RO	Ignored on Read
10	PRBS_PKT_CNT_OVF	0, RO	PRBS Checker Packet Count Overflow If set, PRBS Packet counter has reached overflow. Overflow is cleared when PRBS counters are cleared by setting bit #1 of this register.
9	PRBS_BYTE_CNT_OVF	0, RO	PRBS Byte Count Overflow If set, PRBS Byte counter has reached overflow. Overflow is cleared when PRBS counters are cleared by setting bit #1 of this register.
8	Reserved	0,RO	Ignore on Read
7:0	PRBS_ERR_CNT	0x00, RO	Holds number of error bytes that are received by PRBS checker. Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF (see register 0x0016) Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters

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8.6.42 BIST Control and Status Register 3 (BICSR3)

Table 52. BIST Control and Status Register 3 (BICSR3), Address 0x007B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PKT_LEN_PRBS	0x05DC, RW	Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x05DC, which is equal to 1500 bytes. Each packet is appended with 13 nibbles of 0x5 and then 0xD5 (SFD).

8.6.43 BIST Control and Status Register 4 (BICSR4)

Table 53. BIST Control and Status Register 4 (BICSR4), Address 0x007C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0x00, RO	RESERVED
7:0	IPG_LEN	0x7D, RW	Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D (equal to 500 bytes). An increment in this fields value corresponds to an addition of 4 bytes to the IPG Length.

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8.6.44 RGMII Delay Control Register (RGMIIDCTL)

This register provides access to the RGMII delay controls.

Table 54. RGMII Delay Control Register (RGMIIDCTL), Address 0x0086

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
7:4	RGMII_TX_DELAY_CTRL	Strap, RW	RGMII Transmit Clock Delay: 1111: 4.00 ns 1110: 3.75 ns 1101: 3.50 ns 1100: 3.25 ns 1011: 3.00 ns 1010: 2.75 ns 1001: 2.50 ns 1000: 2.25 ns 0111: 2.00 ns 0110: 1.75 ns 0101: 1.50 ns 0100: 1.25 ns 0011: 1.00 ns 0010: 0.75 ns 0001: 0.50 ns 0000: 0.25 ns
3:0	RGMII_RX_DELAY_CTRL	Strap, RW	RGMII Receive Clock Delay: 1111: 4.00 ns 1110: 3.75 ns 1101: 3.50 ns 1100: 3.25 ns 1011: 3.00 ns 1010: 2.75 ns 1001: 2.50 ns 1000: 2.25 ns 0111: 2.00 ns 0110: 1.75 ns 0101: 1.50 ns 0100: 1.25 ns 0011: 1.00 ns 0010: 0.75 ns 0001: 0.50 ns 0000: 0.25 ns

8.6.45 PLL Clock-out Control Register (PLLCTL)

Table 55. PLL Clock-out Control Register (PLLCTL), Address 0x00C6

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:5	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
4	CLK_MUX	0, RW	Internal Clock MUX Control: 1 = Configures analog CLK_OUT to be TX_TCLK for compliance testing. 0 = Normal operation.
3:0	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.

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8.6.46 SGMII Control Register 1 (SGMIICTL1)

Table 56. SGMII Control Register 1 (SGMIICTL1), Address 0x00D3

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
14	SGMII_TYPE	0, RW	SGMII Configuration: 1 = 6-wire mode. Enable differential SGMII clock to MAC. 0 = 4-wire mode
13:0	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.

8.6.47 Sync FIFO Control (SYNC_FIFO_CTRL)

Table 57. Sync FIFO Control (SYNC_FIFO_CTRL), Address 0x00E9

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	RESERVED	0x9F22, RW	RESERVED

8.6.48 Loopback Configuration Register (LOOPCR)

Table 58. Loopback Configuration Register (LOOPCR), Address 0x00FE

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	LOOP_CFG_VAL	1110 0111 0010 0001, RW	Loopback Configuration Value: 1110 0111 0010 000: Configuration for loopback modes. A software reset through bit 14 of the Control Register (CTRL), address 0x001F, is required after changes to this register value. Other values for this register are not recommended.

8.6.49 DSP Feedforward Equalizer Configuration (DSP_FFE_CFG)

Certain applications may need this register to be configured to 0x0E81 to improve Short Cable performance. Changing this register to 0x0E81, will not effect Long Cable performance.

Table 59. DSP Feedforward Equalizer Configuration (DSP_FFE_CFG), Address 0x012C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	RESERVED	0000 11, RO	RESERVED
9:0	FFE_EQ	00 0010 1101, RW	FFE Equalizer Configuration Set this field to 10 1000 0001 when using cables of length <= 1 m.

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8.6.50 Receive Configuration Register (RXFCFG)

This register provides receive configuration for Wake-on-LAN (WoL).

Table 60. Receive Configuration Register (RXFCFG), Address 0x0134

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0, RO	RESERVED
11	WOL_OUT_CLEAR	0, RW, SC	Clear Wake-on-LAN Output: This bit is only applicable when configured for level mode. 1 = Clear Wake-on-LAN output
10:9	WOL_OUT_STRETCH	00, RW	Wake-on-LAN Output Stretch: If WoL out is configured for pulse mode, the pulse length is defined as the following number of 125-MHz clock cycles: 11 = 64 clock cycles 10 = 32 clock cycles 01 = 16 clock cycles 00 = 8 clock cycles
8	WOL_OUT_MODE	0, RW	Wake-on-LAN Output Mode: 1 = Level Mode. WoL is cleared by a write to WOL_OUT_CLEAR (bit 11). 0 = Pulse Mode. Pulse width is configured via WOL_OUT_STRETCH (bits 10:9).
7	ENHANCED_MAC_SUPPORT	0, RW	Enable Enhanced Receive Features: 1 = Enable for Wake-on-LAN, CRC check, and Receive 1588 indication. 0 = Normal operation.
6	RESERVED	0, RO	RESERVED
5	SCRON_EN	0, RW	Enable SecureOn Password: 1 = SecureOn Password enabled. 0 = SecureOn Password disabled.
4	WAKE_ON_UCAST	0, RW	Wake on Unicast Packet: 1 = Issue an interrupt upon reception of Unicast packet. 0 = Do not issue an interrupt upon reception of Unicast packet.
3	RESERVED	0, RO	RESERVED
2	WAKE_ON_BCAST	1, RW	Wake on Broadcast Packet: 1 = Issue an interrupt upon reception of Broadcast packet. 0 = Do not issue an interrupt upon reception of Broadcast packet.
1	WAKE_ON_PATTERN	0, RW	Wake on Pattern Match: 1 = Issue an interrupt upon pattern match. 0 = Do not issue an interrupt upon pattern match.
0	WAKE_ON_MAGIC	0, RW	Wake on Magic Packet: 1 = Issue an interrupt upon reception of Magic packet. 0 = Do not issue an interrupt upon reception of Magic packet.

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8.6.51 Receive Status Register (RXFSTS)

This register provides status for receive functionality.

Table 61. Receive Status Register (RXFSTS), Address 0x0135

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	RESERVED
7	SFD_ERR	0, R0, LH, SC	SFD Error: 1 = Packet with SFD error (without an 0x5D SFD byte) received. 0 = No SFD error seen.
6	BAD_CRC	0, R0, LH, SC	Bad CRC: 1 = A packet with a bad CRC was received. 0 = No bad CRC seen.
5	SCRON_HACK	0, R0, LH, SC	SecureOn Hack Attempt Flag: 1 = SecureOn Hack attempt seen. 0 = No SecureOn Hack attempt seen.
4	UCAST_RCVD	0, R0, LH, SC	Unicast Packet Received: 1 = A valid Unicast packet was received. 0 = No valid Unicast packet was received.
3	RESERVED	0, RO	RESERVED
2	BCAST_RCVD	0, R0, LH, SC	Broadcast Packet Received: 1 = A valid Broadcast packet was received. 0 = No valid Broadcast packet was received.
1	PATTERN_RCVD	0, R0, LH, SC	Pattern Match Received: 1 = A valid packet with the configured pattern was received. 0 = No valid packet with the configured pattern was received.
0	MAGIC_RCVD	0, R0, LH, SC	Magic Packet Received: 1 = A valid Magic packet was received. 0 = No valid Magic packet was received.

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8.6.52 Pattern Match Data Register 1 (RXFPMD1)

Table 62. Pattern Match Data Register 1 (RXFPMD1), Address 0x0136

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PMATCH_DATA_15_0	0, RW	Bits 15:0 of Perfect Match Data - used for DA (destination address) match

8.6.53 Pattern Match Data Register 2 (RXFPMD2)

Table 63. Pattern Match Data Register 2 (RXFPMD2), address 0x0137

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PMATCH_DATA_31_16	0, RW	Bits 31:16 of Perfect Match Data - used for DA (destination address) match

8.6.54 Pattern Match Data Register 3 (RXFPMD3)

Table 64. Pattern Match Data Register 3 (RXFPMD3), address 0x0138

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PMATCH_DATA_ 47_32	0, RW	Bits 47:32 of Perfect Match Data - used for DA (destination address) match

8.6.55 SecureOn Pass Register 2 (RXFSOP1)

Table 65. SecureOn Pass Register 1 (RXFSOP1), Address 0x0139

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	SCRON_PASSWORD _15_0	0, RW	Bits 15:0 of secure-on password for magic packet)

8.6.56 SecureOn Pass Register 2 (RXFSOP2)

Table 66. SecureOn Pass Register 2 (RXFSOP2), Address 0x013A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	SCRON_PASSWORD _31_16	0, RW	Bits 31:16 of secure-on password for magic packet

8.6.57 SecureOn Pass Register 3 (RXFSOP3)

Table 67. SecureOn Pass Register 3 (RXFSOP3), Address 0x013B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	SCRON_PASSWORD _ 47_32	0, RW	Bits 47:32 of secure-on password for magic packet

8.6.58 Receive Pattern Register 1 (RXFPAT1)

Table 68. Receive Pattern Register 1 (RXFPAT1), Address 0x013C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_0_1	0, RW	Bytes 0 (LSbyte) + 1 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.59 Receive Pattern Register 2 (RXFPAT2)

Table 69. Receive Pattern Register 2 (RXFPAT2), Address 0x013D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_2_3	0, RW	Bytes 2 + 3 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

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8.6.60 Receive Pattern Register 3 (RXFPAT3)

Table 70. Receive Pattern Register 3 (RXFPAT3), Address 0x013E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_4_5	0, RW	Bytes 4 + 5 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.61 Receive Pattern Register 4 (RXFPAT4)

Table 71. Receive Pattern Register 4 (RXFPAT4), Address 0x013F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_6_7	0, RW	Bytes 6 + 7 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.62 Receive Pattern Register 5 (RXFPAT5)

Table 72. Receive Pattern Register 5 (RXFPAT5), Address 0x0140

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_8_9	0, RW	Bytes 8 + 9 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.63 Receive Pattern Register 6 (RXFPAT6)

Table 73. Receive Pattern Register 6 (RXFPAT6), Address 0x0141

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_10_11	0, RW	Bytes 10 + 11 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.64 Receive Pattern Register 7 (RXFPAT7)

Table 74. Receive Pattern Register 7 (RXFPAT7), Address 0x0142

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_12_13	0, RW	Bytes 12 + 13 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.65 Receive Pattern Register 8 (RXFPAT8)

Table 75. Receive Pattern Register 8 (RXFPAT8), Address 0x0143

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_14_15	0, RW	Bytes 0 14 + 15 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.66 Receive Pattern Register 9 (RXFPAT9)

Table 76. Receive Pattern Register 9 (RXFPAT9), Address 0x0144

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_16_17	0, RW.	Bytes 16 + 17 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

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8.6.67 Receive Pattern Register 10 (RXFPAT10)

Table 77. Receive Pattern Register 10 (RXFPAT10), Address 0x0145

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_18_19	0, RW	Bytes 18 + 19 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.68 Receive Pattern Register 11 (RXFPAT11)

Table 78. Receive Pattern Register 11 (RXFPAT11), Address 0x0146

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_20_21	0, RW	Bytes 20 + 21 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.69 Receive Pattern Register 12 (RXFPAT12)

Table 79. Receive Pattern Register 12 (RXFPAT12), Address 0x0147

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_22_23	0, RW	Bytes 22 + 23 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.70 Receive Pattern Register 13 (RXFPAT13)

Table 80. Receive Pattern Register 13 (RXFPAT13), Address 0x0148

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_24_25	0, RW	Bytes 24 + 25 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.71 Receive Pattern Register 14 (RXFPAT14)

Table 81. Receive Pattern Register 14 (RXFPAT14), Address 0x0149

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_26_27	0, RW	Bytes 26 + 27 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.72 Receive Pattern Register 15 (RXFPAT15)

Table 82. Receive Pattern Register 15 (RXFPAT15), address 0x014A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_28_29	0, RW	Bytes 28 + 29 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.73 Receive Pattern Register 16 (RXFPAT16)

Table 83. Receive Pattern Register 16 (RXFPAT16), Address 0x014B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_30_31	0, RW	Bytes 30 + 31 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

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8.6.74 Receive Pattern Register 17 (RXFPAT17)

Table 84. Receive Pattern Register 17 (RXFPAT17), Address 0x014C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_32_33	0, RW	Bytes 32 + 33 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.75 Receive Pattern Register 18 (RXFPAT18)

Table 85. Receive Pattern Register 18 (RXFPAT18), Address 0x014D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_34_35	0, RW	Bytes 34 + 35 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.76 Receive Pattern Register 19 (RXFPAT19)

Table 86. Receive Pattern Register 19 (RXFPAT19), Address 0x014E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_36_37	0, RW	Bytes 36 + 37 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.77 Receive Pattern Register 20 (RXFPAT20)

Table 87. Receive Pattern Register 20 (RXFPAT20), Address 0x014F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_38_39	0, RW	Bytes 38 + 39 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.78 Receive Pattern Register 21 (RXFPAT21)

Table 88. Receive Pattern Register 21 (RXFPAT21), Address 0x0150

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_38_39	0, RW	Bytes 38 + 39 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.79 Receive Pattern Register 22 (RXFPAT22)

Table 89. Receive Pattern Register 22 (RXFPAT22), Address 0x0151

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_42_43	0, RW	Bytes 42 + 43 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.80 Receive Pattern Register 23 (RXFPAT23)

Table 90. Receive Pattern Register 23 (RXFPAT23), Address 0x0152

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_44_45	0, RW	Bytes 44 + 45 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

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8.6.81 Receive Pattern Register 24 (RXFPAT24)

Table 91. Receive Pattern Register 24 (RXFPAT24), Address 0x0153

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_46_47	0, RW	Bytes 46 + 47 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.82 Receive Pattern Register 25 (RXFPAT25)

Table 92. Receive Pattern Register 25 (RXFPAT25), Address 0x0154

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_48_49	0, RW	Bytes 48 + 49 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.83 Receive Pattern Register 26 (RXFPAT26)

Table 93. Receive Pattern Register 26 (RXFPAT26), Address 0x0155

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_50_51	0, RW	Bytes 50 + 51 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.84 Receive Pattern Register 27 (RXFPAT27)

Table 94. Receive Pattern Register 27 (RXFPAT27), Address 0x0156

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_52_53	0, RW	Bytes 52 + 53 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.85 Receive Pattern Register 28 (RXFPAT28)

Table 95. Receive Pattern Register 28 (RXFPAT28), Address 0x0157

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_54_55	0, RW	Bytes 54 + 55 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.86 Receive Pattern Register 29 (RXFPAT29)

Table 96. Receive Pattern Register 29 (RXFPAT29), Address 0x0158

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_56_57	0, RW	Bytes 56 + 57 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.87 Receive Pattern Register 30 (RXFPAT30)

Table 97. Receive Pattern Register 30 (RXFPAT30), Address 0x0159

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_58_59	0, RW	Bytes 58 + 59 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

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8.6.88 Receive Pattern Register 31 (RXFPAT31)

Table 98. Receive Pattern Register 31 (RXFPAT31), Address 0x015A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_0_1	0, RW	Bytes 60 + 61 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.89 Receive Pattern Register 32 (RXFPAT32)

Table 99. Receive Pattern Register 32 (RXFPAT32), Address 0x015B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_62_63	0, RW	Bytes 62 + 63 of the configured pattern. Each byte can be masked separately through the RXF_PATTERN_BYTE_MASK registers.

8.6.90 Receive Pattern Byte Mask Register 1 (RXFPBM1)

Table 100. Receive Pattern Byte Mask Register 1 (RXFPBM1), Address 0x015C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_ MASK_0_15	0, RW	Masks for bytes 0 to 15 of the pattern. A 1 indicates a mask for the associated byte.

8.6.91 Receive Pattern Byte Mask Register 2 (RXFPBM2)

Table 101. Receive Pattern Byte Mask Register 2 (RXFPBM2), Address 0x015D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_ MASK_16_31	0, RW	Masks for bytes 16 to 31 of the pattern. A 1 indicates a mask for the associated byte.

8.6.92 Receive Pattern Byte Mask Register 3 (RXFPBM3)

Table 102. Receive Pattern Byte Mask Register 3 (RXFPBM3), Address 0x015E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_ MASK_32_47	0, RW	Masks for bytes 32 to 47 of the pattern. A 1 indicates a mask for the associated byte.

8.6.93 Receive Pattern Byte Mask Register 4 (RXFPBM4)

Table 103. Receive Pattern Byte Mask Register 4 (RXFPBM4), Address 0x015F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PATTERN_BYTES_ MASK_48_63	0, RW	Masks for bytes 48 to 63 of the pattern. A 1 indicates a mask for the associated byte.

8.6.94 Receive Pattern Control (RXFPATC)

Table 104. Receive Status Register (RXFSTS), Address 0x0161

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:6	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
5:0	PATTERN_START_POINT	0, RW	Number of bytes after SFD where comparison of the RX packet to the configured pattern begins: 111111 - Start compare in the 64th byte after SFD 000000 - Start compare in the 1st byte after SFD

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8.6.95 10M SGMII Configuration (10M_SGMII_CFG)

Table 105. 10M SGMII Configuration (10M_SGMII_CFG), Address 0x016F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0000 0000, RO	RESERVED
7	10M_SGMII_RATE_ADAPT	1, RW	RESERVED - Do not change this bit. The PHY adapts automatically to 10M speed.
6:0	RESERVED	001 0101, RO	RESERVED

8.6.96 I/O Configuration (IO_MUX_CFG)

Table 106. I/O Configuration (IO_MUX_CFG), Address 0x0170

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	RESERVED	0, RO	RESERVED
12:8	CLK_O_SEL	0 1100, RW	Clock Output Select: 01101 - 11111: RESERVED 01100: Reference clock (synchronous to XI input clock) 01011: Channel D transmit clock 01010: Channel C transmit clock 01001: Channel B transmit clock 01000: Channel A transmit clock 00111: Channel D receive clock divided by 5 00110: Channel C receive clock divided by 5 00101: Channel B receive clock divided by 5 00100: Channel A receive clock divided by 5 00011: Channel D receive clock 00010: Channel C receive clock 00001: Channel B receive clock 00000: Channel A receive clock
7	RESERVED	0, RO	RESERVED
6	CLK_O_DISABLE	0, RW	Clock Output Disable: 1 = Disable clock output on CLK_OUT pin. 0 = Enable clock output on CLK_OUT pin.
5	RESERVED	0, RO	RESERVED
4:0	IO_IMPEDANCE_CTRL	TRIM, RW	Impedance Control for MAC I/Os: Output impedance approximate range from 35-70 Ω in 32 steps. Lowest being 11111 and highest being 00000. Range and Step size will vary with process. Default is set to 50 Ω by trim. But the default register value can vary by process. Non default values of MAC I/O impedance can be used based on trace impedance. Mismatch between device and trace impedance can cause voltage overshoot and undershoot.

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8.6.97 GPIO Mux Control Register (GPIO_MUX_CTRL)

Table 107. GPIO Mux Control Register (GPIO_MUX_CTRL), Address 0x0172

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	RESERVED
7:4	GPIO_1_CTRL	RW, 0000	GPIO_1 Control: 1010 - 1111: RESERVED 1001: Constant 1 1000: Constant 0 0111: PRBS Errors / Loss of Sync 0110: LED_3 0101: RESERVED 0100: Energy Detect (1000Base-T and 100Base-TX only) 0011: WOL 0010: 1588 RX SFD 0001: 1588 TX SFD 0000: COL
3:0	GPIO_0_CTRL	RW, 0000	GPIO_0 Control: 1010 - 1111: RESERVED 1001: Constant 1 1000: Constant 0 0111: PRBS Errors / Loss of Sync 0110: LED_3 0101: RESERVED 0100: Energy Detect (1000Base-T and 100Base-TX only) 0011: WOL 0010: 1588 RX SFD 0001: 1588 TX SFD 0000: RX_ER

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8.6.98 TDR General Configuration Register 1 (TDR_GEN_CFG1)

Table 108. TDR General Configuration Register 1 (TDR_GEN_CFG1), Address 0x0180

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	RESERVED	0, RO	RESERVED
12	TDR_CH_CD_BYPASS	0, RW	TDR Bypass for Channel C and D: 1 = Bypass channel C and D in TDR tests. 0 = Normal operation.
11	TDR_CROSS_MODE_DIS	0, RW	Disable TDR Cross Mode: 1 = Disable cross mode option. Do not check cross channels. Only listen to the channel being used for transmit. 0 = Normal operation.
10	TDR_NLP_CHECK	1, RW	TDR NLP Check: 1 = Check for NLPs during silence. 0 = Normal operation.
9:7	TDR_AVG_NUM	110, RW	Number Of TDR Cycles to Average: 111: RESERVED: Writes ignored, read as 0. 110: 64 TDR cycles 101: 32 TDR cycles 100: 16 TDR cycles 011: 8 TDR cycles 010: 4 TDR cycles 001: 2 TDR cycles 000: 1 TDR cycle
6:4	TDR_SEG_NUM	101, RW	Set the number of TDR segments to check.
3:0	TDR_CYCLE_TIME	010, RW	Set the time for each TDR cycle. Value is measured in microseconds.

8.6.99 TDR Peak Locations Register 1 (TDR_PEAKS_LOC_1)

Table 109. TDR Peak Locations Register 1 (TDR_PEAKS_LOC_1), Address 0x0190

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_A_1	0, RO	Location of the second peak discovered by the TDR mechanism on channel A. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_A_0	0, RO	Location of the first peak discovered by the TDR mechanism on channel A. The value of these bits is translated into distance from the PHY.

8.6.100 TDR Peak Locations Register 2 (TDR_PEAKS_LOC_2)

Table 110. TDR Peak Locations Register 2 (TDR_PEAKS_LOC_2), Address 0x0191

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_A_3	0, RO	Location of the fourth peak discovered by the TDR mechanism on channel A. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_A_2	0, RO	Location of the third peak discovered by the TDR mechanism on channel A. The value of these bits is translated into distance from the PHY.

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8.6.101 TDR Peak Locations Register 3 (TDR_PEAKS_LOC_3)

Table 111. TDR Peak Locations Register 3 (TDR_PEAKS_LOC_3), Address 0x0192

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_B_0	0, RO	Location of the first peak discovered by the TDR mechanism on channel B. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_A_4	0, RO	Location of the fifth peak discovered by the TDR mechanism on channel A. The value of these bits is translated into distance from the PHY.

8.6.102 TDR Peak Locations Register 4 (TDR_PEAKS_LOC_4)

Table 112. TDR Peak Locations Register 4 (TDR_PEAKS_LOC_4), Address 0x0193

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_B_2	0, RO	Location of the third peak discovered by the TDR mechanism on channel B. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_B_1	0, RO	Location of the second peak discovered by the TDR mechanism on channel B. The value of these bits is translated into distance from the PHY.

8.6.103 TDR Peak Locations Register 5 (TDR_PEAKS_LOC_5)

Table 113. TDR Peak Locations Register 5 (TDR_PEAKS_LOC_5), Address 0x0194

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_B_4	0, RO	Location of the fifth peak discovered by the TDR mechanism on channel B. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_B_3	0, RO	Location of the fourth peak discovered by the TDR mechanism on channel B. The value of these bits is translated into distance from the PHY.

8.6.104 TDR Peak Locations Register 6 (TDR_PEAKS_LOC_6)

Table 114. TDR Peak Locations Register 6 (TDR_PEAKS_LOC_6), Address 0x0195

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_C_1	0, RO	Location of the second peak discovered by the TDR mechanism on channel C. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_C_0	0, RO	Location of the first peak discovered by the TDR mechanism on channel C. The value of these bits is translated into distance from the PHY.

8.6.105 TDR Peak Locations Register 7 (TDR_PEAKS_LOC_7)

Table 115. TDR Peak Locations Register 7 (TDR_PEAKS_LOC_7), Address 0x0196

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_C_3	0, RO	Location of the fourth peak discovered by the TDR mechanism on channel C. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_C_2	0, RO	Location of the third peak discovered by the TDR mechanism on channel C. The value of these bits is translated into distance from the PHY.

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8.6.106 TDR Peak Locations Register 8 (TDR_PEAKS_LOC_8)

Table 116. TDR Peak Locations Register 8 (TDR_PEAKS_LOC_8), Address 0x0197

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_D_0	0, RO	Location of the first peak discovered by the TDR mechanism on channel D. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_C_4	0, RO	Location of the fifth peak discovered by the TDR mechanism on channel C. The value of these bits is translated into distance from the PHY.

8.6.107 TDR Peak Locations Register 9 (TDR_PEAKS_LOC_9)

Table 117. TDR Peak Locations Register 9 (TDR_PEAKS_LOC_9), Address 0x0198

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_D_2	0, RO	Location of the third peak discovered by the TDR mechanism on channel D. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_D_1	0, RO	Location of the second peak discovered by the TDR mechanism on channel D. The value of these bits is translated into distance from the PHY.

8.6.108 TDR Peak Locations Register 10 (TDR_PEAKS_LOC_10)

Table 118. TDR Peak Locations Register 10 (TDR_PEAKS_LOC_10), Address 0x0199

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TDR_PEAKS_LOC_D_4	0, RO	Location of the fifth peak discovered by the TDR mechanism on channel D. The value of these bits is translated into distance from the PHY.
7:0	TDR_PEAKS_LOC_D_3	0, RO	Location of the fourth peak discovered by the TDR mechanism on channel D. The value of these bits is translated into distance from the PHY.

8.6.109 TDR Peak Amplitudes Register 1 (TDR_PEAKS_AMP_1)

Table 119. TDR Peak Amplitudes Register 1 (TDR_PEAKS_AMP_1), Address 0x019A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_A_1	0, RO	Amplitude of the second peak discovered by the TDR mechanism on channel A. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_A_0	0, RO	Amplitude of the first peak discovered by the TDR mechanism on channel A. The value of these bits is translated into type of cable fault and-or interference.

8.6.110 TDR Peak Amplitudes Register 2 (TDR_PEAKS_AMP_2)

Table 120. TDR Peak Amplitudes Register 2 (TDR_PEAKS_AMP_2), Address 0x019B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_A_3	0, RO	Amplitude of the fourth peak discovered by the TDR mechanism on channel A. The value of these bits is translated into type of cable fault and-or interference.

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Table 120. TDR Peak Amplitudes Register 2 (TDR_PEAKS_AMP_2), Address 0x019B (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_A_2	0, RO	Amplitude of the third peak discovered by the TDR mechanism on channel A. The value of these bits is translated into type of cable fault and-or interference.

8.6.111 TDR Peak Amplitudes Register 3 (TDR_PEAKS_AMP_3)

Table 121. TDR Peak Amplitudes Register 3 (TDR_PEAKS_AMP_3), Address 0x019C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_B_0	0, RO	Amplitude of the first peak discovered by the TDR mechanism on channel B. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_A_4	0, RO	Amplitude of the fifth peak discovered by the TDR mechanism on channel A. The value of these bits is translated into type of cable fault and-or interference.

8.6.112 TDR Peak Amplitudes Register 4 (TDR_PEAKS_AMP_4)

Table 122. TDR Peak Amplitudes Register 4 (TDR_PEAKS_AMP_4), Address 0x019D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_B_2	0, RO	Amplitude of the third peak discovered by the TDR mechanism on channel B. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_B_1	0, RO	Amplitude of the second peak discovered by the TDR mechanism on channel B. The value of these bits is translated into type of cable fault and-or interference.

8.6.113 TDR Peak Amplitudes Register 5 (TDR_PEAKS_AMP_5)

Table 123. TDR Peak Amplitudes Register 5 (TDR_PEAKS_AMP_5), Address 0x019E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_B_4	0, RO	Amplitude of the fifth peak discovered by the TDR mechanism on channel B. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_B_3	0, RO	Amplitude of the fourth peak discovered by the TDR mechanism on channel B. The value of these bits is translated into type of cable fault and-or interference.

8.6.114 TDR Peak Amplitudes Register 6 (TDR_PEAKS_AMP_6)

Table 124. TDR Peak Amplitudes Register 6 (TDR_PEAKS_AMP_6), Address 0x019F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED

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Table 124. TDR Peak Amplitudes Register 6 (TDR_PEAKS_AMP_6), Address 0x019F (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
14:8	TDR_PEAKS_AMP_C_1	0, RO	Amplitude of the second peak discovered by the TDR mechanism on channel C. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_C_0	0, RO	Amplitude of the first peak discovered by the TDR mechanism on channel C. The value of these bits is translated into type of cable fault and-or interference.

8.6.115 TDR Peak Amplitudes Register 7 (TDR_PEAKS_AMP_7)

Table 125. TDR Peak Amplitudes Register 7 (TDR_PEAKS_AMP_7), Address 0x01A0

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_C_3	0, RO	Amplitude of the fourth peak discovered by the TDR mechanism on channel C. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_C_2	0, RO	Amplitude of the third peak discovered by the TDR mechanism on channel C. The value of these bits is translated into type of cable fault and-or interference.

8.6.116 TDR Peak Amplitudes Register 8 (TDR_PEAKS_AMP_8)

Table 126. TDR Peak Amplitudes Register 8 (TDR_PEAKS_AMP_8), Address 0x01A1

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_D_0	0, RO	Amplitude of the first peak discovered by the TDR mechanism on channel D. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_C_4	0, RO	Amplitude of the fifth peak discovered by the TDR mechanism on channel C. The value of these bits is translated into type of cable fault and-or interference.

8.6.117 TDR Peak Amplitudes Register 9 (TDR_PEAKS_AMP_9)

Table 127. TDR Peak Amplitudes Register 9 (TDR_PEAKS_AMP_9), Address 0x01A2

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_D_2	0, RO	Amplitude of the third peak discovered by the TDR mechanism on channel D. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_D_1	0, RO	Amplitude of the second peak discovered by the TDR mechanism on channel D. The value of these bits is translated into type of cable fault and-or interference.

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8.6.118 TDR Peak Amplitudes Register 10 (TDR_PEAKS_AMP_10)

Table 128. TDR Peak Amplitudes Register 10 (TDR_PEAKS_AMP_10), Address 0x01A3

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED
14:8	TDR_PEAKS_AMP_D_4	0, RO	Amplitude of the fifth peak discovered by the TDR mechanism on channel D. The value of these bits is translated into type of cable fault and-or interference.
7	RESERVED	0, RO	RESERVED
6:0	TDR_PEAKS_AMP_D_3	0, RO	Amplitude of the fourth peak discovered by the TDR mechanism on channel D. The value of these bits is translated into type of cable fault and-or interference.

8.6.119 TDR General Status (TDR_GEN_STATUS)

Table 129. TDR General Status (TDR_GEN_STATUS), Address 0x01A4

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0, RO	RESERVED
11	TDR_P_LOC_CROSS_MODE_D	0, RO	Cross Detect on Channel D: 1 = Cross reflection detected on channel D. Indicates a short between channels. 0 = No cross reflection detected.
10	TDR_P_LOC_CROSS_MODE_C	0, RO	Cross Detect on Channel C: 1 = Cross reflection detected on channel C. Indicates a short between channels. 0 = No cross reflection detected.
9	TDR_P_LOC_CROSS_MODE_B	0, RO	Cross Detect on Channel B: 1 = Cross reflection detected on channel B. Indicates a short between channels. 0 = No cross reflection detected.
8	TDR_P_LOC_CROSS_MODE_A	0, RO	Cross Detect on Channel A: 1 = Cross reflection detected on channel A. Indicates a short between channels. 0 = No cross reflection detected.
7	TDR_P_LOC_OVERFLOW_D	0, RO	Peak Overflow on Channel D: 1 = More than 5 reflections were detected on channel D. 0 = Normal operation.
6	TDR_P_LOC_OVERFLOW_C	0, RO	Peak Overflow on Channel C: 1 = More than 5 reflections were detected on channel C. 0 = Normal operation.
5	TDR_P_LOC_OVERFLOW_B	0, RO	Peak Overflow on Channel B: 1 = More than 5 reflections were detected on channel B. 0 = Normal operation.
4	TDR_P_LOC_OVERFLOW_A	0, RO	Peak Overflow on Channel A: 1 = More than 5 reflections were detected on channel A. 0 = Normal operation.
3:0	RESERVED	0, RO	RESERVED

8.6.120 Programmable Gain Register (PROG_GAIN)

Table 130. Programmable Gain (PROG_GAIN), Address 0x01D5

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:4	RESERVED	1111 0101 0000, RW	RESERVED
3	UNF_FUNC_MODE	0, RW	For Force Mode Only 1 = Sets required swing level for compliance testing. 0 = Normal operation.

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Table 130. Programmable Gain (PROG_GAIN), Address 0x01D5 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
2	RESERVED	0, RW	RESERVED
1	SGMII_TX_POL_IN	0, RW	SGMII TX Bus Polarity Invert 1 = Invert Polarity 0 = Normal Polarity
0	SGMII_RX_POL_IN	0, RW	SGMII RX Bus Polarity Invert 1= Invert Polarity 0 = Normal Polarity

8.6.121 MMD3 PCS Control Register (MMD3_PCS_CTRL)

This register is accessed via indirect register access. See *Extended Address Space Access* for details

Table 131. MMD3 PCS Control Register (MMD3_PCS_CTRL), MMD3 Address 0x0000

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	PCS_RESET	0, RW, SC	MMD3 PCS Reset: 1 = Resets the MMD3 register. Note: Setting this bit will subsequently cause a soft reset via the BMCR RESET bit (bit 15 of register address 0x0000). 0 = Normal operation.
14:0	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DP83867 is a single port 10/100/1000 Ethernet PHY. It supports connections to an Ethernet MAC through SGMII or RGMII. Connections to the Ethernet media are made through the IEEE 802.3 defined Media Dependent Interface.

When using the device for Ethernet application, it is necessary to meet certain requirements for normal operation of the device. The following typical application and design requirements can be used for selecting appropriate component values for DP83867.

9.2 Typical Application

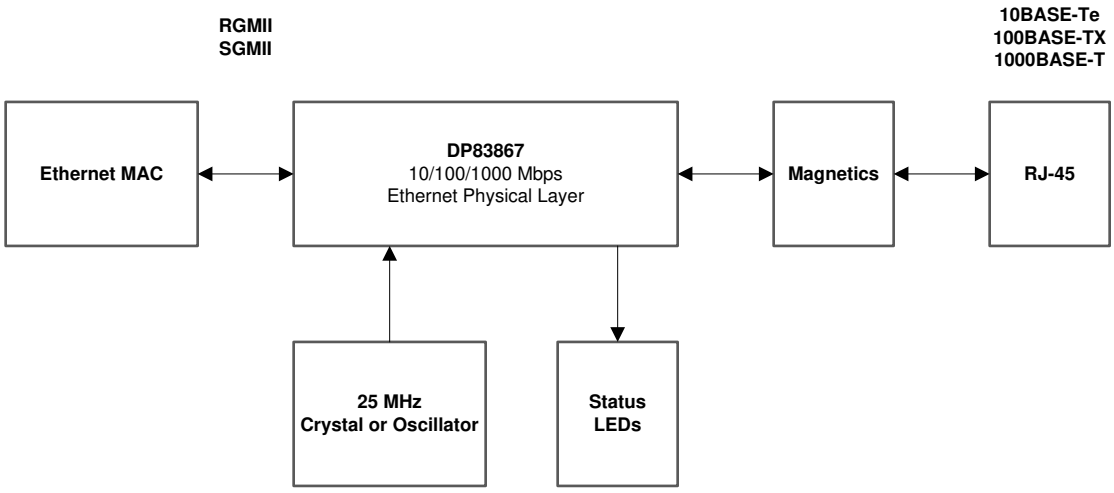


Figure 26. Typical DP83867 Application

9.2.1 Design Requirements

The design requirements for the DP83867 are:

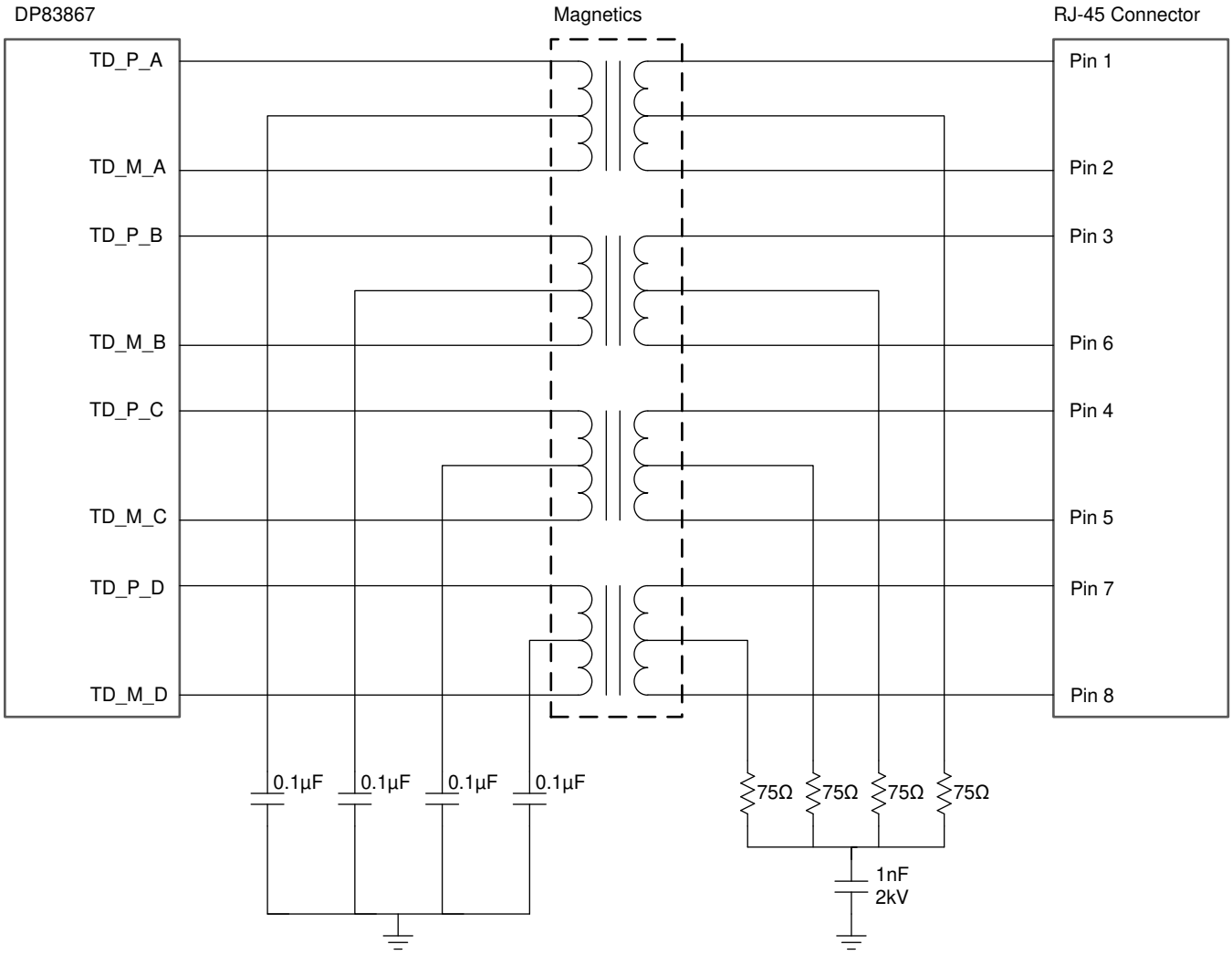
- VDDA2P5 = 2.5 V
- VDD1P0 = 1 V
- VDDIO = 3.3 V, 2.5 V, or 1.8 V
- Clock Input = 25 MHz

Typical Application (continued)

9.2.1.1 Cable Line Driver

The line driver implementation is designed to support simple connections to the transformer and the connector. The DP83867 includes integrated terminations so no external termination resistors are required.

The connection diagram for the cable line driver is shown in Figure 27.



(1) Each center tap on the side connected to the PHY, must be isolated from one another and connected to ground via a decoupling capacitor (0.1 µF recommended).

(2) Pulse Electronics part, HX5008FNL is recommended for a discrete magnetics solution.

Figure 27. Magnetics Connections

Magnetic isolation used with the DP83867 can either be a discrete solution or integrated with the RJ-45 connector. Refer to Table 132 for the electrical requirements.

Table 132. Magnetic Isolation Requirements

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Open Circuit Inductance	-	320 to 350	µH
Insertion Loss	1-100 MHz	-1	dB

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Typical Application (continued)

Table 132. Magnetic Isolation Requirements (continued)

PARAMETER	TEST CONDITIONS	TYP	UNIT
Return Loss	1-30 MHz	-16	dB
	30-60 MHz	-12	dB
	60-100 MHz	-10	dB
Differential to Common Mode Rejection Ratio	1-50 MHz	-30	dB
	50-150 MHz	-20	dB
Crosstalk	30 MHz	-35	dB
	60 MHz	-30	dB
Isolation	HPOT	1500	Vrms

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9.2.1.2 Clock In (XI) Recommendation

If an external clock source is used, XO should be left floating. For a 1.8-V clock source, XI should be tied to the clock source. For a 3.3-V or 2.5-V clock source, a capacitor divider is recommended as shown in Figure 28. For a 3.3-V clock source, the CD1 and CD2 capacitors used are recommended to be 27 pF. If a 2.5-V clock source is used check with the vendor for recommended capacitor loads. The values of CD1 and CD2 shall be adjusted to meet XI Input pin specification defined in Electrical Characteristics.

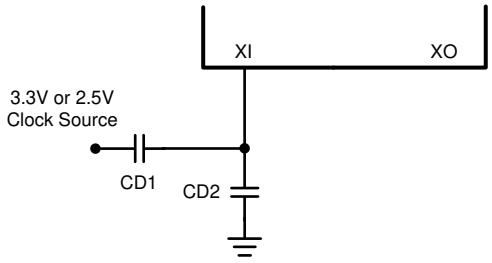

Figure 28. Clock Divider

The CMOS 25-MHz oscillator specifications are listed in Table 133. Additionally, the maximum oscillator phase noise tolerated by the PHY is shown in Figure 29

Table 133. 25-MHz Oscillator Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm
Rise / Fall Time	20% - 80%			5	ns
Symmetry	Duty Cycle	40%		60%	
Jitter RMS	Integration Band: 12 kHz to 5 MHz			11	ps

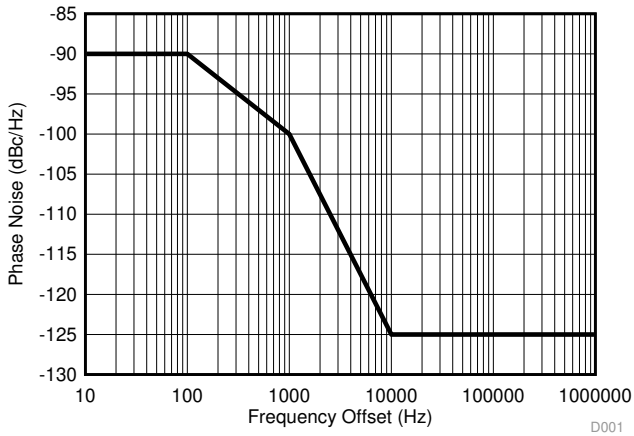

Figure 29. 25-MHz Oscillator Phase Noise

9.2.1.3 Crystal Recommendations

A 25-MHz, parallel, 18-pF load crystal resonator should be used if a crystal source is desired. Figure 30 shows a typical connection for a crystal resonator circuit. The load capacitor values vary with the crystal vendors; check with the vendor for the recommended loads.

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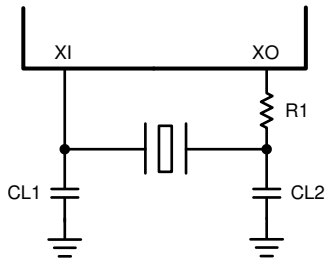

Figure 30. Crystal Oscillator Circuit

As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, CL1 and CL2 should be set at 27 pF, and R1 should be set at 0 Ω.

Specification for 25-MHz crystal are listed in Table 134.

Table 134. 25-MHz Crystal Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm

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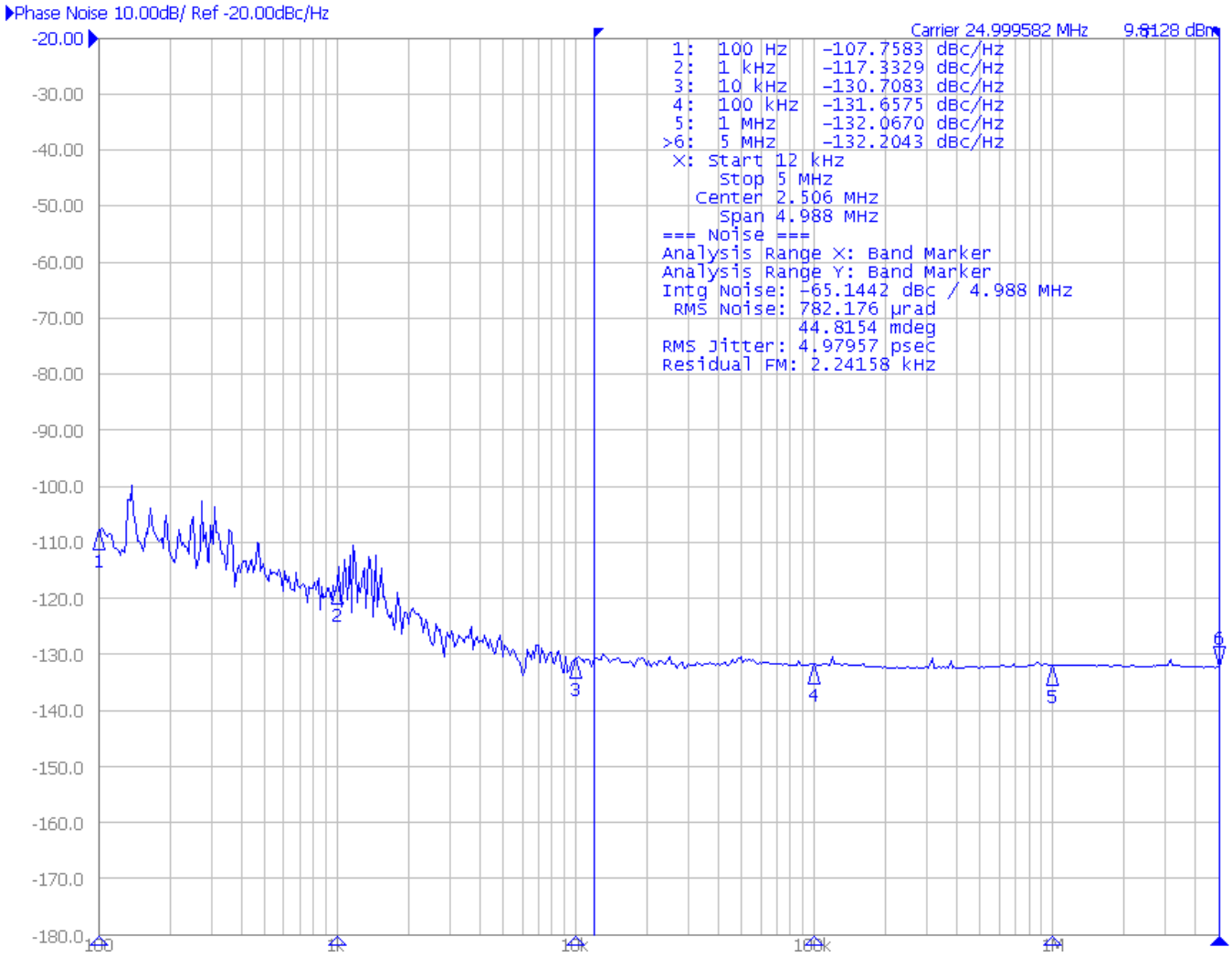
9.2.1.4 Clock Out (CLK_OUT) Phase Noise

Figure 31 provides a phase noise plot for the 25 MHz clock output from the device.



(1) This measurement was taken on a DP83867 configured as a slave. The PHY was linked to another DP83867 configured as the master. Both devices had PRBS enabled (BISCR, register 0x0016, configured to 0xD000).

(2) The phase noise on the CLK_OUT pin before linkup and after link up with no packets being generated are expected to be lower than pictured.

Figure 31. 25 MHz Clock Output Phase Noise

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9.2.2 Detailed Design Procedure

9.2.2.1 MAC Interface

The Media Independent Interface (SGMII / RGMII) connects the DP83867 to the Media Access Controller (MAC). The MAC may in fact be a discrete device, integrated into a microprocessor, CPU, or FPGA.

9.2.2.1.1 SGMII Layout Guidelines

- All SGMII connections must be AC-coupled through an 0.1-µF capacitor. Series capacitors must be 0.1 µF and the size should be 0402 or smaller.
- SGMII signals are differential signals.
- Traces must be routed with 100-Ω differential impedance.
- Skew matching within a pair must be less than 5 pS, which correlates to 30 mil for standard FR4.
- There is no requirement to match the TX pair to the RX pair.
- SGMII signals must be routed on the same layer.
- Pairs must be referenced to parallel ground plane.
- When operating in 6-wire mode, the RX pair must match the Clock pair to within 5 pS, which correlates to 30 mil for standard FR4.

9.2.2.1.2 RGMII Layout Guidelines

- RGMII signals are single-ended signals.
- Traces must be routed with impedance of 50 Ω to ground.
- Skew between TXD[3:0] lines should be less than 11 ps, which correlates to 60 mil for standard FR4.
- Skew between RXD[3:0] lines should be less than 11 ps, which correlates to 60 mil for standard FR4.
- Keep trace lengths as short as possible; less than 2 inches is recommended with less than 6 inches as maximum length.
- Configurable clock skew for GTX_CLK and RX_CLK.
  - Clock skew for RX and TX paths can be optimized independently.
  - Clock skew is adjustable in 0.25-ns increments (through register).

9.2.2.2 Media Dependent Interface (MDI)

The Media Dependent Interface (MDI) connects the DP83867 to the transformer and the Ethernet network.

9.2.2.2.1 MDI Layout Guidelines

- MDI traces must be 50 Ω to ground and 100 Ω-differential controlled impedance.
- Route MDI traces to transformer on the same layer.
- Use a metal shielded RJ-45 connector, and connect the shield to chassis ground.
- Use magnetics with integrated common-mode choking devices.
- Void supplies and ground beneath magnetics.
- Do not overlap the circuit and chassis ground planes, keep them isolated. Instead, make chassis ground an isolated island and make a void between the chassis and circuit ground. Connecting circuit and chassis planes using a size 1206 resistor and capacitor on either side of the connector is a good practice.

9.2.3 Application Curves

Table 135 lists the application curves for this application.

Table 135. Table of Graphs

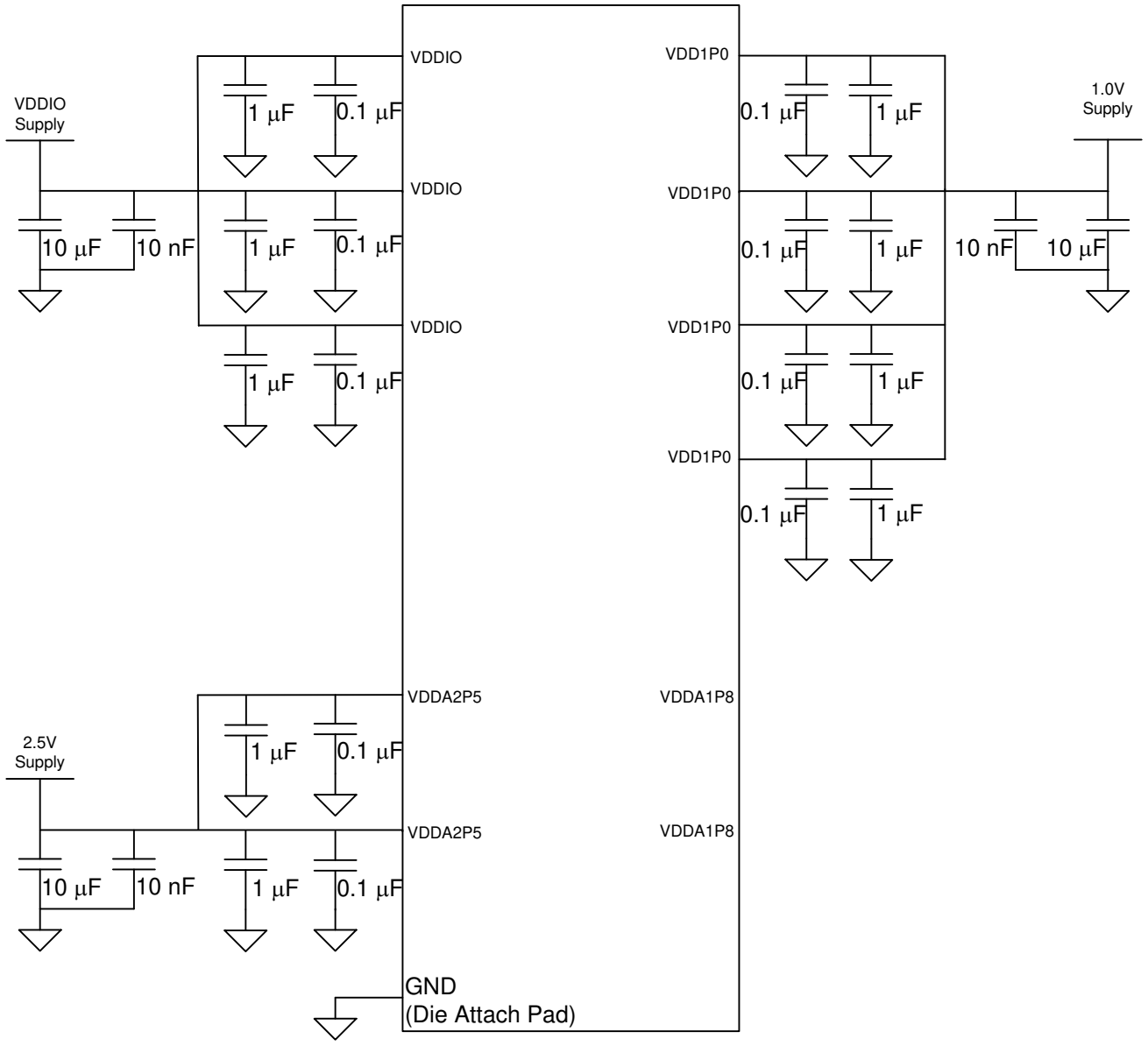
TITLE	FIGURE
1000Base-T Signaling	Figure 9
100Base-TX Signaling	Figure 10

10 Power Supply Recommendations

The DP83867 is capable of operating with as few as two or three supplies. The I/O power supply can also be operated independently of the main device power supplies to provide flexibility for the MAC interface.

For detailed information about DP83867 power consumption for specific supplies under a wide set of conditions, see the *DP83867E/IS/CS/IR/CR RGZ Power Consumption Data* application report (SNLA241).

The connection diagrams for the two-supply and three-supply configurations are shown in Figure 32 and Figure 33.



For two supply configuration, both VDDA1P8 pins must be left unconnected.

Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins, placing the 0.1-µF capacitor closest to the pin.

VDDIO may be 3.3 V or 2.5 V or 1.8 V.

No Components should be connected to VDDA1P8 pins in Two-Supply Configuration.

Figure 32. Two-Supply Configuration

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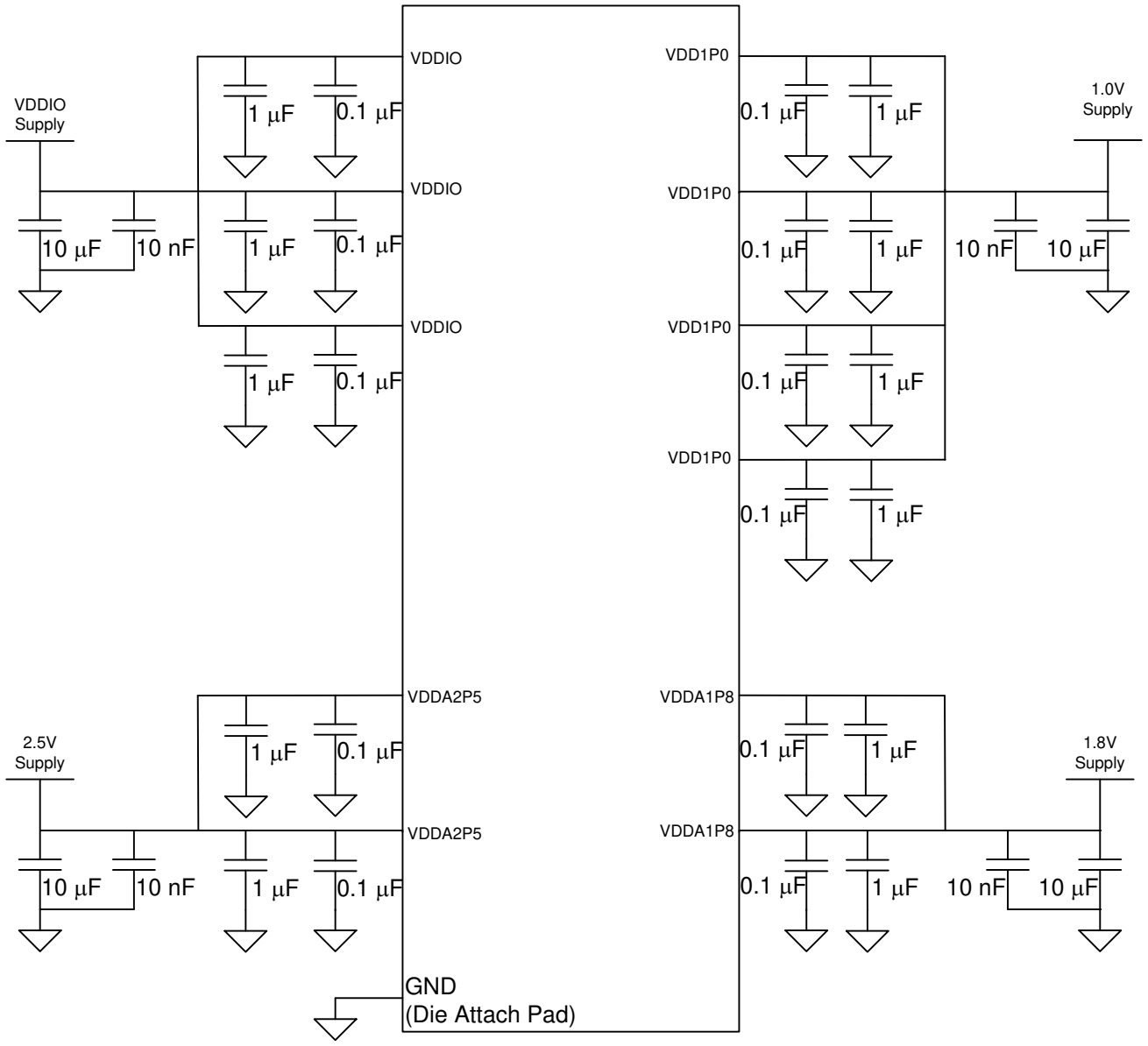

Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins, placing the 0.1-µF capacitor closest to the pin.

Note: VDDIO may be 3.3 V or 2.5 V or 1.8 V.

Figure 33. Three-Supply Configuration

There is no requirement for the sequence of the supplies when operating in two-supply mode.

When operating in three-supply mode, the 1.8-V VDDA1P8 supply must be stable within 25 ms of the 2.5-V VDDA2P5 supply ramping up. There is no sequencing requirement for other supplies when operating in three-supply mode.

When powering down the DP83867, the 1.8-V supply should be brought down before the 2.5-V supply.

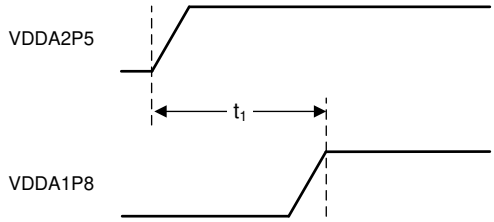

Figure 34. Three-Supply Mode Power Supply Sequence Diagram

Table 136. Three-Supply Mode Power Supply Sequence

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T1	Beginning of VDDA2P5 ramp up to VDDA1P8 stable		0		25	ms

NOTE

If the 2.5-V power supply provides power to DP83867 devices only, the 1.8-V supply may ramp up any time before 2.5-V.

11 Layout

11.1 Layout Guidelines

11.1.1 Signal Traces

PCB traces are lossy and long traces can degrade the signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces should be 50-Ω, single-ended impedance. Differential traces should be 50-Ω, single-ended and 100-Ω differential. Take care that the impedance is constant throughout. Impedance discontinuities cause reflections leading to EMI & signal integrity problems. Stubs must be avoided on all signal traces, especially the differential signal pairs. See Figure 35

Within the differential pairs, the trace lengths must run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common-mode noise and increased EMI.

Length matching is also important on MAC interface. All Transmit signal trace lengths must match to each other and all Receive signal trace lengths must match to each other.

Ideally, there should be no crossover or via on the signal paths. Vias present impedance discontinuities and should be minimized. Route an entire trace pair on a single layer if possible.

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Layout Guidelines (continued)

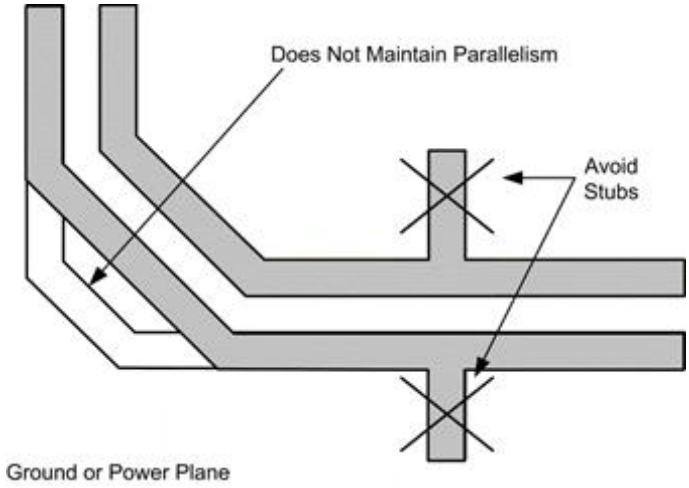

Figure 35. Avoiding Stubs in a Differential Signal Pair

Signals on different layers should not cross each other without at least one return path plane between them.

Coupling between traces is also an important factor. Unwanted coupling can cause cross talk problems. Differential pairs on the other hand, should have a constant coupling distance between them.

For convenience and efficient layout process, start by routing the critical signals first.

11.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path width can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path beneath the signal traces should be avoided at all cost. A signal crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems. See Figure 36

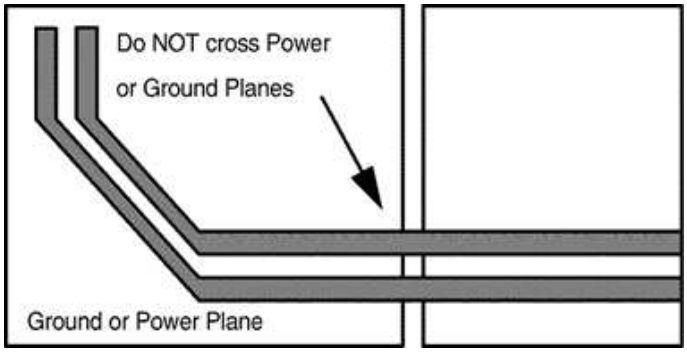

Figure 36. Differential Signal Pair-Plane Crossing

11.1.3 Transformer Layout

There should be no metal layer running beneath the transformer. Transformers can inject noise in metal beneath them which can affect the performance of the system.

11.1.4 Metal Pour

All metal pours which are not signals or power should be tied to ground. There should be no floating metal on the system. There should be no metal between the differential traces.

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Layout Guidelines (continued)

11.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, at minimum a 4-layer PCB should be used. However a 6-layer board is recommended. See Figure 37 for the recommended layer stack ups for 4, 6 and 8-layer boards. These are recommendations not requirements, other configurations can be used as per system requirements.

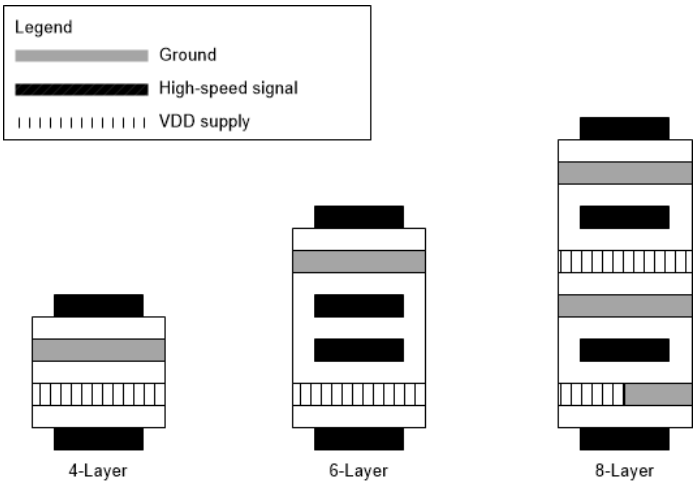

Figure 37. Recommended Layer Stack Up

Within a PCB, it may be desirable to run traces using different methods, microstrip vs. stripline, depending on the location of the signal on the PCB. For example, it may be desirable to change layer stacking where an isolated chassis ground plane is used. Figure 38 illustrates alternative PCB stacking options.

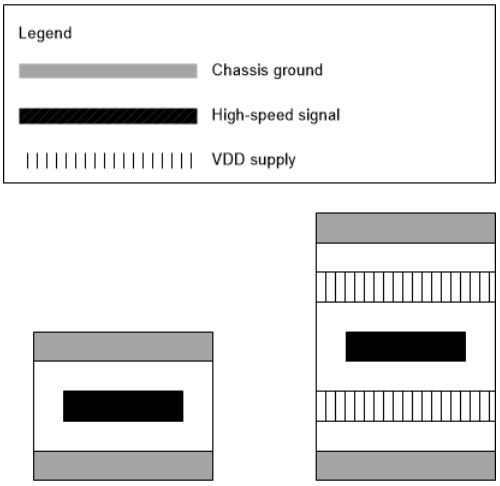

Figure 38. Alternative Layer Stack Up

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11.2 Layout Example

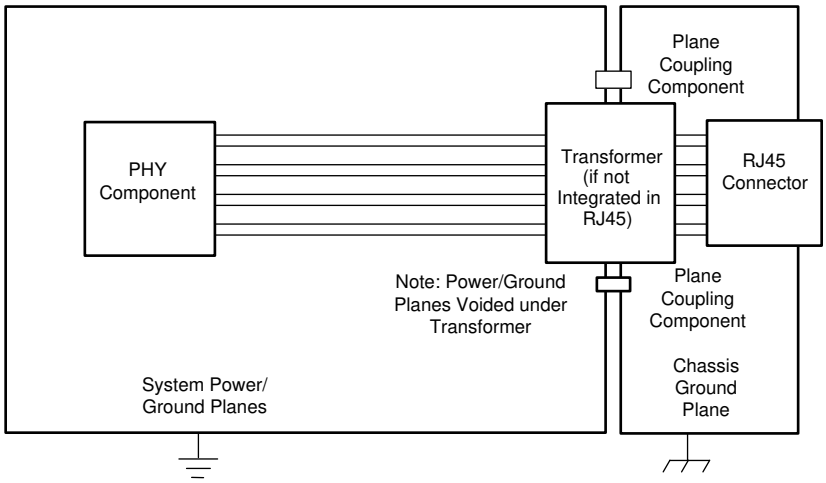

Figure 39. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *DP83867 Troubleshooting Guide* (SNLA246)
- *How to Configure DP838XX for Ethernet Compliance Testing* (SNLA239)
- *Configuring Ethernet Devices with 4-Level Straps* (SNLA258)
- *RGMII Interface Timing Budgets* (SNLA243)
- *DP83867E/IS/CS/IR/CR RGZ Power Consumption Data* (SNLA241)
- *How to Configure DP83867 Start of Frame* (SNLA242)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 137. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DP83867CS	Click here	Click here	Click here	Click here	Click here
DP83867IS	Click here	Click here	Click here	Click here	Click here
DP83867E	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83867CSRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	DP83867CS	Samples
DP83867CSRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	DP83867CS	Samples
DP83867ERGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	DP83867E	Samples
DP83867ERGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	DP83867E	Samples
DP83867ISRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DP83867IS	Samples
DP83867ISRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DP83867IS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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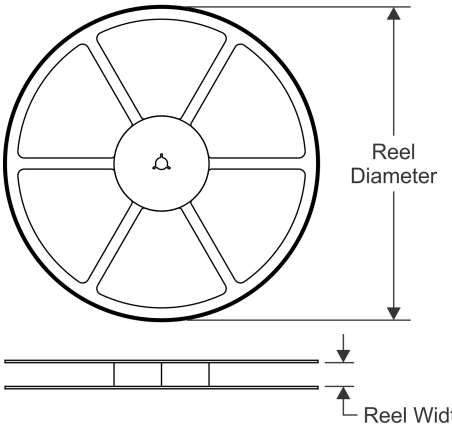
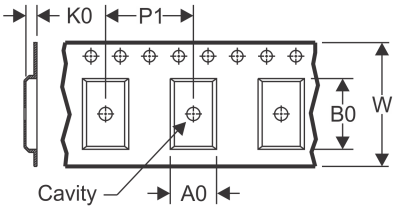
TAPE AND REEL INFORMATION

REEL DIMENSIONS

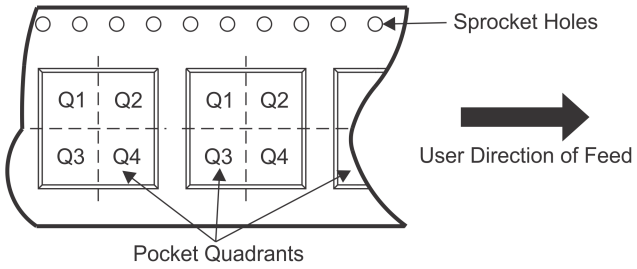


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

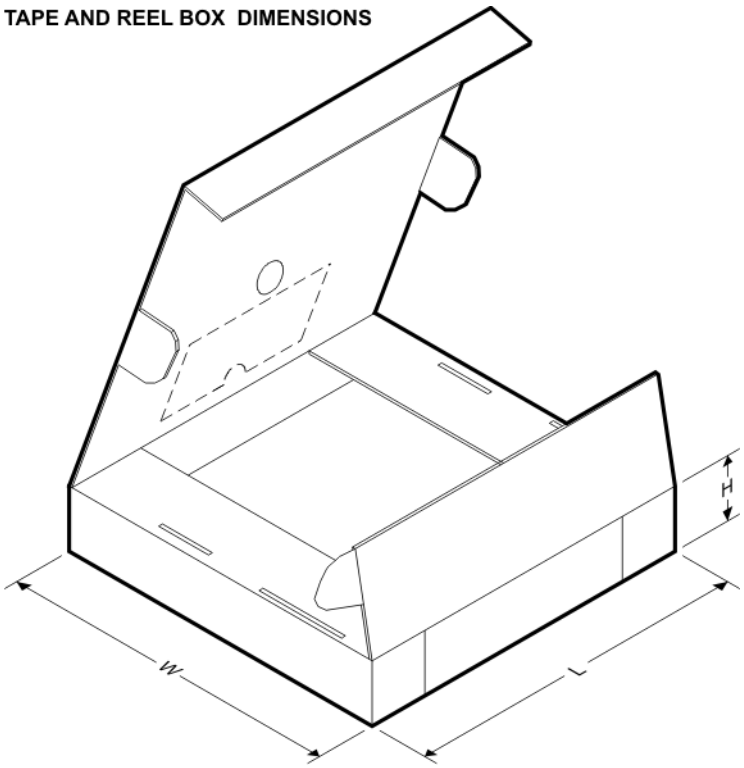
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83867CSRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
DP83867CSRGZT	VQFN	RGZ	48	250	178.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
DP83867ERGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
DP83867ERGZT	VQFN	RGZ	48	250	178.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
DP83867ISRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
DP83867ISRGZT	VQFN	RGZ	48	250	178.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83867CSRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
DP83867CSRGZT	VQFN	RGZ	48	250	208.0	191.0	35.0
DP83867ERGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
DP83867ERGZT	VQFN	RGZ	48	250	208.0	191.0	35.0
DP83867ISRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
DP83867ISRGZT	VQFN	RGZ	48	250	208.0	191.0	35.0

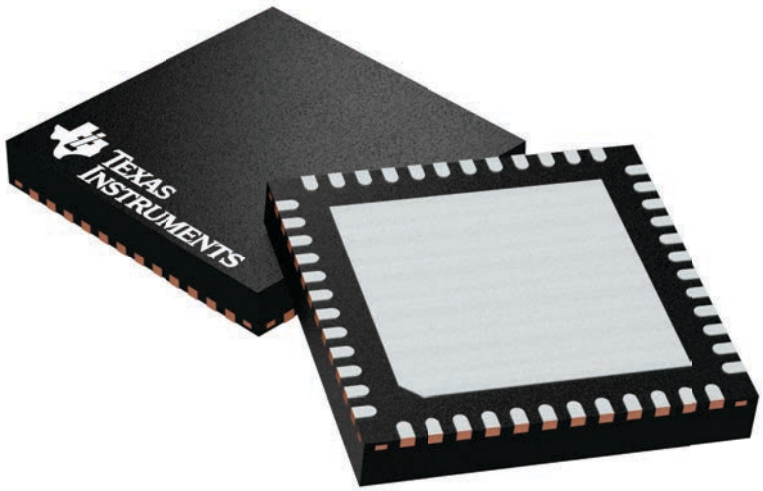
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

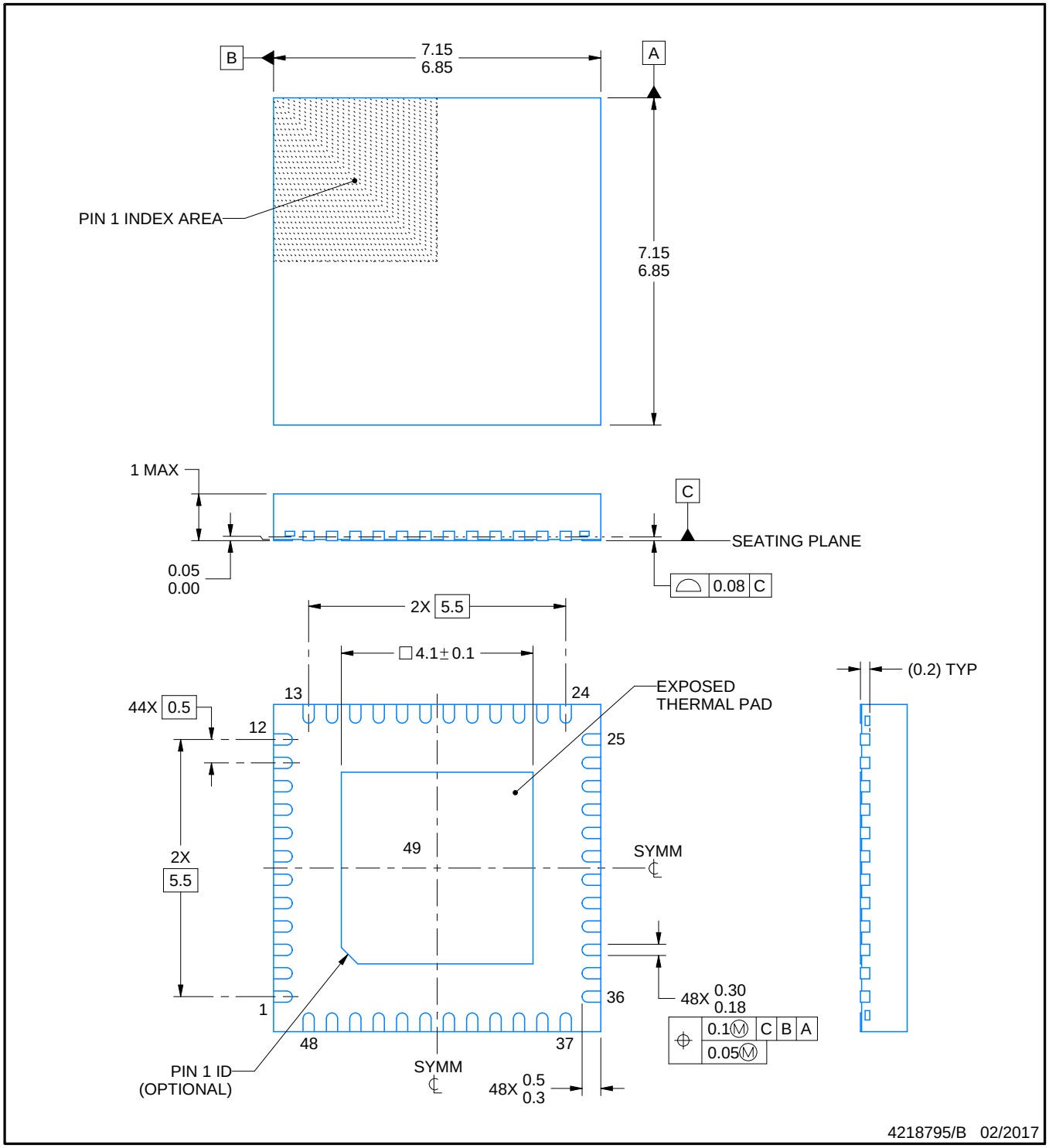
4224671/A

RGZ0048B

PACKAGE OUTLINE

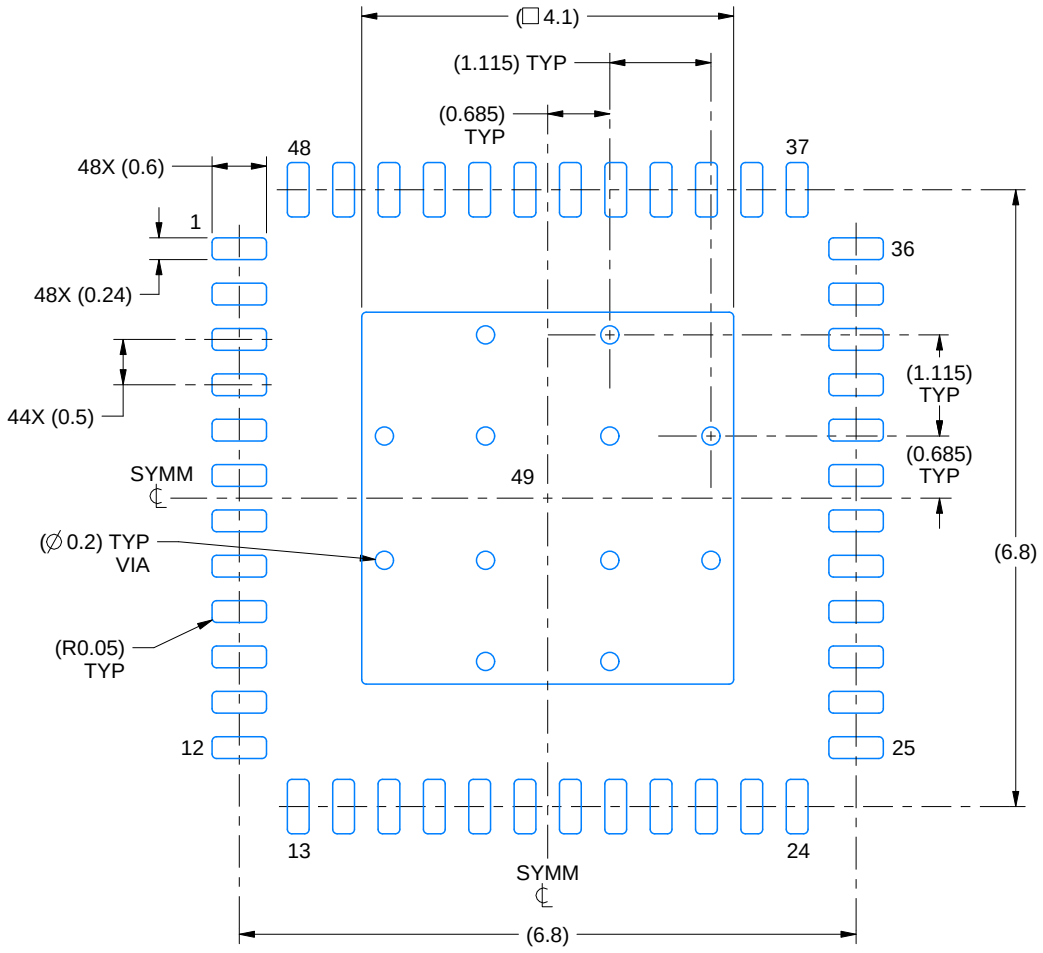
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

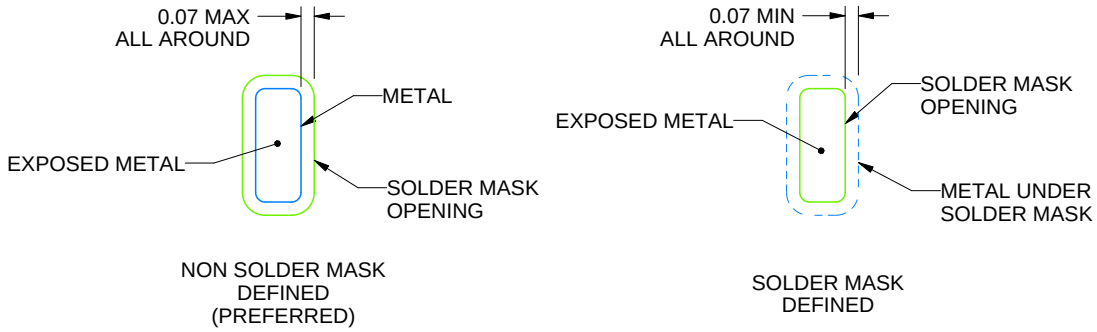


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

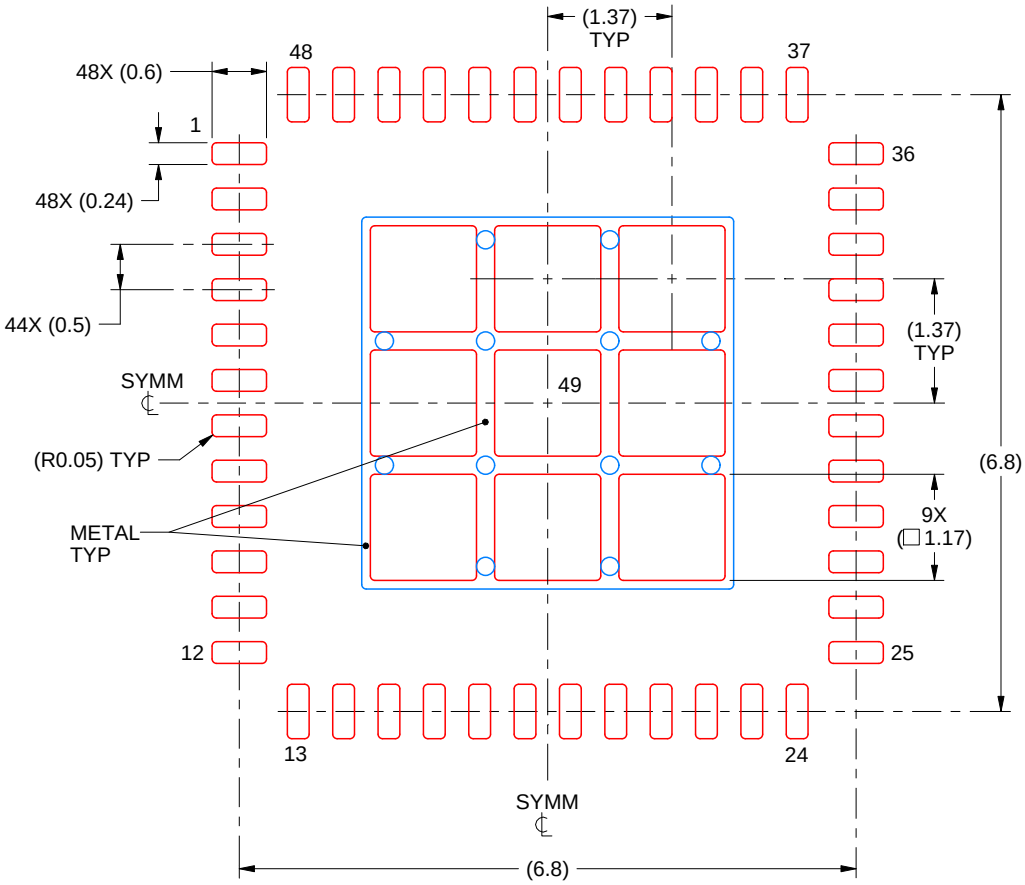


SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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