





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**PACKAGING/ORDERING INFORMATION<sup>(1)</sup>**

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM GAIN ERROR (% OF FSR)	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8551	±8	±1	±0.15	MSOP-8	DGK	-40°C to +105°C	D81	DAC8551DGK	Tube, 80
								DAC8551DGKT	Tape and Reel, 250
								DAC8551DGKR	Tape and Reel, 2500
DAC8551A	±12	±1	±0.2	MSOP-8	DGK	-40°C to +105°C	D81	DAC8551ADGK	Tube, 80
								DAC8551ADGKT	Tape and Reel, 250
								DAC8551ADGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

	UNIT	
V <sub>DD</sub> to GND	-0.3V to 6V	
Digital input voltage to GND	-0.3V to +V <sub>DD</sub> + 0.3V	
V <sub>OUT</sub> to GND	-0.3V to +V <sub>DD</sub> + 0.3V	
Operating temperature range	-40°C to +105°C	
Storage temperature range	-65°C to +150°C	
Junction temperature range (T <sub>J</sub> max)	+150°C	
Power dissipation (DGK)	(T <sub>J</sub> max - T <sub>A</sub> )/θ <sub>JA</sub>	
Thermal impedance	θ <sub>JA</sub>	206°C/W
	θ <sub>JC</sub>	44°C/W

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS**

V<sub>DD</sub> = 2.7V to 5.5V, and -40°C to +105°C range, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC PERFORMANCE<sup>(1)</sup></b>					
Resolution		16			Bits
Relative accuracy	Measured by line passing through codes 485 and 64741	DAC8551	±3	±8	LSB
		DAC8551A	±3	±12	LSB
Differential nonlinearity	16-bit monotonic		±0.25	±1	LSB
Zero-code error	Measured by line passing through codes 485 and 64741		±2	±12	mV
Full-scale error			±0.05	±0.5	% of FSR
Gain error	Measured by line passing through codes 485 and 64741	DAC8551	±0.02	±0.15	% of FSR
		DAC8551A	±0.02	±0.2	% of FSR
Zero-code error drift			±5		µV/°C
Gain temperature coefficient			±1		ppm of FSR/°C
PSRR Power-supply rejection ratio	R <sub>L</sub> = 2kΩ, C <sub>L</sub> = 200pF		0.75		mV/V

(1) Linearity calculated using a reduced code range of 485 to 64741; output unloaded.

**ELECTRICAL CHARACTERISTICS (continued)**

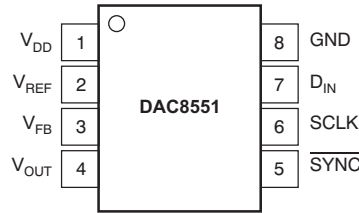
$V_{DD} = 2.7V$  to  $5.5V$ , and  $-40^{\circ}C$  to  $+105^{\circ}C$  range, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT CHARACTERISTICS (2)</b>					
Output voltage range		0		$V_{REF}$	V
Output voltage settling time	$T_0 \pm 0.003\%$ FSR, 0200h to FD00h, $R_L = 2k\Omega$ , $0pF < C_L < 200pF$		8	10	$\mu s$
	$R_L = 2k\Omega$ , $C_L = 50 pF$		12		$\mu s$
Slew rate			1.8		V/ $\mu s$
Capacitive load stability	$R_L = \infty$		470		pF
	$R_L = 2k\Omega$		1000		pF
Code change glitch impulse	1LSB change around major carry		0.1		nV-s
Digital feedthrough	50k $\Omega$ series resistance on digital lines		0.1		
DC output impedance	At mid-code input		1		$\Omega$
Short-circuit current	$V_{DD} = 5V$		50		mA
	$V_{DD} = 3V$		20		
Power-up time	Coming out of power-down mode, $V_{DD} = 5V$		2.5		$\mu s$
	Coming out of power-down mode, $V_{DD} = 3V$		5		
<b>AC PERFORMANCE</b>					
SNR	BW = 20kHz, $V_{DD} = 5V$ , $f_{OUT} = 1kHz$ , 1st 19 harmonics removed for SNR calculation		95		dB
THD			-85		
SFDR			87		
SINAD			84		
<b>REFERENCE INPUT</b>					
Reference current	$V_{REF} = V_{DD} = 5V$		40	75	$\mu A$
	$V_{REF} = V_{DD} = 3.6V$		30	45	$\mu A$
Reference input range		0		$V_{DD}$	V
Reference input impedance			125		k $\Omega$
<b>LOGIC INPUTS (2)</b>					
Input current			$\pm 1$		$\mu A$
$V_{INL}$ Input LOW voltage	$V_{DD} = 5V$			0.8	V
	$V_{DD} = 3V$			0.6	
$V_{INH}$ Input HIGH voltage	$V_{DD} = 5V$	2.4			V
	$V_{DD} = 3V$	2.1			
Pin capacitance				3	pF
<b>POWER REQUIREMENTS</b>					
$V_{DD}$		2.7		5.5	V
$I_{DD}$ (normal mode)	Input code = 32768, no load, does not include reference current				
$V_{DD} = 3.6V$ to $5.5V$	$V_{IH} = V_{DD}$ and $V_{IL} = GND$		160	250	$\mu A$
		$V_{DD} = 2.7V$ to $3.6V$	140	240	
$I_{DD}$ (all power-down modes)	$V_{IH} = V_{DD}$ and $V_{IL} = GND$		0.2	2	$\mu A$
		$V_{DD} = 2.7V$ to $3.6V$	0.05	2	
<b>POWER EFFICIENCY</b>					
$I_{OUT}/I_{DD}$	$I_{LOAD} = 2mA$ , $V_{DD} = 5V$		89		%
<b>TEMPERATURE RANGE</b>					
Specified performance		-40		+105	$^{\circ}C$

(2) Specified by design and characterization; not production tested.

**PIN CONFIGURATION**

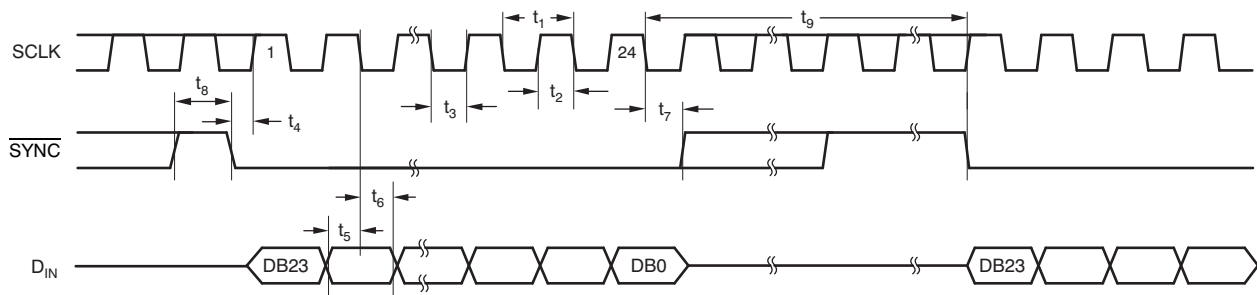
DGK PACKAGE  
MSOP-8  
(Top View)



**PIN DESCRIPTIONS**

PIN	NAME	DESCRIPTION
1	V <sub>DD</sub>	Power supply input, 2.7V to 5.5V.
2	V <sub>REF</sub>	Reference voltage input.
3	V <sub>FB</sub>	Feedback connection for the output amplifier. For voltage output operation, tie to V <sub>OUT</sub> externally.
4	V <sub>OUT</sub>	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{\text{SYNC}}$	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock (unless $\overline{\text{SYNC}}$ is taken HIGH before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the DAC8551). Schmitt-Trigger logic input.
6	SCLK	Serial clock input. Data can be transferred at rates up to 30MHz. Schmitt-Trigger logic input.
7	D <sub>IN</sub>	Serial data input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
8	GND	Ground reference point for all circuitry on the part.

## SERIAL WRITE OPERATION



## TIMING CHARACTERISTICS<sup>(1)(2)</sup>

$V_{DD} = 2.7V$  to  $5.5V$ , all specifications  $-40^{\circ}C$  to  $+105^{\circ}C$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_1^{(3)}$ SCLK cycle time	$V_{DD} = 2.7V$ to $3.6V$	50			ns
	$V_{DD} = 3.6V$ to $5.5V$	33			
$t_2$ SCLK HIGH time	$V_{DD} = 2.7V$ to $3.6V$	13			ns
	$V_{DD} = 3.6V$ to $5.5V$	13			
$t_3$ SCLK LOW time	$V_{DD} = 2.7V$ to $3.6V$	22.5			ns
	$V_{DD} = 3.6V$ to $5.5V$	13			
$t_4$ $\overline{SYNC}$ to SCLK rising edge setup time	$V_{DD} = 2.7V$ to $3.6V$	0			ns
	$V_{DD} = 3.6V$ to $5.5V$	0			
$t_5$ Data setup time	$V_{DD} = 2.7V$ to $3.6V$	5			ns
	$V_{DD} = 3.6V$ to $5.5V$	5			
$t_6$ Data hold time	$V_{DD} = 2.7V$ to $3.6V$	4.5			ns
	$V_{DD} = 3.6V$ to $5.5V$	4.5			
$t_7$ 24th SCLK falling edge to $\overline{SYNC}$ rising edge	$V_{DD} = 2.7V$ to $3.6V$	0			ns
	$V_{DD} = 3.6V$ to $5.5V$	0			
$t_8$ Minimum $\overline{SYNC}$ HIGH time	$V_{DD} = 2.7V$ to $3.6V$	50			ns
	$V_{DD} = 3.6V$ to $5.5V$	33			
$t_9$ 24th SCLK falling edge to $\overline{SYNC}$ falling edge	$V_{DD} = 2.7V$ to $5.5V$	100			ns

(1) All input signals are specified with  $t_R = t_F = 5ns$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

(2) See [Serial Write Operation Timing Diagram](#).

(3) Maximum SCLK frequency is 30MHz at  $V_{DD} = 3.6V$  to  $5.5V$  and 20MHz at  $V_{DD} = 2.7V$  to  $3.6V$ .

**TYPICAL CHARACTERISTICS:  $V_{DD} = 5\text{ V}$**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

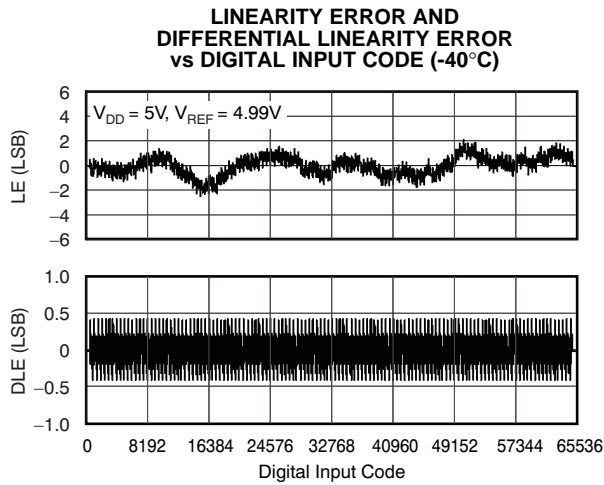


Figure 1.

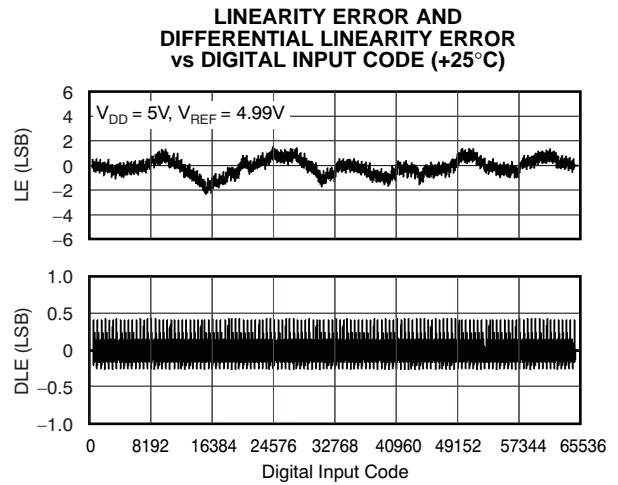


Figure 2.

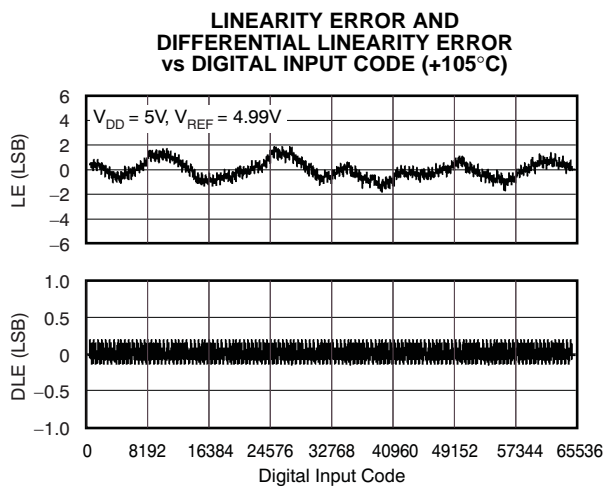


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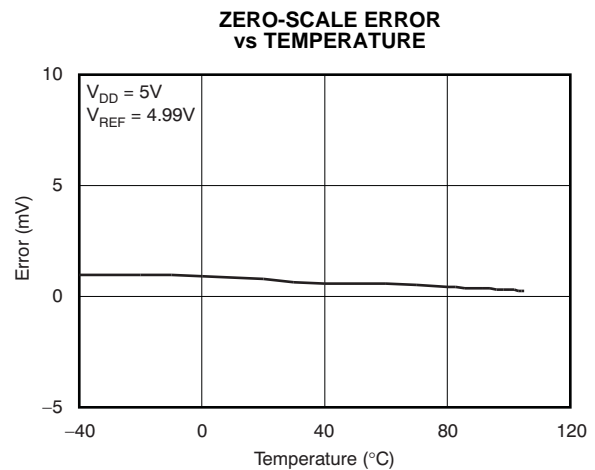


Figure 4.

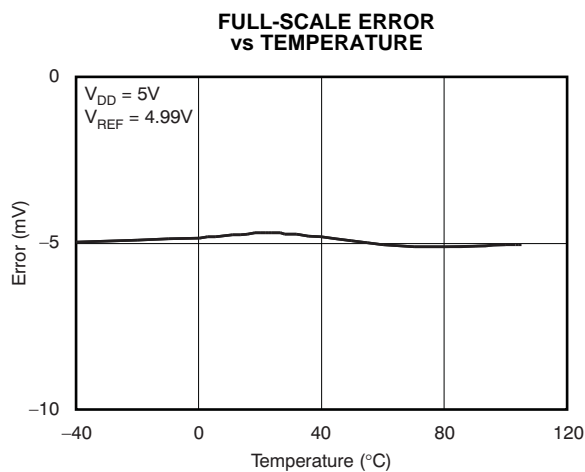


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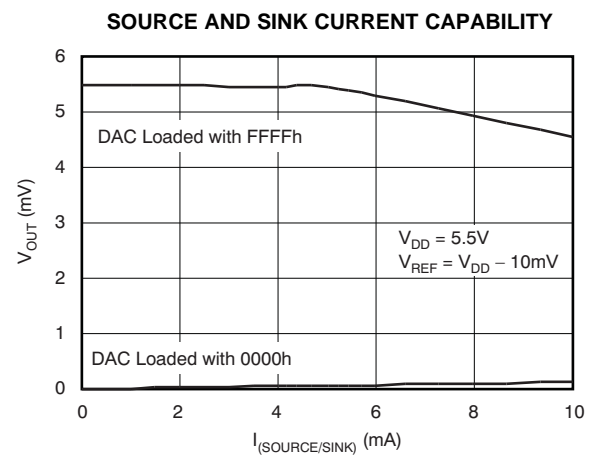


Figure 6.

**TYPICAL CHARACTERISTICS:  $V_{DD} = 5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

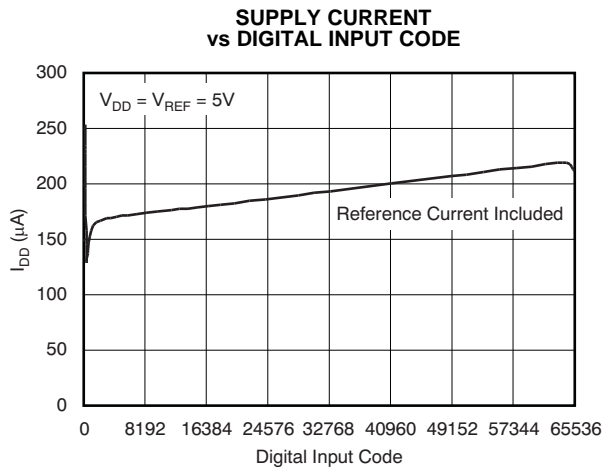


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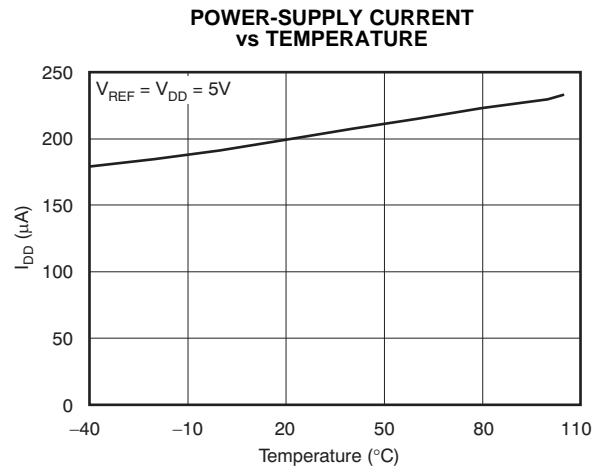


Figure 8.

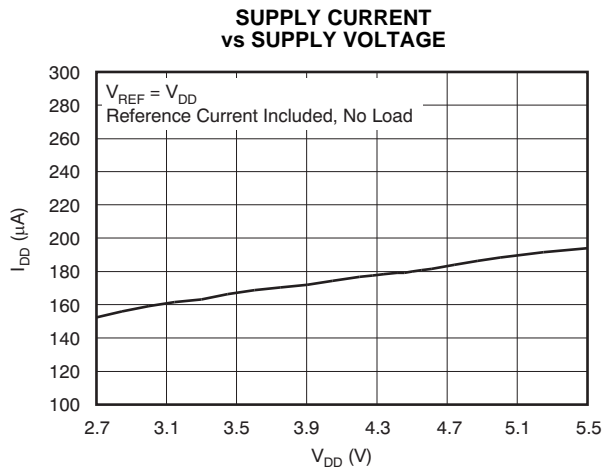


Figure 9.

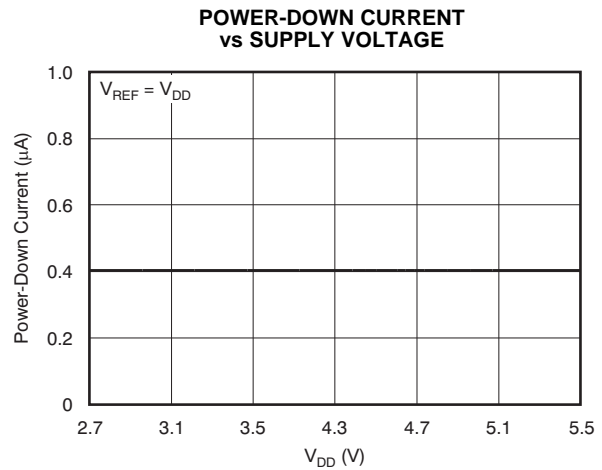


Figure 10.

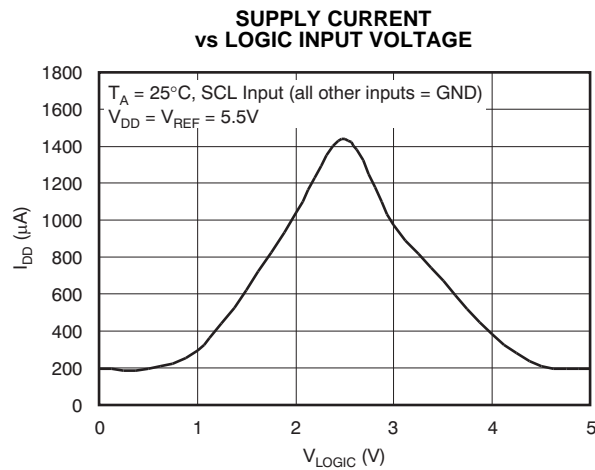


Figure 11.

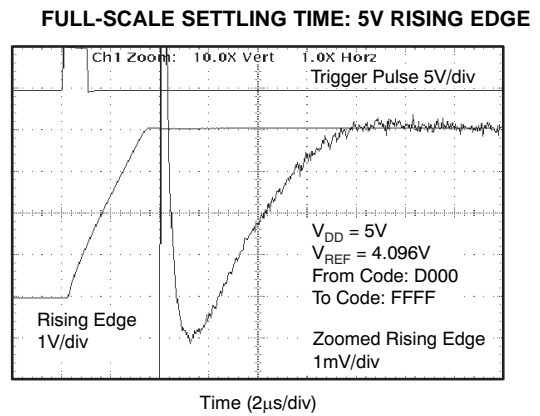
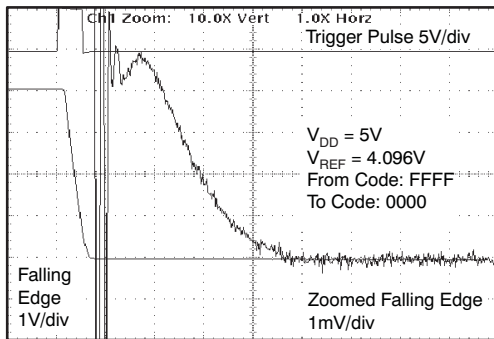


Figure 12.

**TYPICAL CHARACTERISTICS:  $V_{DD} = 5\text{ V}$  (continued)**

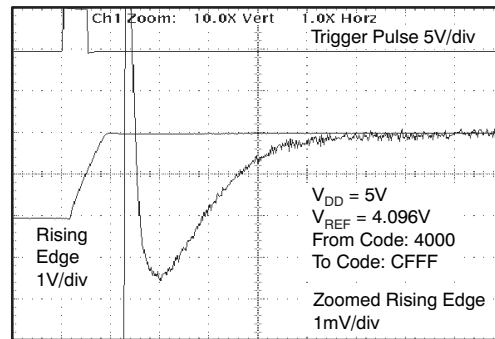
At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

**FULL-SCALE SETTLING TIME: 5V FALLING EDGE**



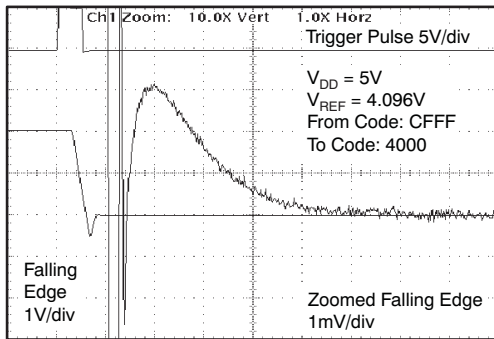
**Figure 13.**

**HALF-SCALE SETTLING TIME: 5V RISING EDGE**



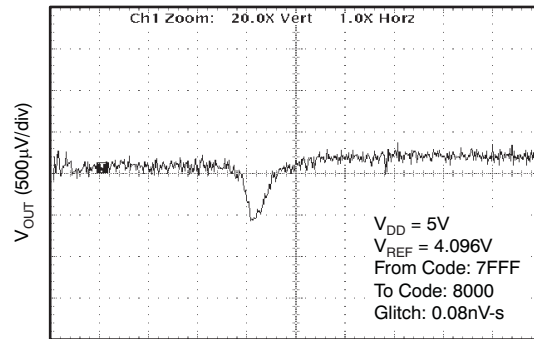
**Figure 14.**

**HALF-SCALE SETTLING TIME: 5V FALLING EDGE**



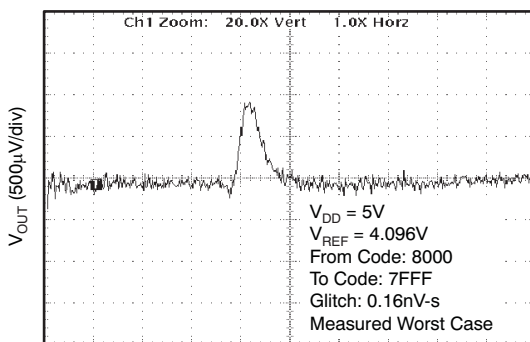
**Figure 15.**

**GLITCH ENERGY: 5V, 1LSB STEP, RISING EDGE**



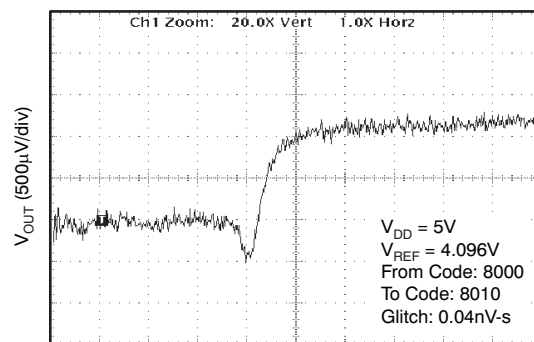
**Figure 16.**

**GLITCH ENERGY: 5V, 1LSB STEP, FALLING EDGE**



**Figure 17.**

**GLITCH ENERGY: 5V, 16LSB STEP, RISING EDGE**

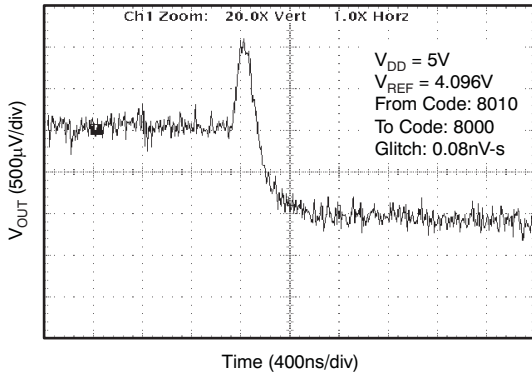


**Figure 18.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = 5\text{ V}$  (continued)**

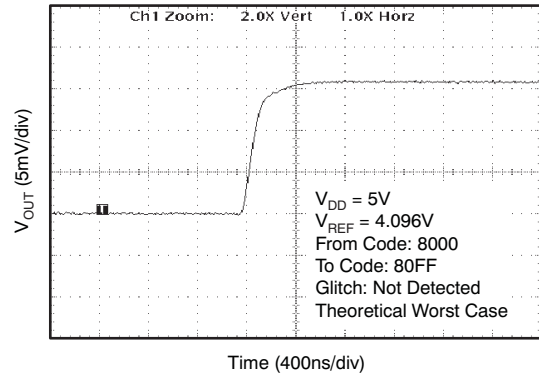
At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

**GLITCH ENERGY: 5V, 16LSB STEP, FALLING EDGE**



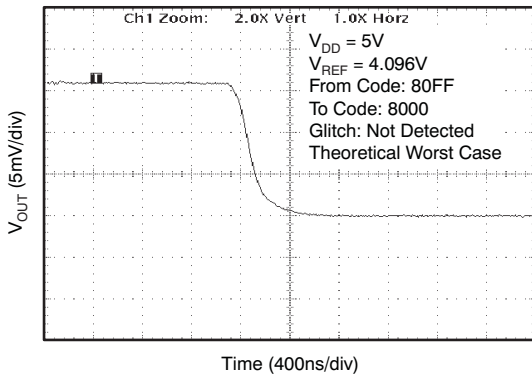
**Figure 19.**

**GLITCH ENERGY: 5V, 256LSB STEP, RISING EDGE**



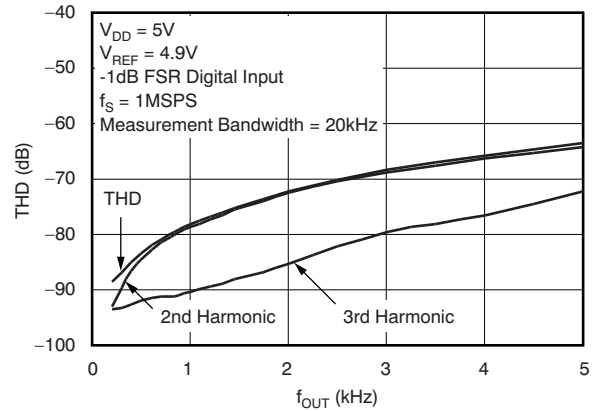
**Figure 20.**

**GLITCH ENERGY: 5V, 256LSB STEP, FALLING EDGE**



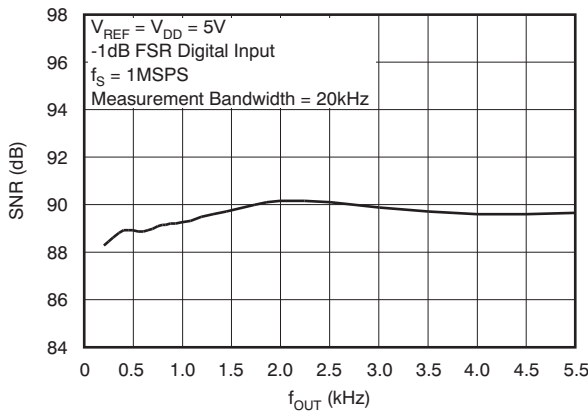
**Figure 21.**

**TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY**



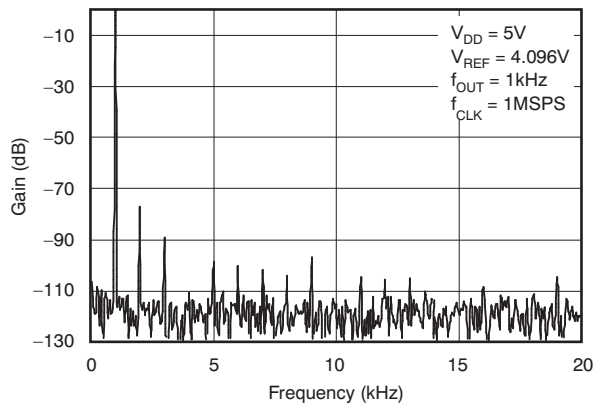
**Figure 22.**

**SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY**

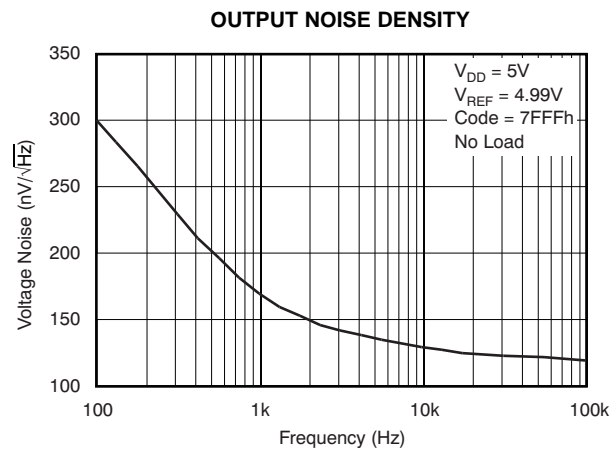


**Figure 23.**

**POWER SPECTRAL DENSITY**



**Figure 24.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = 5\text{ V}$  (continued)**At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

**TYPICAL CHARACTERISTICS:  $V_{DD} = 2.7\text{ V}$**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

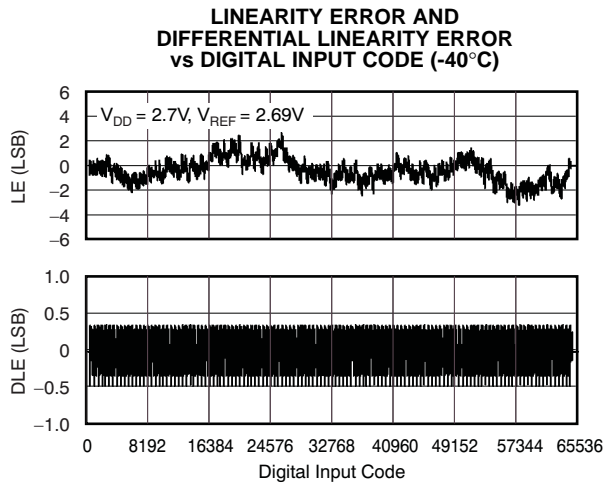


Figure 26.

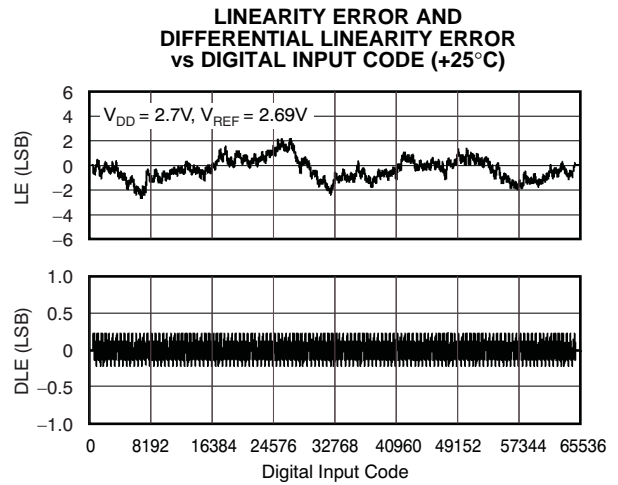


Figure 27.

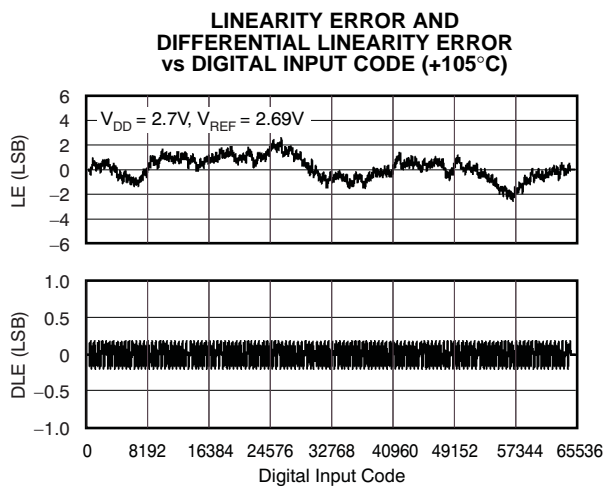


Figure 28.

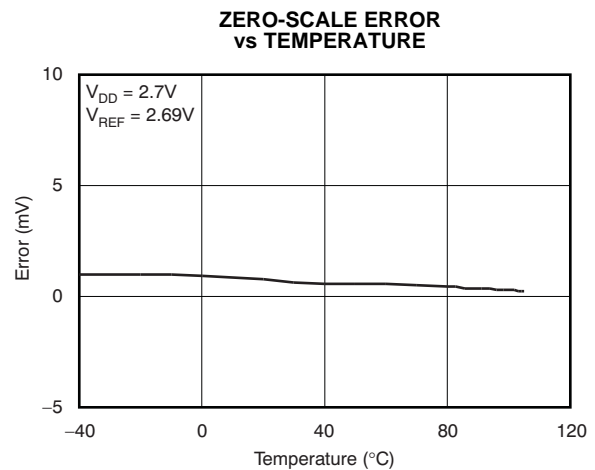


Figure 29.

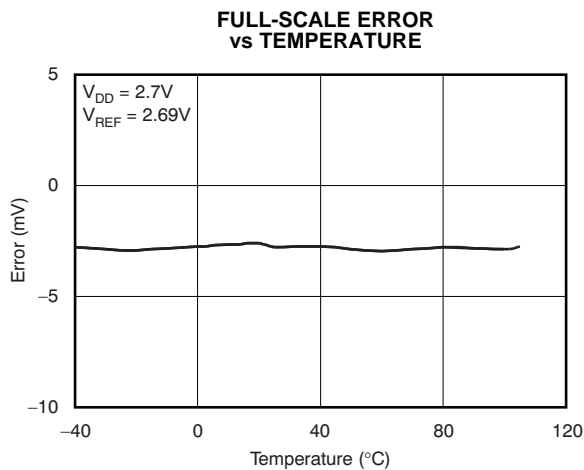


Figure 30.

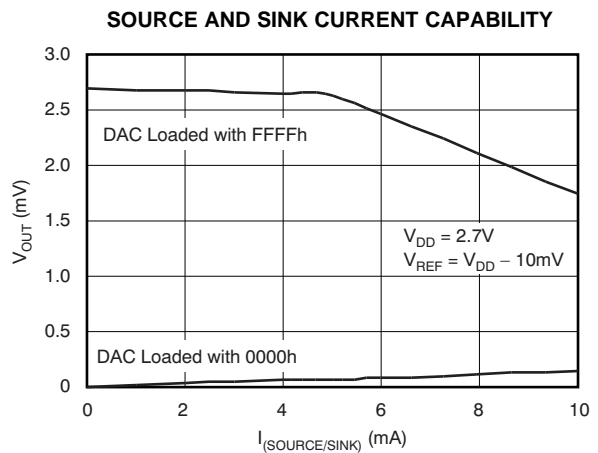


Figure 31.

**TYPICAL CHARACTERISTICS:  $V_{DD} = 2.7\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

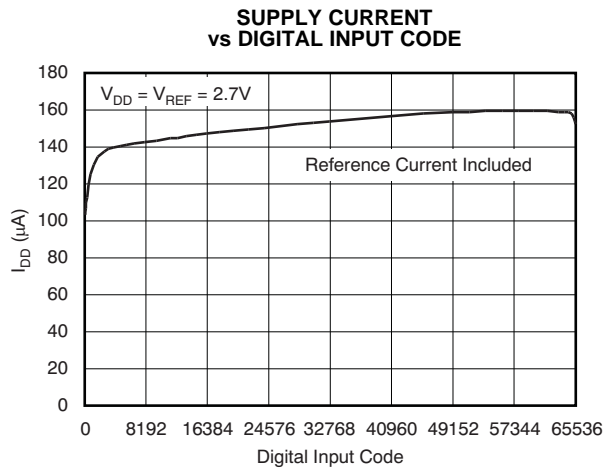


Figure 32.

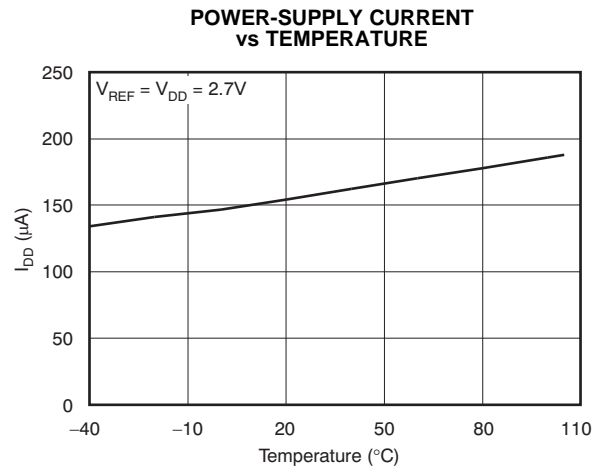


Figure 33.

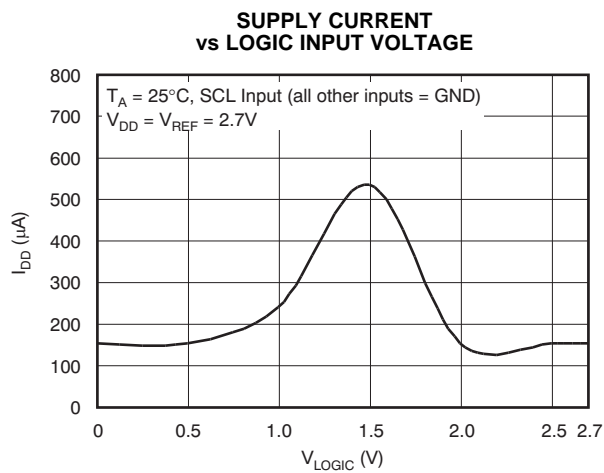


Figure 34.

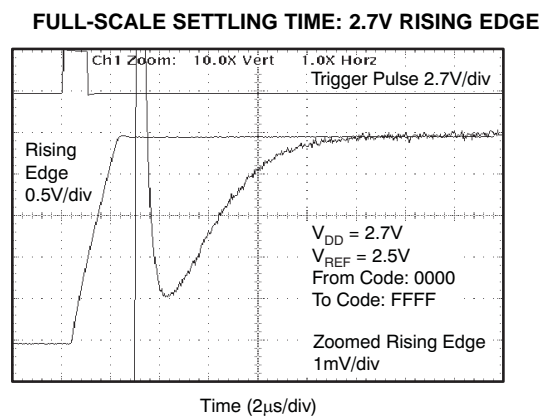


Figure 35.

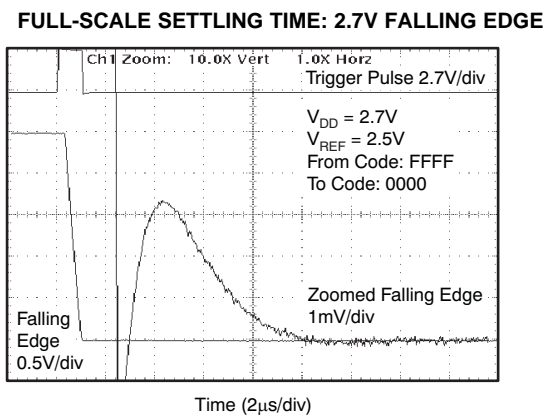


Figure 36.

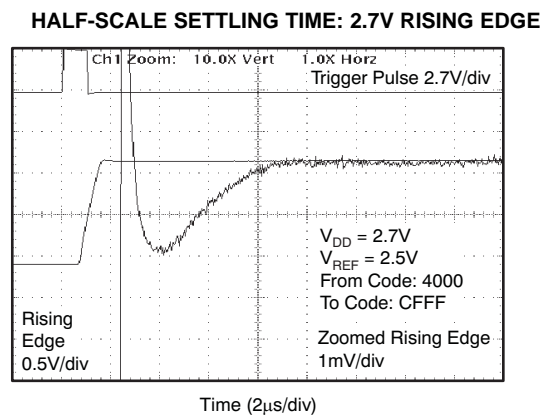
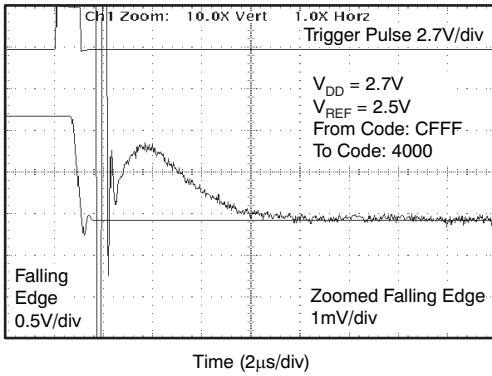


Figure 37.

**TYPICAL CHARACTERISTICS:  $V_{DD} = 2.7\text{ V}$  (continued)**

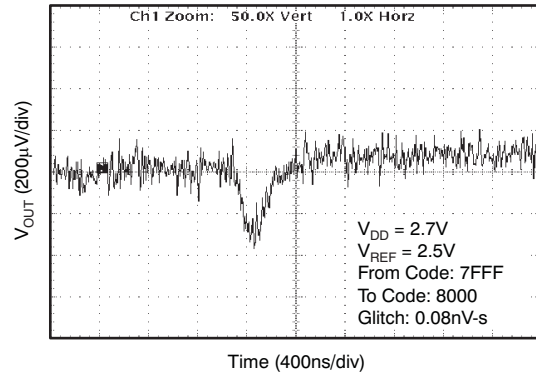
At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

**HALF-SCALE SETTLING TIME: 2.7V FALLING EDGE**



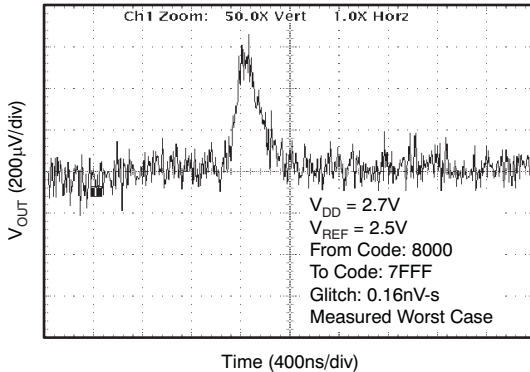
**Figure 38.**

**GLITCH ENERGY: 2.7V, 1LSB STEP, RISING EDGE**



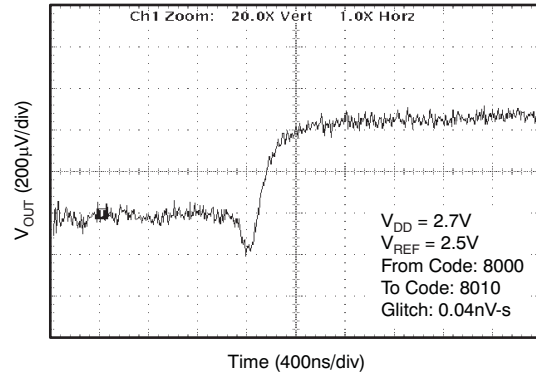
**Figure 39.**

**GLITCH ENERGY: 2.7V, 1LSB STEP, FALLING EDGE**



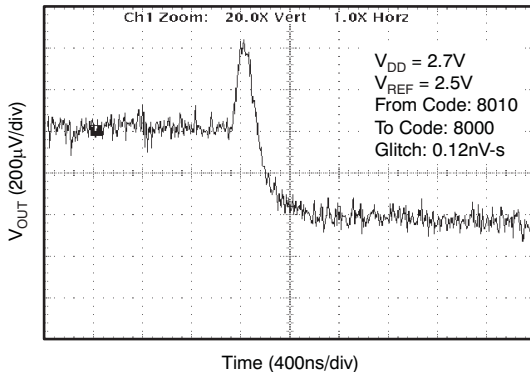
**Figure 40.**

**GLITCH ENERGY: 2.7V, 16LSB STEP, RISING EDGE**



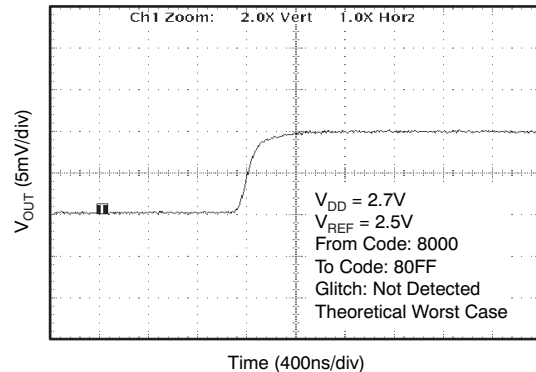
**Figure 41.**

**GLITCH ENERGY: 2.7V, 16LSB STEP, FALLING EDGE**



**Figure 42.**

**GLITCH ENERGY: 2.7V, 256LSB STEP, RISING EDGE**

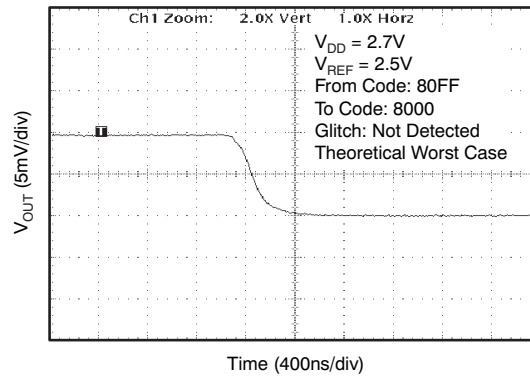


**Figure 43.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = 2.7\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

**GLITCH ENERGY: 2.7V, 256LSB STEP, FALLING EDGE**

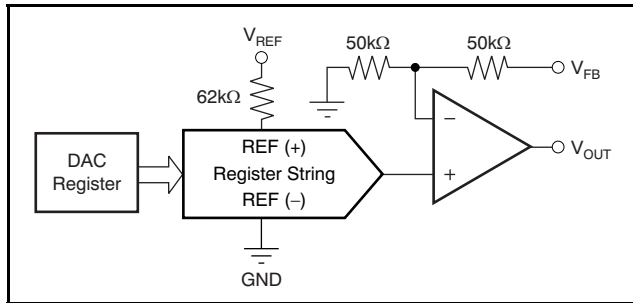


**Figure 44.**

## THEORY OF OPERATION

### DAC SECTION

The DAC8551 architecture consists of a string DAC followed by an output buffer amplifier. Figure 45 shows a block diagram of the DAC architecture.



**Figure 45. DAC8551 Architecture**

The input coding to the DAC8551 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = \frac{D_{IN}}{65536} \times V_{REF} \quad (1)$$

where  $D_{IN}$  = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

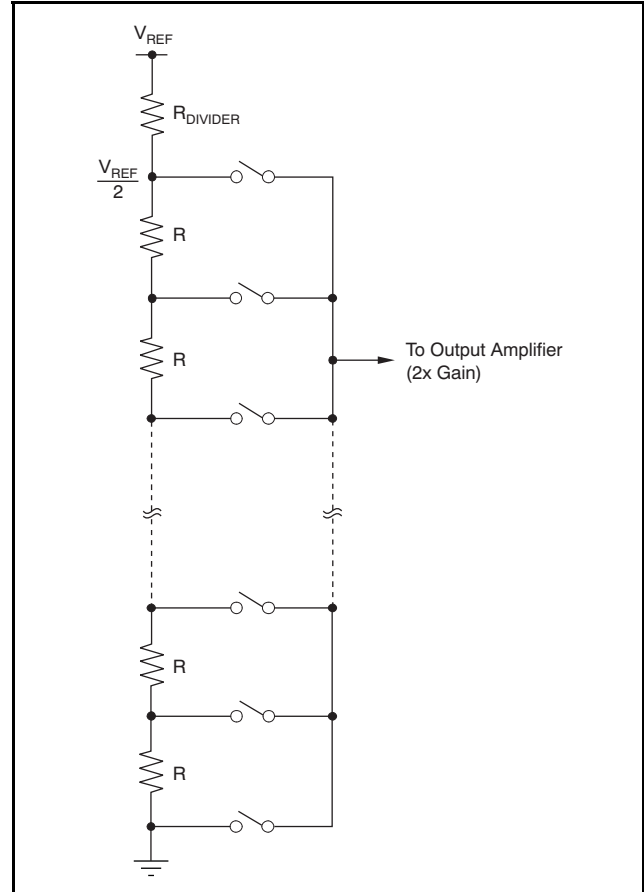
### RESISTOR STRING

The resistor string section is shown in Figure 46. It is simply a string of resistors, each of value  $R$ . The code loaded into the DAC register determines at which node on the string the voltage is tapped off by closing one of the switches connecting the string to the amplifier. Monotonicity is ensured because of the string resistor architecture.

### OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to  $V_{DD}$ . It is capable of driving a load of  $2k\Omega$  in parallel with  $1000pF$  to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is  $1.8V/\mu s$  with a full-scale setting time of  $8\mu s$  with the output unloaded.

The inverting input of the output amplifier is brought out to the  $V_{FB}$  pin. This configuration allows for better accuracy in critical applications by tying the  $V_{FB}$  point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.



**Figure 46. Resistor String**

### SERIAL INTERFACE

The DAC8551 has a 3-wire serial interface ( $\overline{SYNC}$ , SCLK, and  $D_{IN}$ ), which is compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation Timing Diagram for an example of a typical write sequence.

The write sequence begins by bringing the  $\overline{SYNC}$  line LOW. Data from the  $D_{IN}$  line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC8551 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed (that is, a change in DAC register contents and/or a change in the mode of operation).

At this point, the  $\overline{\text{SYNC}}$  line may be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of 33ns before the next write sequence so that a falling edge of  $\overline{\text{SYNC}}$  can initiate the next write sequence. As previously mentioned, it must be brought HIGH again just before the next write sequence.

### INPUT SHIFT REGISTER

The input shift register is 24 bits wide, as shown in Figure 47. The first six bits are *don't care* bits. The next two bits (PD1 and PD0) are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). A more complete description of the various modes is located in the Power-Down Modes section. The next 16 bits are the data bits. These bits are transferred to the DAC register on the 24th falling edge of SCLK.

### SYNC INTERRUPT

In a normal write sequence, the  $\overline{\text{SYNC}}$  line is kept LOW for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if  $\overline{\text{SYNC}}$  is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 48.

### POWER-ON RESET

The DAC8551 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC registers are filled with zeros and the output voltages are 0V; they remain that way until a valid write sequence is made to the DAC. The power-on reset is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

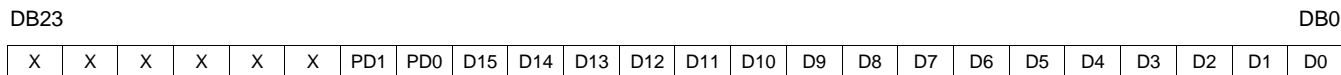


Figure 47. DAC8551 Data Input Register Format

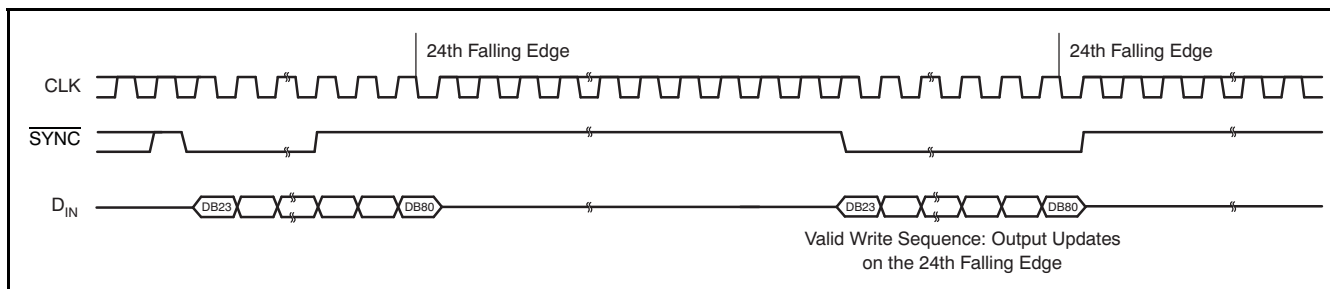


Figure 48.  $\overline{\text{SYNC}}$  Interrupt Facility

## POWER-DOWN MODES

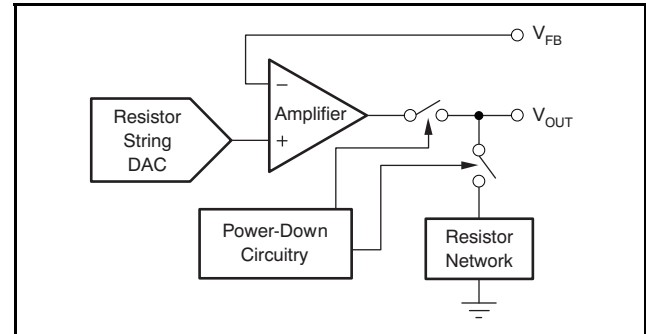
The DAC8551 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 1 shows how the state of the bits corresponds to the mode of operation of the device.

**Table 1. Operating Modes**

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal operation
–	–	Power-down modes
0	1	Output typically 1kΩ to GND
1	0	Output typically 100kΩ to GND
1	1	High-Z

When both bits are set to '0', the device works normally with its typical current consumption of 200μA at 5V. However, for the three power-down modes, the supply current falls to 200nA at 5V (50nA at 3V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This configuration has the advantage that the output impedance of the device is known while it is in

power-down mode. There are three different options. The output is connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 49.



**Figure 49. Output Stage During Power-Down**

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5μs for  $V_{DD} = 5V$ , and 5μs for  $V_{DD} = 3V$ . See the [Typical Characteristics](#) for more information.

## MICROPROCESSOR INTERFACING

### DAC8551 to 8051 Interface

See [Figure 50](#) for a serial interface between the DAC8551 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8551, while RXD drives the serial data line of the device. The  $\overline{\text{SYNC}}$  signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data are to be transmitted to the DAC8551, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The DAC8551 requires data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed.

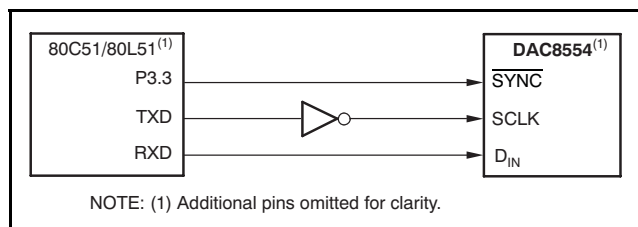


Figure 50. DAC8551 to 80C51/80L51 Interface

### DAC8551 to Microwire Interface

[Figure 51](#) shows an interface between the DAC8551 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and is clocked into the DAC8551 on the rising edge of the SK signal.

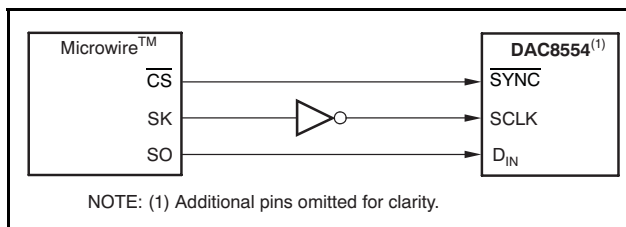


Figure 51. DAC8551 to Microwire Interface

### DAC8551 to 68HC11 Interface

[Figure 52](#) shows a serial interface between the DAC8551 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8551, while the MOSI output drives the serial data line of the DAC. The  $\overline{\text{SYNC}}$  signal is derived from a port line (PC7), similar to the 8051 diagram.

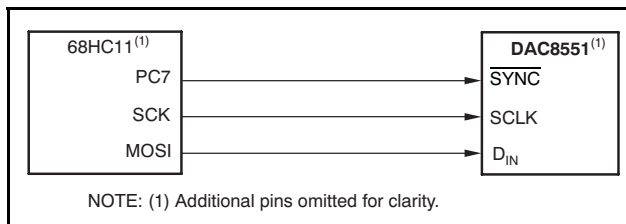


Figure 52. DAC8551 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the  $\overline{\text{SYNC}}$  line is held LOW (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC8551, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation are performed to the DAC. PC7 is taken HIGH at the end of this procedure.

## APPLICATION INFORMATION

### USING THE REF02 AS A POWER SUPPLY FOR THE DAC8551

Due to the extremely low supply current required by the DAC8551, an alternative option is to use the REF02 (+5 V precision voltage reference) to supply the required voltage to the device, as illustrated in Figure 53.

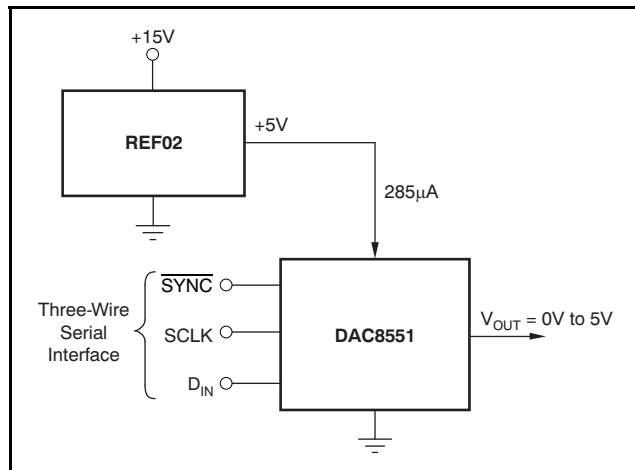


Figure 53. REF02 as a Power Supply to the DAC8551

This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 outputs a steady supply voltage for the DAC8551. If the REF02 is used, the current it needs to supply to the DAC8551 is 200µA. This configuration is with no load on the output of the DAC. When a DAC output is loaded, the REF02 also needs to supply the current to the load.

The total typical current required (with a 5kΩ load on the DAC output) is:

$$200\mu\text{A} + \frac{5\text{V}}{5\text{k}\Omega} = 1.2\text{mA} \quad (2)$$

The load regulation of the REF02 is typically 0.005%/mA, resulting in an error of 299µV for the 1.2mA current drawn from it. This value corresponds to a 3.9LSB error.

### BIPOLAR OPERATION USING THE DAC8551

The DAC8551 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 54. The circuit shown gives an output voltage range of  $\pm V_{\text{REF}}$ . Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_o = \left[ V_{\text{REF}} \times \left( \frac{D}{65536} \right) \times \left( \frac{R_1 + R_2}{R_1} \right) - V_{\text{REF}} \times \left( \frac{R_2}{R_1} \right) \right] \quad (3)$$

where D represents the input code in decimal (0–65535).

With  $V_{\text{REF}} = 5\text{V}$ ,  $R_1 = R_2 = 10\text{k}\Omega$ .

$$V_o = \left( \frac{10 \times D}{65536} \right) - 5\text{V} \quad (4)$$

Using this example, an output voltage range of  $\pm 5\text{V}$  with 0000h corresponding to a  $-5\text{V}$  output and FFFFh corresponding to a  $5\text{V}$  output can be achieved. Similarly, using  $V_{\text{REF}} = 2.5\text{V}$ , a  $\pm 2.5\text{V}$  output voltage range can be achieved.

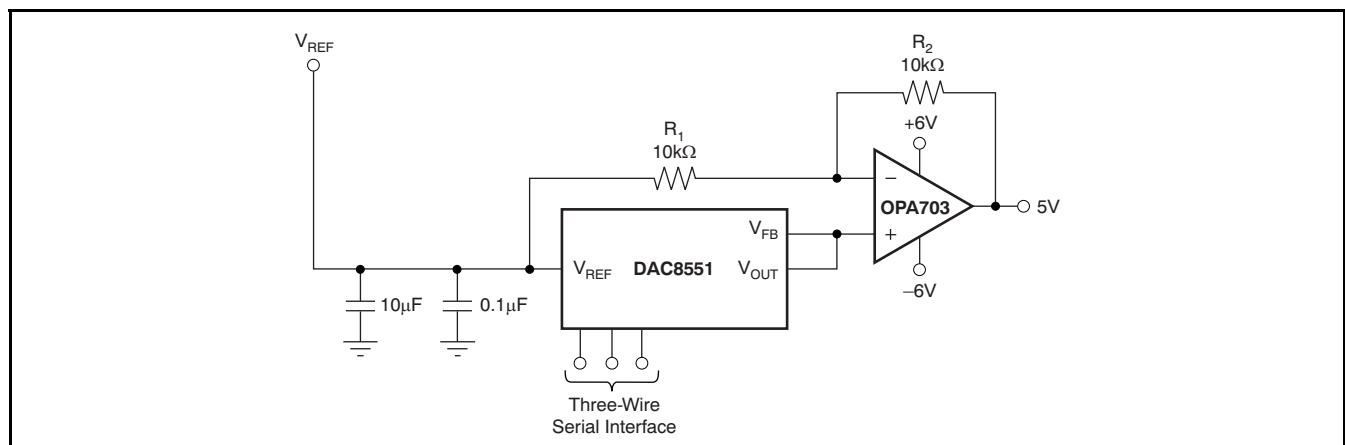


Figure 54. Bipolar Output Range

## LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8551 offers single-supply operation, and it often is used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8551, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to  $V_{DD}$  should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection,  $V_{DD}$  should be connected to a 5V power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1 $\mu$ F to 10 $\mu$ F capacitor and 0.1 $\mu$ F bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100 $\mu$ F electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5V supply, removing the high-frequency noise.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8551IADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D81	<a href="#">Samples</a>
DAC8551IADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D81	<a href="#">Samples</a>
DAC8551IADGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D81	<a href="#">Samples</a>
DAC8551IADGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D81	<a href="#">Samples</a>
DAC8551IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D81	<a href="#">Samples</a>
DAC8551IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D81	<a href="#">Samples</a>
DAC8551IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D81	<a href="#">Samples</a>
DAC8551IDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D81	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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\*All dimensions are nominal

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DAC8551IADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8551IADGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8551IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8551IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8551IADGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
DAC8551IADGKT	VSSOP	DGK	8	250	367.0	367.0	35.0
DAC8551IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
DAC8551IDGKT	VSSOP	DGK	8	250	367.0	367.0	35.0



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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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