12-Bit, Serial Input, Multiplying Digital-to-Analog Converter

FEATURES

- **2.7V to 5.5V Supply Operation**
- **50MHz Serial Interface**
- **10MHz Multiplying Bandwidth**
- **±15V Reference Input**
- **Low Glitch Energy: 5nV-s**
- **Extended Temperature Range: –40°C to +125°C**
- **10-Lead MSOP Package**
- **12-Bit Monotonic**
- **4-Quadrant Multiplication**
- **Power-On Reset with Brownout Detection**
- **Daisy-Chain Mode**
- **Readback Function**
- **Industry-Standard Pin Configuration**

APPLICATIONS

- **Portable Battery-Powered Instruments**
- **Waveform Generators**
- **Analog Processing**
- **Programmable Amplifiers and Attenuators**
- **Digitally Controlled Calibration**
- **Programmable Filters and Oscillators**
- **Composite Video**
- **Ultrasound**

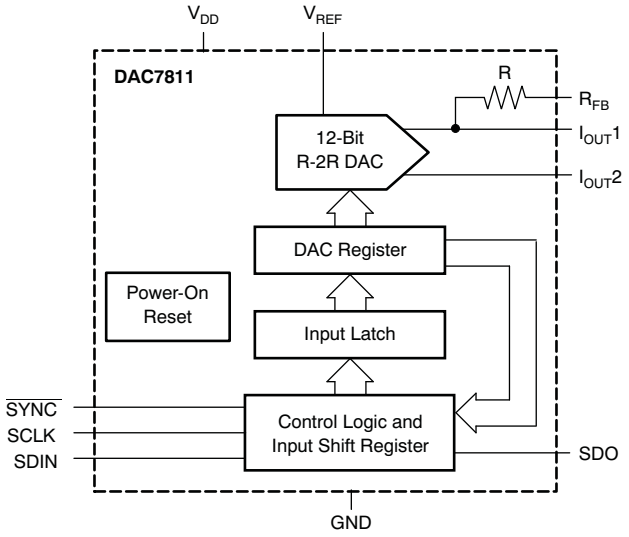
DESCRIPTION

The DAC7811 is a CMOS, 12-bit, current output digital-to-analog converter (DAC). This device operates from a 2.7V to 5.5V power supply, making it suitable for battery-powered and many other applications.

This DAC uses a double-buffered 3-wire serial interface that is compatible with SPI™, QSPI™, MICROWIRE™, and most DSP interface standards. In addition, a serial data out pin (SDO) allows for daisy-chaining when multiple devices are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with zeroes and the DAC outputs are at zero scale.

The DAC7811 offers excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidth of 10MHz. The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier.

The DAC7811 is available in a 10-lead MSOP package.



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PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	DAC7811	UNIT
V_{DD} to GND	–0.3 to +7.0	V
Digital input voltage to GND	–0.3 to V_{DD} + 0.3	V
$I_{OUT}1$, $I_{OUT}2$ to GND	–0.3 to V_{DD} + 0.3	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature (T_J max)	+150	°C
ESD Rating, HBM	2000	V
ESD Rating, CDM	1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7 V to +5.5 V; $I_{OUT}1$ = Virtual GND; $I_{OUT}2$ = 0V; V_{REF} = +10 V; T_A = full operating temperature. All specifications –40°C to +125°C, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7811			UNITS
		MIN	TYP	MAX	
STATIC PERFORMANCE					
Resolution		12			Bits
Relative accuracy				±1	LSB
Differential nonlinearity				±1	LSB
Output leakage current	Data = 0000h, T_A = +25°C			±5	nA
Output leakage current	Data = 0000h, T_A = T_{MAX}			±25	nA
Full-scale gain error	All ones loaded to DAC register		±5	±10	mV
Full-scale tempco(1)			±5		ppm/°C
Output capacitance(1)	Code dependent		5		pF

(1) Specified by design and characterization; not production tested.

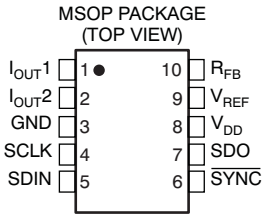
ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = +2.7 V to +5.5 V; $I_{OUT}1$ = Virtual GND; $I_{OUT}2$ = 0V; V_{REF} = +10 V; T_A = full operating temperature. All specifications –40°C to +125°C, unless otherwise noted.

PARAMETER		CONDITIONS	DAC7811 MIN	DAC7811 TYP	DAC7811 MAX	UNITS
REFERENCE INPUT						
V_{REF} range			–15		15	V
Input resistance			8	10	12	kΩ
R_{FB} resistance			8	10	12	kΩ
LOGIC INPUTS AND OUTPUT(2)						
Input low voltage	V_{IL}	V_{DD} = +2.7V			0.6	V
	V_{IL}	V_{DD} = +5V			0.8	V
Input high voltage	V_{IH}	V_{DD} = +2.7V	2.1			V
	V_{IH}	V_{DD} = +5V	2.4			V
Input leakage current	I_{IL}				10	µA
Input capacitance	C_{IL}				10	pF
INTERFACE TIMING (see Figure 28)						
Clock input frequency	f_{CLK}				50	MHz
Clock period	t_C		20			ns
Clock pulse width high	t_{CH}		8			ns
Clock pulse width low	t_{CC}		8			ns
$\overline{SYNC}$ falling edge to SCLK active edge setup time	t_{CSS}		13			ns
SCLK active edge to $\overline{SYNC}$ rising edge hold time	t_{CST}		5			ns
Data setup time	t_{DS}		5			ns
Data hold time	t_{DH}		3			ns
$\overline{SYNC}$ high time	t_{SH}		30			ns
$\overline{SYNC}$ inactive edge to SDO valid	t_{DDS}	V_{DD} = +2.7V		25	35	ns
		V_{DD} = +5V		20	30	ns
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
I_{DD} (normal operation)		Logic inputs = 0V			5	µA
V_{DD} = +4.5 V to +5.5 V		V_{IH} = V_{DD} and V_{IL} = GND		0.8	5	µA
V_{DD} = +2.7 V to +3.6 V		V_{IH} = V_{DD} and V_{IL} = GND		0.4	2.5	µA
AC CHARACTERISTICS(2)						
Output voltage settling time					0.2	µs
Reference multiplying BW		V_{REF} = 7 V_{PP}, Data = FFFh		10		MHz
DAC glitch impulse		V_{REF} = 0 V to 10 V, Data = 7FFh to 800h to 7FFh		5		nV-s
Feedthrough error V_{OUT}/V_{REF}		Data = 000h, V_{REF} = 100kHz		–60		dB
Digital feedthrough				2		nV-s
Total harmonic distortion				–105		dB
Output spot noise voltage				18		nV/√Hz

(2) Specified by design and characterization; not production tested.

PIN DESCRIPTION



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1	$I_{OUT}1$	DAC Current Output
2	$I_{OUT}2$	DAC Analog Ground. This pin is normally tied to the analog ground of the system.
3	GND	Ground pin.
4	SCLK	Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device may be configured such that data is clocked into the shift register on the rising edge of SCLK.
5	SDIN	Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, on power-up, data is clocked into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to the rising edge.
6	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers, and the input shift register is enabled. Data is loaded to the shift register on the active edge of the following clocks (power-on default is falling clock edge). In stand-alone mode, the serial interface counts the clocks and data is latched to the shift register on the 16th active clock edge.
7	SDO	Serial Data Output. This allows a number of parts to be daisy-chained. By default, data is clocked into the shift register on the falling edge and out via SDO on the rising edge of SCLK. Data will always be clocked out on the alternate edge to loading data to the shift register. Writing the Readback control word to the shift register makes the DAC register contents available for readback on the SDO pin, clocked out on the opposite edges to the active clock edge.
8	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.7V to 5.5V.
9	V_{REF}	DAC Reference Voltage Input
10	R_{FB}	DAC Feedback Resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

TYPICAL CHARACTERISTICS: V_{DD} = +5V

At T_A = +25°C, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

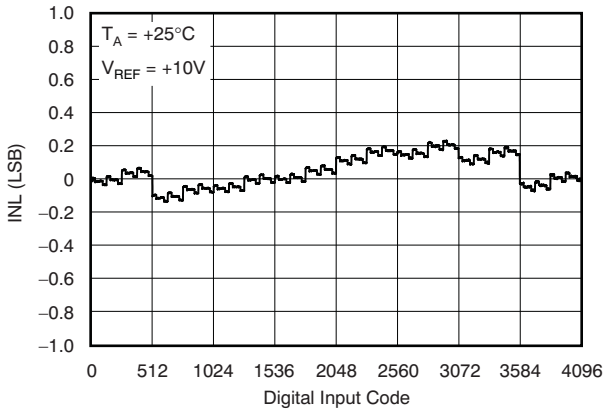


Figure 1.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

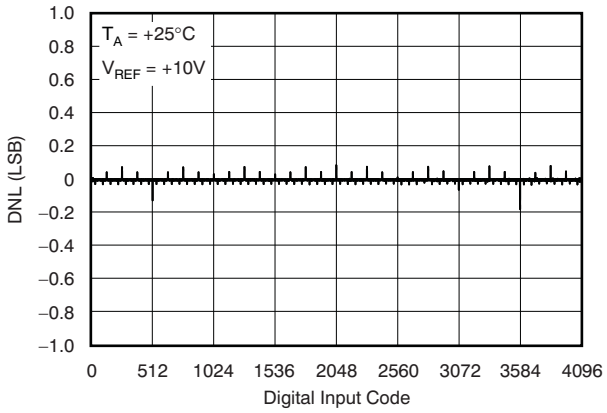


Figure 2.

LINEARITY ERROR vs DIGITAL INPUT CODE

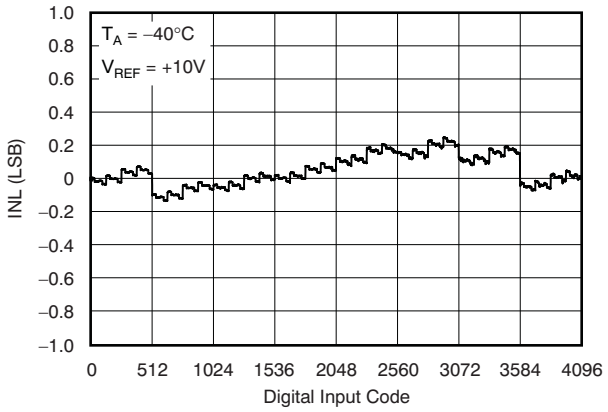


Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

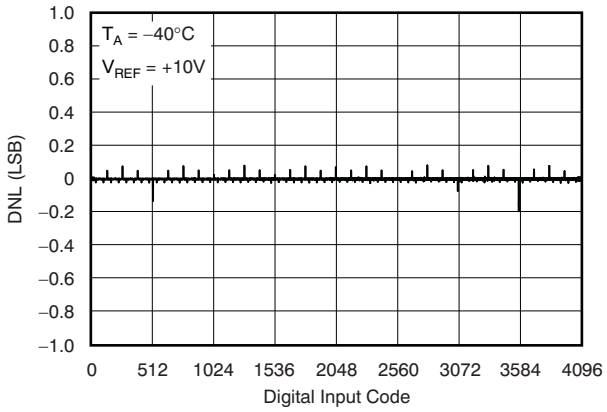


Figure 4.

LINEARITY ERROR vs DIGITAL INPUT CODE

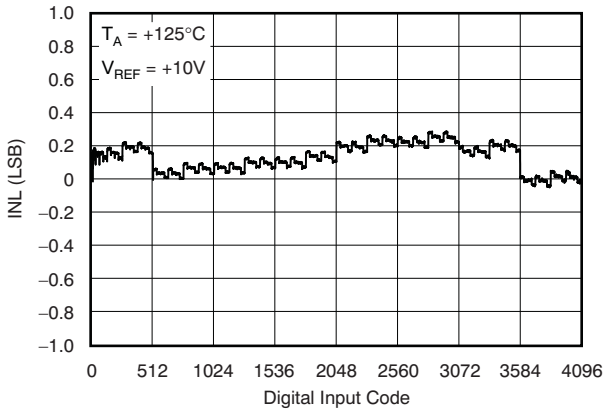


Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

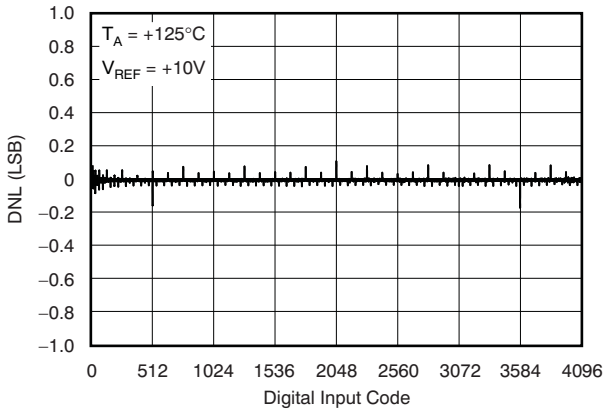


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

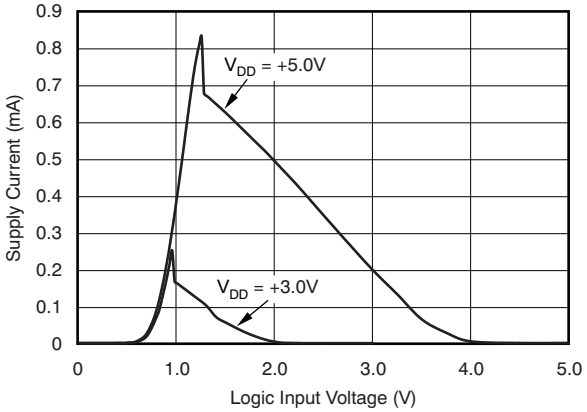


Figure 7.

REFERENCE MULTIPLYING BANDWIDTH

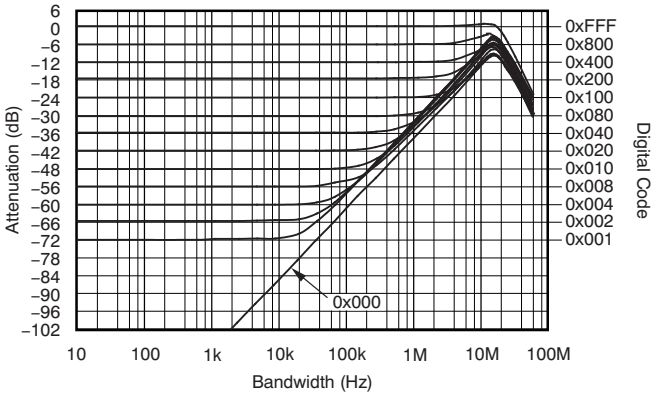


Figure 8.

MIDSCALE DAC GLITCH

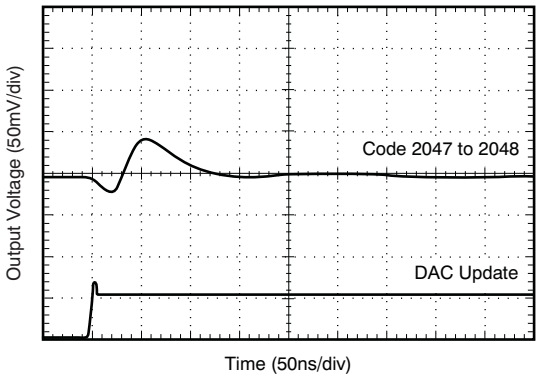


Figure 9.

MIDSCALE DAC GLITCH

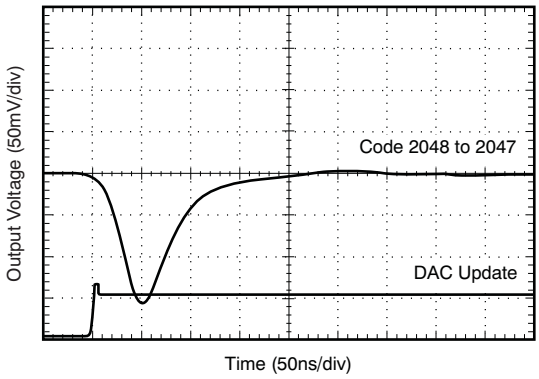


Figure 10.

DAC SETTLING TIME

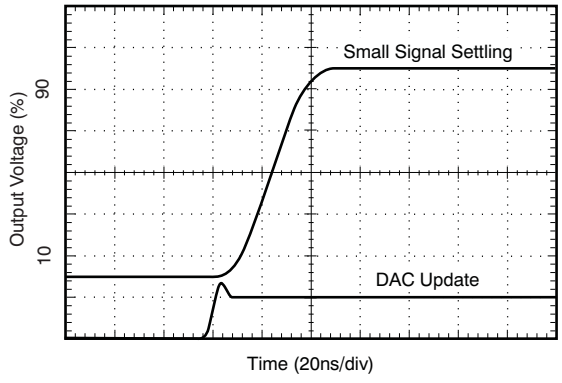


Figure 11.

GAIN ERROR vs TEMPERATURE

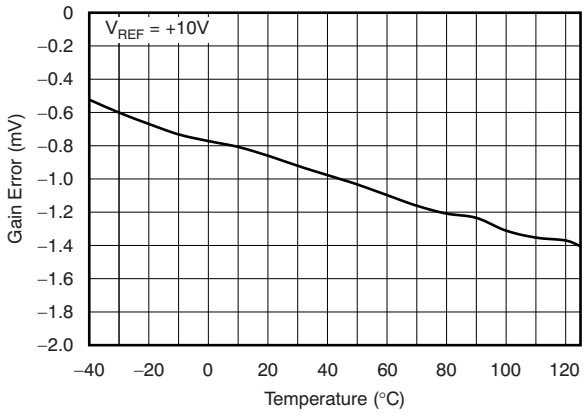


Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, unless otherwise noted.

SUPPLY CURRENT vs TEMPERATURE

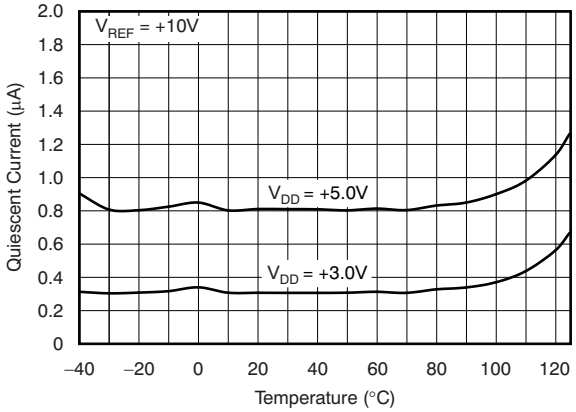


Figure 13.

OUTPUT LEAKAGE vs TEMPERATURE

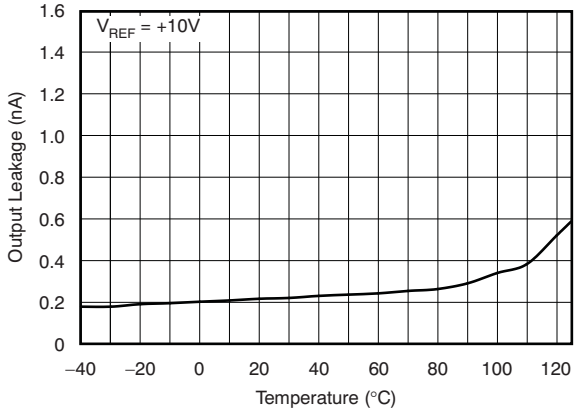


Figure 14.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

At T_A = +25°C, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

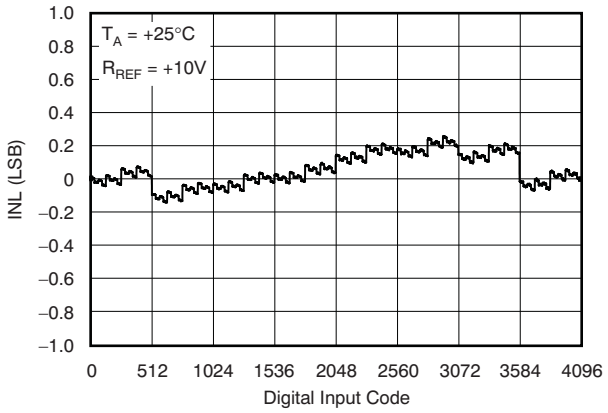


Figure 15.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

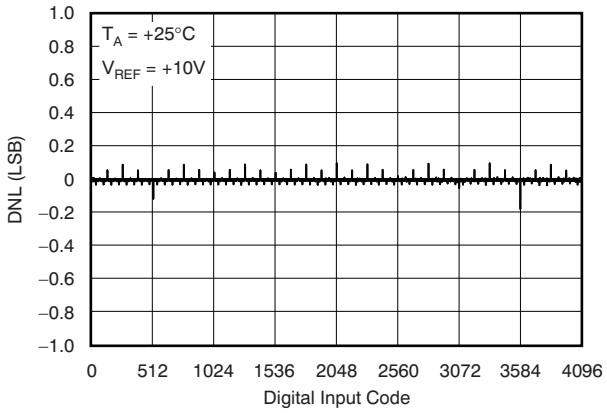


Figure 16.

LINEARITY ERROR vs DIGITAL INPUT CODE

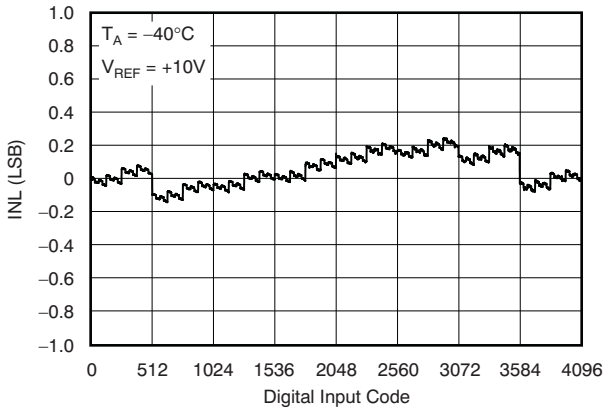


Figure 17.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

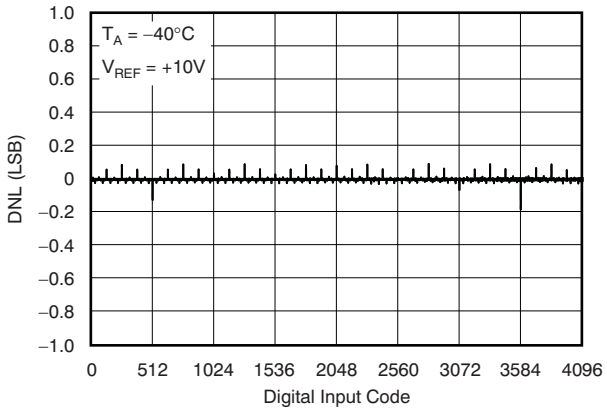


Figure 18.

LINEARITY ERROR vs DIGITAL INPUT CODE

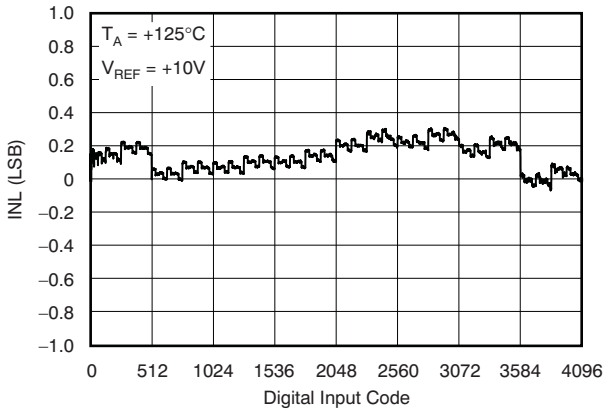


Figure 19.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

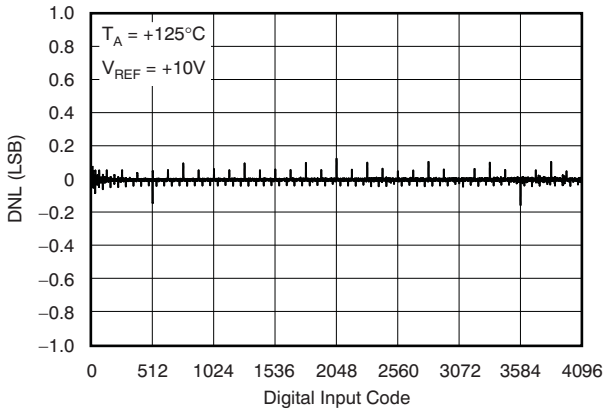


Figure 20.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, unless otherwise noted.

MIDSCALE DAC GLITCH

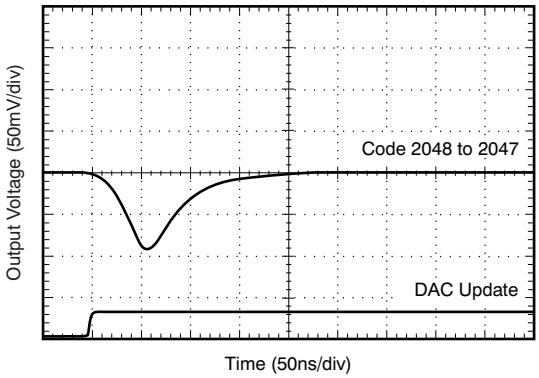


Figure 21.

MIDSCALE DAC GLITCH

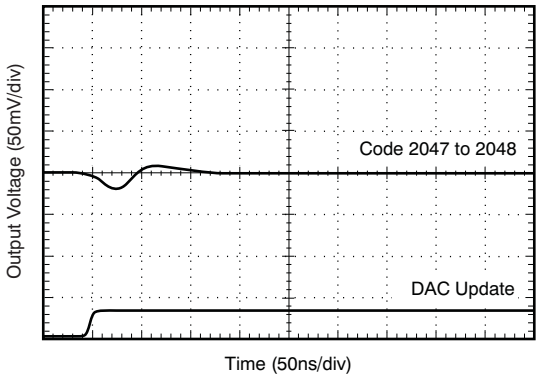


Figure 22.

GAIN ERROR vs TEMPERATURE

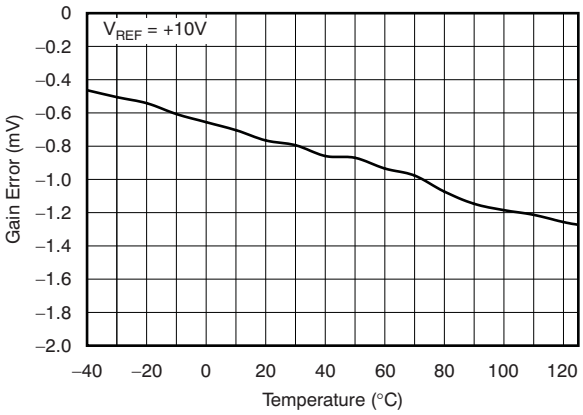


Figure 23.

OUTPUT LEAKAGE vs TEMPERATURE

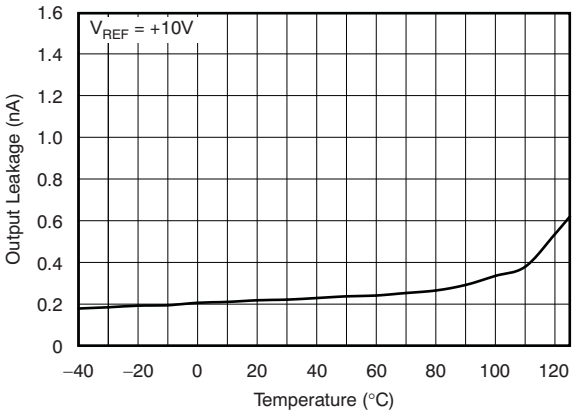


Figure 24.

Theory of Operation

The DAC7811 is a single channel, current output, 12-bit digital-to-analog converter (DAC). The architecture, illustrated in Figure 25, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to $I_{OUT}1$ or the $I_{OUT}2$ terminal. The $I_{OUT}1$ terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V_{REF} that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 10kΩ ±20%. The external reference voltage can vary over a range of –15V to +15V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter and the DAC7811 R_{FB} resistor, output voltage ranges of $–V_{REF}$ to V_{REF} can be generated.

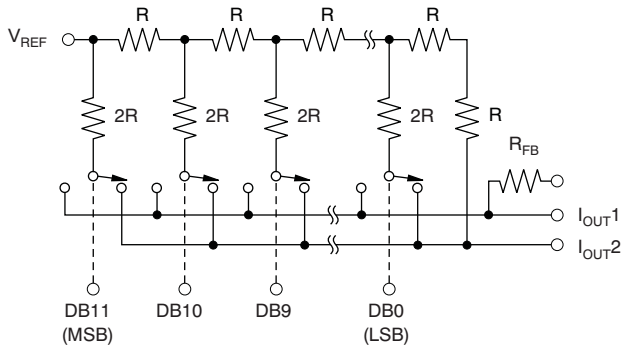


Figure 25. Equivalent R-2R DAC Circuit

When using an external I/V converter and the DAC7811 R_{FB} resistor, the DAC output voltage is given by Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{CODE}{4096} \quad (1)$$

Each DAC code determines the 2R leg switch position to either GND or I_{OUT}. Because the DAC output impedance as seen looking into the $I_{OUT}1$ terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC $I_{OUT}1$ terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC7811 due to offset modulation versus DAC code.

For best linearity performance of the DAC7811, a low offset voltage op amp (such as the OPA277) is recommended (see Figure 26). This circuit allows V_{REF} swinging from –10V to +10V.

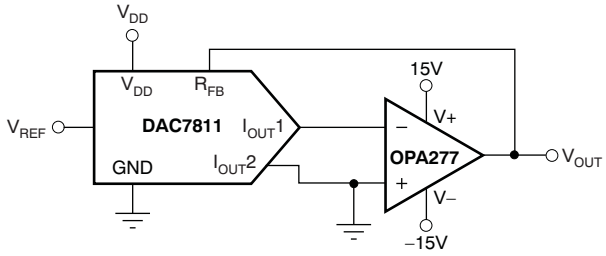


Figure 26. Voltage Output Configuration

Theory of Operation (continued)

Table 1. Control Logic Truth Table(1)

CLK	$\overline{\text{SYNC}}$	SERIAL SHIFT REGISTER	DAC REGISTER
X	H	No effect	Latched
↓–	L	Shift register data advanced one bit	Latched
X	↑+	In daisy-chain mode, the function as determined by C3-C0 is executed.	In daisy-chain mode, the contents may change as determined by C3-C0.

(1) ↓– Negative logic transition, default CLK mode;↑+ Positive logic transition; **X** = Do not care.

Serial Interface

The DAC7811 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and SDIN), which is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most Digital Signal Processor (DSP) devices. See the Serial Write Operation timing diagram (Figure 28) for an example of a typical write sequence. The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line are clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DAC7811 compatible with high-speed DSPs. The SDIN and SCLK input buffers are gated off while $\overline{\text{SYNC}}$ is high which minimizes the power dissipation of the digital interface. After $\overline{\text{SYNC}}$ goes low, the digital interface will respond to the SDIN and SCLK input signals and data can now be shifted into the device. If an inactive clock edge occurs after $\overline{\text{SYNC}}$ goes low, but before the first active clock edge, it will be ignored. If the SDO pin is being used then $\overline{\text{SYNC}}$ must remain low until after the inactive clock edge that follows the 16th active clock edge.

Input Shift Register

The input shift register is 16 bits wide, as shown in Figure 27. The four MSBs are the control bits C3–C0; these bits determine which function will be executed at the rising edge of $\overline{\text{SYNC}}$ in daisy-chain mode or the 16th active clock edge in stand-alone mode. The remaining 12 bits are the data bits. On a load and update command (C3–C0 = 0001) these 12 data bits will be transferred to the DAC register; otherwise, they have no effect.

4 CONTROL BITS				12 DATA BITS											
B15 (MSB)	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
C3	C2	C1	C0	DB11											DB0

Figure 27. Contents of the 16-Bit Input Shift Register

$\overline{\text{SYNC}}$ Interrupt (Stand-Alone Mode)

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs.

Daisy-Chain

The DAC7811 powers up in the daisy-chain mode which must be used when two or more devices are connected in tandem. The SCLK and $\overline{\text{SYNC}}$ signals are shared across all devices while the SDO output of the first device connects to the SDIN input of the following device, and so forth. In this configuration 16 SCLK cycles for each DAC7811 in the chain are required. Please refer to the timing diagram of Figure 28.

For *n* devices in a daisy-chain configuration, 16*n* SCLK cycles are required to shift in the entire input data stream. After 16*n* active SCLK edges are received following a falling $\overline{\text{SYNC}}$, the data stream becomes complete, and $\overline{\text{SYNC}}$ can brought high to update *n* devices simultaneously.

When $\overline{\text{SYNC}}$ is brought high, each device will execute the function defined by the four DAC control bits C3-C0 in its input shift register. For example, C3-C0 must be **0001** for each DAC in the chain that is to be updated with new data, and C3-C0 must be **0000** for each DAC in the chain whose contents are to remain unchanged.

A continuous stream containing the exact number of SCLK cycles may be sent first while the $\overline{\text{SYNC}}$ signal is held low, and then raise $\overline{\text{SYNC}}$ at a later time. Nothing happens until the rising edge of $\overline{\text{SYNC}}$, and then each DAC7811 in the chain will execute the function defined by the four DAC control bits C3-C0 in its input shift register.

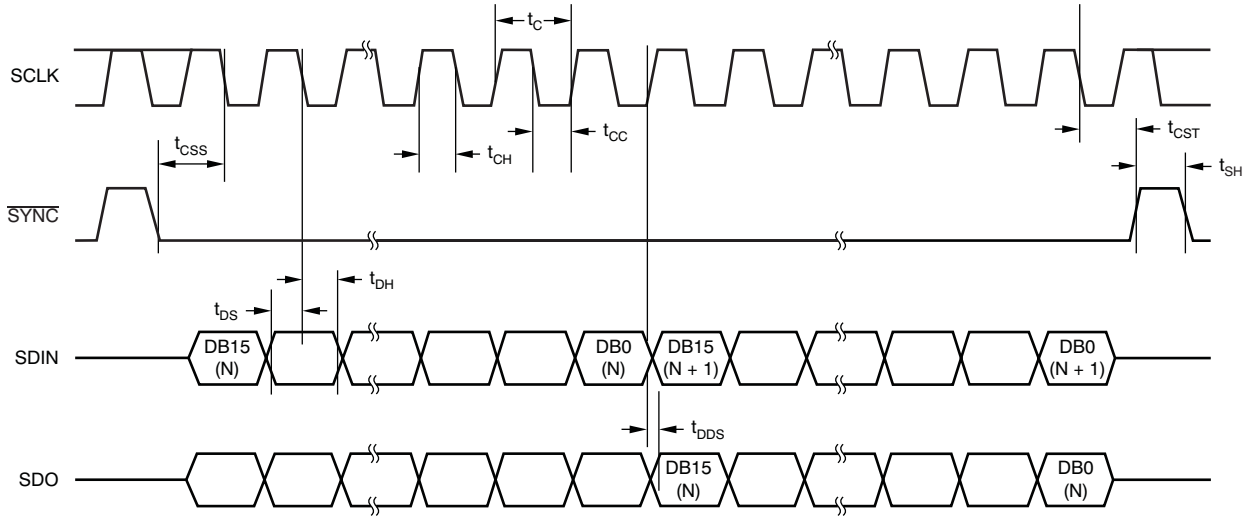


Figure 28. DAC7811 Timing Diagram

Control Bits C3 to C0

Control Bits C3 to C0 allow control of various functions of the DAC; see Table 2. Default settings of the DAC on powering up are as follows: Data clocked into shift register on falling clock edges; daisy-chain mode is enabled. The device powers on with zero-scale loaded into the DAC register and I_{OUT} lines. The DAC control bits allow the user to adjust certain features as part of an initialization sequence; for example, daisy-chaining may be disabled if not in use, active clock edge may be changed to rising edge, and DAC output may be cleared to either zero or midscale. The user may also initiate a readback of the DAC register contents for verification purposes.

Table 2. Serial Input Register Data Format, Data Loaded MSB First

C3	C2	C1	C0	FUNCTION IMPLEMENTED
0	0	0	0	No operation (power-on default)
0	0	0	1	Load and update
0	0	1	0	Initiate readback
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Daisy-chain disable
1	0	1	0	Clock data to shift register on rising edge
1	0	1	1	Clear DAC output to zero
1	1	0	0	Clear DAC output to midscale
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

APPLICATION INFORMATION

Stability Circuit

For a current-to-voltage design (see Figure 29), the DAC7811 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct printed circuit board (PCB) layout design practices. For each code change, there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C_1 (1pF to 5pF typ) can be added to the design, as shown in Figure 29.

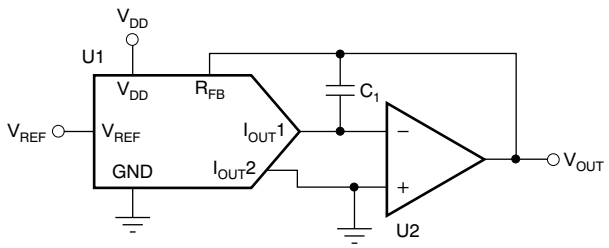


Figure 29. Gain Peaking Prevention Circuit with Compensation Capacitor

Amplifier Selection

There are many choices and many differences in selecting the proper operational amplifier for a multiplying DAC (MDAC). Making the analog signal out of the MDAC is one critical aspect. However, there are also other issues to take into account such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy. Table 3 and Table 4 suggest some suitable operational amplifiers for low power, fast settling, and high-speed applications. A greater selection of operational amplifiers can be found at www.ti.com/amplifer.

Table 3. Suitable Precision Operational Amplifiers from Texas Instruments

PRODUCT	TOTAL SUPPLY VOLTAGE (V) (min)	TOTAL SUPPLY VOLTAGE (V) (max)	I_Q PER CHANNEL (max) (mA)	GBW (typ) (MHz)	SLEW RATE (typ) (V/µs)	OFFSET DRIFT (typ) (µV/°C)	I_{IB} (max) (pA)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
Low Power										
OPA703	4	12	0.2	1	0.6	4	10	70	SOT5-23, PDIP-8, SOIC-8	12V, CMOS, Rail-to-Rail I/O, Operational Amplifier
OPA735	2.7	12	0.75	1.6	1.5	0.01	200	115	SOT5-23, SOIC-8	0.05µV/°C (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier
OPA344	2.7	5.5	0.25	1	1	2.5	10	80	SOT5-23, PDIP-8, SOIC-8	Low Power, Single-Supply, Rail-To-Rail Operational Amplifiers MicroAmplifier Series
OPA348	2.1	5.5	0.065	1	0.5	2	10	70	SC5-70, SOT5-23, SOIC-8	1MHz, 45µA, Rail-to-Rail I/O, Single Op Amp
OPA277	4	36	0.825	1	0.8	0.1	1000	130	PDIP-8, SOIC-8, SON-8	High Precision Operational Amplifiers
Fast Settling										
OPA350	2.7	5.5	7.5	38	22	4	10	76	MSOP-8, PDIP-8, SOIC-8	High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series
OPA727	4	12	6.5	20	30	0.6	500	86	MSOP-8, SON-8	e-trim 20MHz, High Precision CMOS Operational Amplifier
OPA227	5	36	3.8	8	2.3	0.1	10000	120	PDIP-8, SOIC-8	High Precision, Low Noise Operational Amplifiers

Table 4. Suitable High Speed Operational Amplifiers from Texas Instruments (Multiple Channel Options)

PRODUCT	SUPPLY VOLTAGE (V)	GBW PRODUCT (MHz)	VOLTAGE NOISE nV/√Hz	GBW (typ) (MHz)	SLEW RATE (V/µs)	V_{OS} (typ) (µV)	V_{OS} (max) (µV)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
Single Channel										
THS4281	±2.7 to ±15	38	12.5	35	500	3500	500	1000	SOT5-23, MSOP-8, SOIC-8	Very Low-Power High Speed Rail-To-Rail Input/Output Voltage Feedback Operational Amplifier
THS4031	±4.5 to ±16.5	200	1.6	100	500	3000	3000	8000	CDIP-8, MSOP-8, SOIC-8	100-MHz Low Noise Voltage-Feedback Amplifier
THS4631	±4.5 to ±16.5	210	7	900	260	2000	50pA	2	SOIC-8, MSOP-8	High Speed FET-Input Operational Amplifier
OPA656	±4 to ±6	230	7	290	250	2600	2pA	5pA	SOIC-8, SOT5-23	Wideband, Unity Gain Stable FET-Input Operational Amplifier
OPA820	±2.5 to ±6	280	2.5	240	200	1200	900	23,000	SOIC-8, SOT5-23	Unity Gain Stable, Low Noise, Voltage Feedback Operational Amplifier
Dual Channel										
THS4032	±4.5 to ±16.5	200	1.6	100	500	3000	3000	8000	SOIC-8, MSOP-8	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
OPA2822	±2 to ±6.3	220	2	170	200	1200	9600	12000	SOIC-8, MSOP-8	SpeedPlus Dual Wideband, Low-Noise Operational Amplifier

Positive Voltage Output Circuit

As Figure 30 illustrates, in order to generate a positive voltage output, a negative reference is input to the DAC7811. This design is suggested instead of using an inverting amp to invert the output as a result of resistor tolerance errors. For a negative reference, V_{OUT} and GND of the reference are level-shifted to a virtual ground and a –2.5V input to the DAC7811 with an op amp.

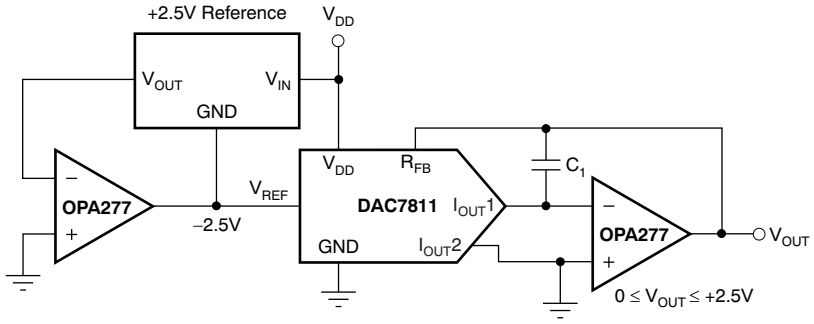


Figure 30. Positive Voltage Output Circuit

Bipolar Output Section

The DAC7811, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 31, external op amp U3 is added as a summing amp and has a gain of 2X that widens the output span to 5V. A 4-quadrant multiplying circuit is implemented by using a 2.5V offset of the reference voltage to bias U3. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full-scale produces output voltages of V_{OUT} = –2.5V to V_{OUT} = +2.5V.

$$V_{OUT} = \left(\frac{D}{0.5 \times 2^{N}} - 1\right) \times V_{REF} \quad (2)$$

External resistance mismatching is the significant error in Figure 31.

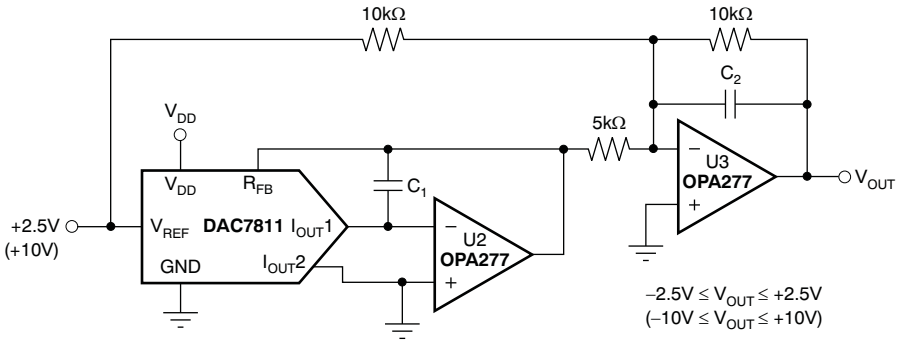


Figure 31. Bipolar Output Circuit

Programmable Current Source Circuit

A DAC7811 can be integrated into the circuit in Figure 32 to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 3:

$$I_L = \frac{(R2 + R3) \,/\, R1}{R3} \times V_{REF} \times \frac{D}{4096} \tag{3}$$

The value of R3 in Equation 3 can be reduced to increase the output current drive of U3. U3 can drive ±20mA in both directions with voltage compliance limited up to 15V by the U3 voltage supply. Elimination of the circuit compensation capacitor C_1 in the circuit is not suggested as a result of the change in the output impedance Z_O, according to Equation 4:

$$Z_O = \frac{R1'R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \tag{4}$$

As shown in Equation 4, with matched resistors, Z_O is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C_1 into the circuit, possible oscillation problems are eliminated. The value of C_1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

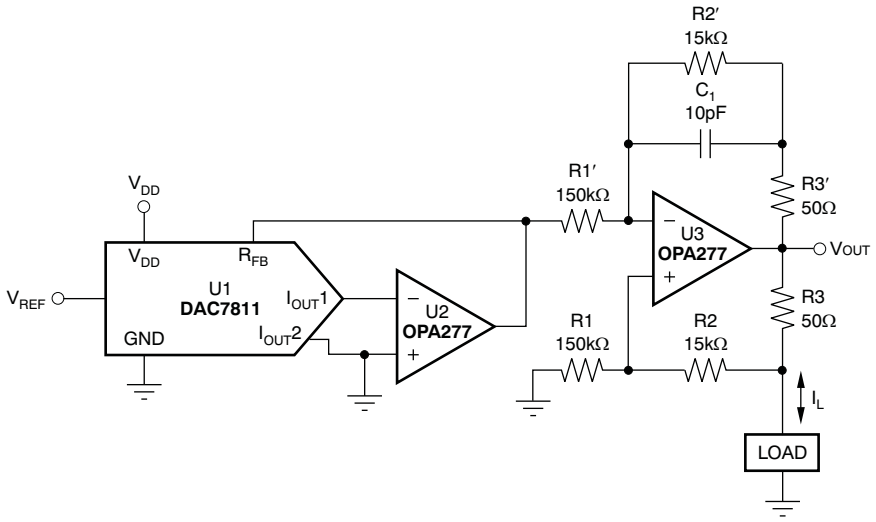


Figure 32. Programmable Bidirectional Current Source Circuit

Cross-Reference

The DAC7811 has an industry-standard pinout. Table 5 provides the cross-reference information.

Table 5. Cross-Reference

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC7811	±1	±1	–40°C to +125°C	10-Lead MicroSOIC	MSOP-10	AD5443YRM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC7811IDGS	ACTIVE	MSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7811IDGSG4	ACTIVE	MSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7811IDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7811IDGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7811IDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7811IDGSTG4	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

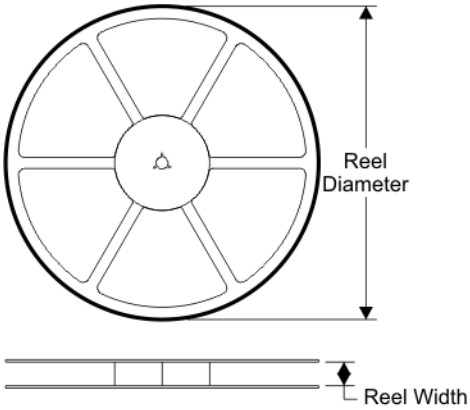
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

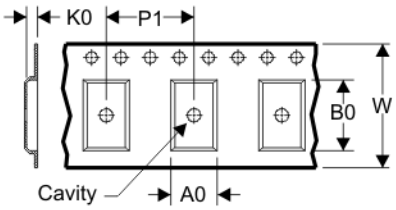
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

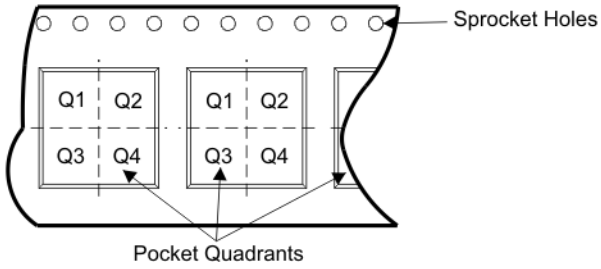


TAPE DIMENSIONS



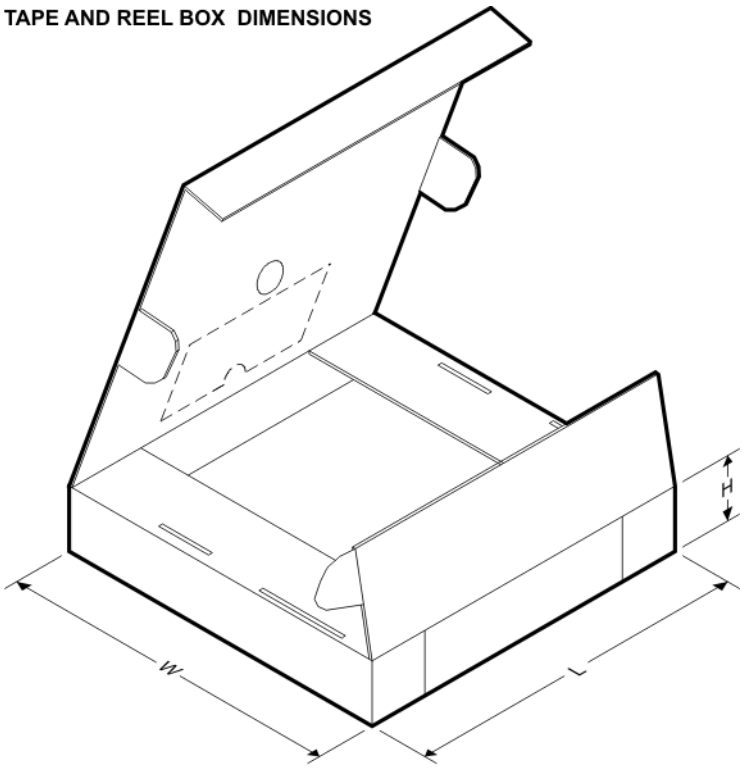
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



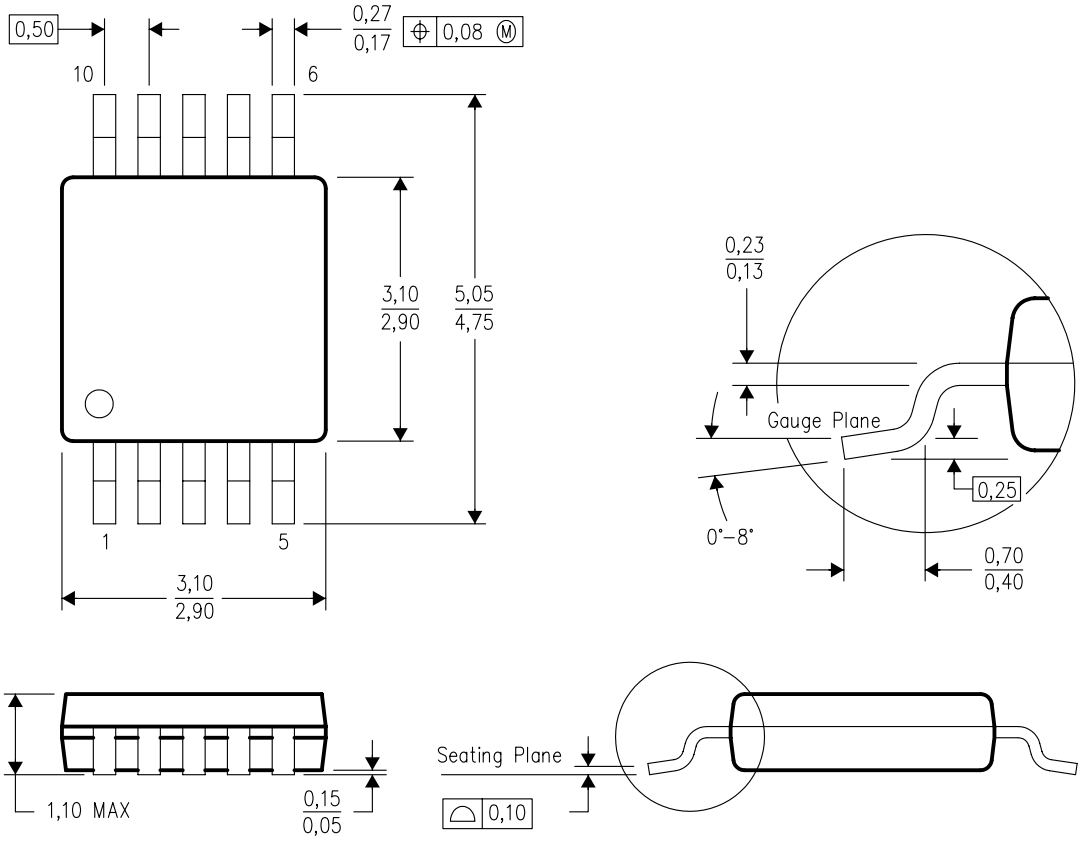
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7811IDGSR	DGS	10	SITE 60	330	12	5.3	3.4	1.4	8	12	Q1
DAC7811IDGST	DGS	10	SITE 60	330	12	5.3	3.4	1.4	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
DAC7811IDGSR	DGS	10	SITE 60	346.0	346.0	29.0
DAC7811IDGST	DGS	10	SITE 60	346.0	346.0	29.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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