DACx750 Single-Channel, 12- and 16-Bit Programmable Current Output Digital-to-Analog Converters for 4-mA to 20-mA Current Loop Applications

1 Features

- Current Output Options:
  - 0 mA to 24 mA
  - 4 mA to 20 mA
  - 0 mA to 20 mA
- ±0.1% FSR Typical Total Unadjusted Error (TUE)
- DNL: ±1 LSB Max
- Max Loop Compliance Voltage: AVDD – 2 V
- Internal 5-V Reference (10 ppm/°C, max)
- Internal 4.6-V Power-Supply Output
- CRC Frame Error Check
- Watchdog Timer
- Thermal Alarm
- Open Circuit Alarm
- Terminals to Monitor Output Current
- On-Chip Fault Alarm
- User-Calibration for Offset and Gain
- Wide Temperature Range: –40°C to +125°C
- 6-mm × 6-mm QFN-40 and TSSOP-24 Packages

2 Applications

- 4-mA to 20-mA Current Loops
- Analog Output Modules
- Building Automation
- Environment Monitoring
- Programmable Logic Controllers (PLCs)
- Field Sensors and Process Transmitters

3 Description

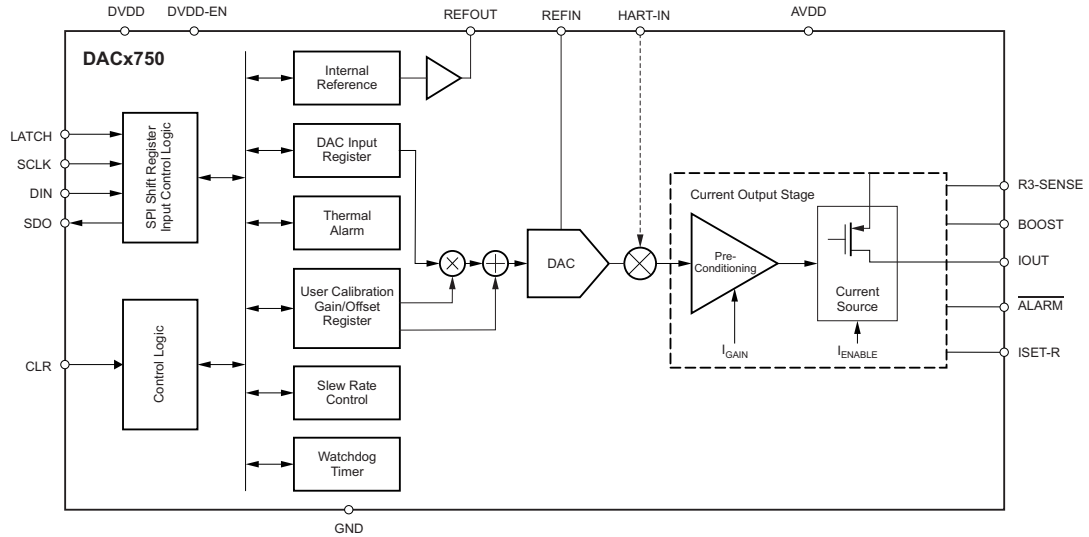
The DAC7750 and DAC8750 are low-cost, precision, fully-integrated 12-bit and 16-bit digital-to-analog converters (DACs) designed to meet the requirements of industrial process-control applications. These devices can be programmed as a current output with a range of 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA. The DAC7750 and DAC8750 include reliability features such as CRC error checking on the serial peripheral interface (SPI™) frame, a watchdog timer, an open circuit, compliance voltage, and thermal alarm. In addition, the output current can be monitored by accessing an internal precision resistor.

These devices include a power-on-reset function to ensure that the device powers up in a known state (IOUT is disabled and in a Hi-Z state). The CLR terminal sets the current output to the low end of the range if the output is enabled. Program the zero and gain registers to digitally calibrate the device in the end system. The output slew rate is also programmable by register. These devices can superimpose an external HART® signal on the current output, and can operate with a +10-V to +36-V supply.

All versions are available in both 6-mm × 6-mm QFN-40 and TSSOP-24 packages.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
DACx750IPWP	HTSSOP (24)	7,8 mm × 4,4 mm
DACx750IRHA	VQFN (40)	6 mm × 6 mm



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (December 2013) to Revision A **Page**

- Changed format to meet latest data sheet standards; added new sections and moved existing sections ... 1
- Changed data sheet from 1-page product preview to full production data ... 1

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Device Comparison(1)

PRODUCT	RESOLUTION	TUE (%FSR)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE
DAC8750	16	0.2%	±1	–40°C to +125°C
DAC7750	12	0.2%	±1	–40°C to +125°C

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

Device Family Comparison

RESOLUTION (BITS)	CURRENT OUTPUT	CURRENT AND VOLTAGE OUTPUT
12	DAC7750	DAC7760
16	DAC8750	DAC8760

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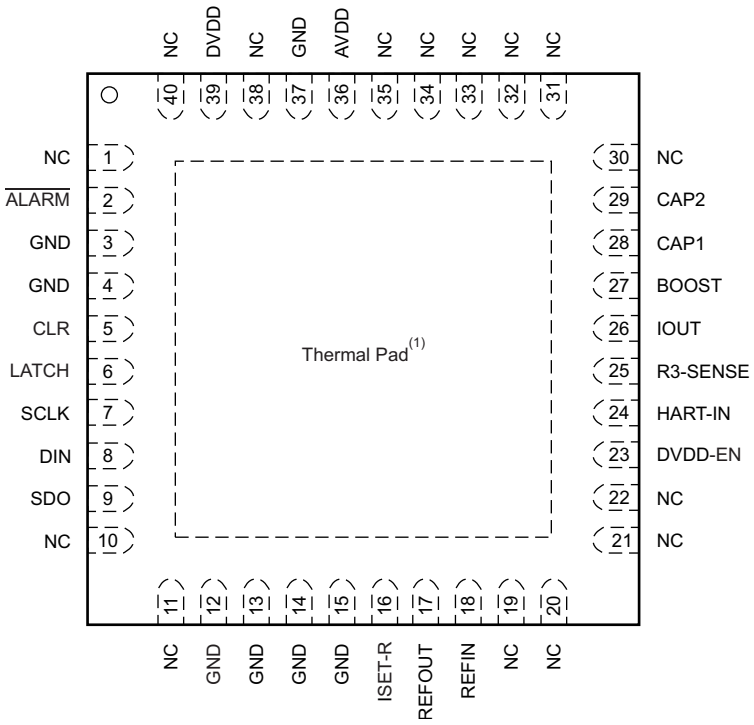
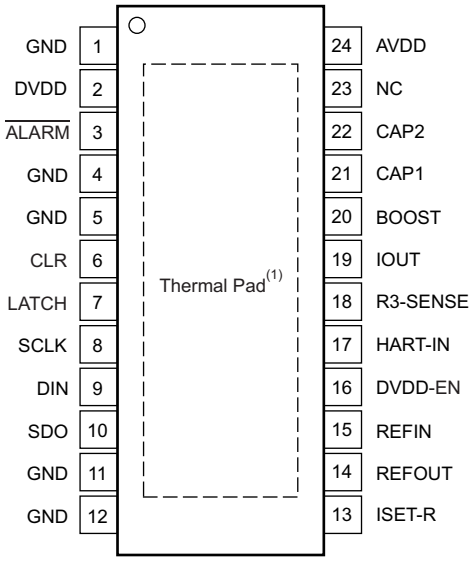
5 Terminal Configuration and Functions

RHA Package
40-Terminal VQFN
(Top View)



PWP Package
24-Terminal HTSSOP
(Top View)



(1) Thermal pad connected to ground.

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Terminal Functions

TERMINAL			DESCRIPTION
NAME	RHA (VQFN)	PWP (HTSSOP)	
$\overline{\text{ALARM}}$	2	3	Alarm terminal. Open drain output. External pull-up resistor required (10 kΩ). The terminal goes low (active) when the $\overline{\text{ALARM}}$ condition is detected (open circuit/over temperature/timeout, etc.).
AVDD	36	24	Positive analog power supply.
BOOST	27	20	Boost terminal. External transistor connection (optional).
CAP1	28	21	Connection for output filtering capacitor (optional).
CAP2	29	22	Connection for output filtering capacitor (optional).
CLR	5	6	Clear input. Logic high on this terminal causes the part to enter CLEAR state. Active high.
DIN	8	9	Serial data input. Data are clocked into the 24-bit input shift register on the rising edge of the serial clock input. Schmitt-Trigger logic input.
DVDD	39	2	Digital power supply. Can be input or output, depending on DVDD-EN terminal.
DVDD-EN	23	16	Internal power-supply enable terminal. Connect this terminal to GND to disable the internal supply, or leave this terminal unconnected to enable the internal supply. When this terminal is connected to GND, an external supply must be connected to the DVDD terminal.
GND	12, 13, 14, 15, 37	1, 11, 12	Ground reference point for all analog circuitry of the device.
GND	3, 4	4, 5	Ground reference point for all digital circuitry of the device.
HART-IN	24	17	Input terminal for HART modulation.
IOUT	26	19	Current output terminal
ISET-R	16	13	Connection terminal for external precision resistor (15 kΩ). See the Detailed Description section of this datasheet.
LATCH	6	7	Load DAC registers input. A rising edge on this terminal loads the input shift register data into the DAC data and control registers and updates the DAC output.
NC	1, 10, 11, 19, 20, 21, 22, 30, 31, 32, 33, 34, 35, 38, 40	23	No connection.
R3-SENSE	25	18	This terminal is used as a monitoring feature for the output current. The voltage measured between the R3-SENSE terminal and the BOOST terminal is directly proportional to the output current.
REFOUT	17	14	Internal reference output. Connects to REFIN when using internal reference.
REFIN	18	15	Reference input
SCLK	7	8	Serial clock input of the SPI. Data can be transferred at rates up to 30 MHz. Schmitt-Trigger logic input.
SDO	9	10	Serial data output. Data are valid on the rising edge of SCLK.
Thermal Pad	—	—	The thermal pad is internally connected to GND. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance. The pad can be electrically connected to the same potential as the GND terminal or left electrically unconnected provided a supply connection is made at the GND terminal.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	40	V
DVDD to GND	–0.3	6	V
IOUT to GND	-0.3	AVDD	V
REFIN to GND	–0.3	6	V
REFOUT to GND	–0.3	6	V
Current into REFOUT		10	mA
Digital input voltage to GND	–0.3	DVDD + 0.3	V
SDO to GND	–0.3	DVDD + 0.3	V
$\overline{\text{ALARM}}$ to GND	–0.3	6	V
Operating temperature range	–40	+125	°C
Junction temperature range (T_J max)		+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

		MIN	MAX	UNIT
t_{stg}	Storage temperature range	–65	+150	°C
V_{ESD}(1)	Human body model (HBM) ESD stress voltage(2)		3000	V
	Charged device model (CDM) ESD stress voltage(3)		1000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
AVDD	10	24	36	V
Operating temperature range	-40	25	125	°C
Loop compliance voltage	0		AVDD – 2	V

6.4 Thermal Information

THERMAL METRIC		DAC7750, DAC8750		UNIT
		RHA (VQFN)	PWP (HTSSOP)	
		40 TERMINALS	24 TERMINALS	
θ_{JA}	Junction-to-ambient thermal resistance	32.9	32.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	17.2	14.1	
θ_{JB}	Junction-to-board thermal resistance	7.5	12.2	
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.3	
ψ_{JB}	Junction-to-board characterization parameter	7.5	12.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.4	0.63	

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6.5 Electrical Characteristics

At AVDD = +10 V to +36 V, GND = 0 V, REFIN = +5 V external, DVDD = +2.7 V to +5.5 V, and all specifications are from –40°C to +125°C (unless otherwise noted). For IOUT: R_L = 300 Ω. Typical specifications are at +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT OUTPUT						
Current output ranges			0		24	mA
			0		20	mA
			4		20	mA
Resolution		DAC8750	16			Bits
		DAC7750	12			Bits
CURRENT OUTPUT ACCURACY (For 0-mA to 20-mA and 0-mA to 24-mA Range Settings)(1)						
Total unadjusted error, TUE		T_A = –40°C to +125°C	–0.2		+0.2	%FSR
		T_A = –40°C to +85°C	–0.16		+0.16	%FSR
		T_A = +25°C	–0.08	±0.02	+0.08	%FSR
Differential nonlinearity, DNL		Monotonic			±1	LSB
Relative accuracy, INL(2)		T_A = –40°C to +125°C			±0.080	%FSR
		T_A = –40°C to +85°C			±0.024	%FSR
Offset error		T_A = –40°C to +125°C	–0.17		+0.17	%FSR
		T_A = –40°C to +85°C	–0.1		+0.1	%FSR
		T_A = +25°C	–0.07	±0.01	+0.07	%FSR
Offset error temperature coefficient				±5		ppm FSR/°C
Full-scale error		T_A = –40°C to +125°C	–0.2		+0.2	%FSR
		T_A = –40°C to +85°C	–0.16		+0.16	%FSR
		T_A = +25°C	–0.08	±0.015	+0.08	%FSR
Full-scale error temperature coefficient	Internal R_{SET}			±5		ppm FSR/°C
	External R_{SET}			±10		ppm FSR/°C
Gain error	Internal R_{SET}	–40°C to +125°C	–0.2		+0.2	%FSR
		–40°C to +85°C	–0.15		+0.15	%FSR
		T_A = +25°C	–0.08	±0.01	+0.08	%FSR
	External R_{SET}	–40°C to +125°C	–0.17		+0.17	%FSR
		–40°C to +85°C	–0.12		+0.12	%FSR
		T_A = +25°C	–0.05	±0.01	+0.05	%FSR
Gain error temperature coefficient	Internal R_{SET}			±3		ppm FSR/°C
	External R_{SET}			±8		ppm FSR/°C
Output current drift vs time	Internal R_{SET}	T_A = +125°C, 1000 hrs		±50		ppm FSR
	External R_{SET}			±25		ppm FSR
CURRENT OUTPUT ACCURACY (for 4-mA to 20-mA Range Setting)(1)						
Total unadjusted error, TUE	Internal R_{SET}	T_A = –40°C to +125°C	–0.25		+0.25	%FSR
		T_A = +25°C	–0.08	±0.02	+0.08	%FSR
	External R_{SET}	T_A = –40°C to +125°C	–0.29		+0.29	%FSR
		T_A = –40°C to +85°C	–0.25		+0.25	%FSR
		T_A = +25°C	–0.1	±0.02	+0.1	%FSR
Differential nonlinearity, DNL		Monotonic			±1	LSB
Relative accuracy, INL(2)		T_A = –40°C to +125°C			±0.080	%FSR
		T_A = –40°C to +85°C			±0.024	%FSR
Offset error	Internal R_{SET}	T_A = –40°C to +125°C	–0.22		+0.22	%FSR
		T_A = –40°C to +85°C	–0.2		+0.2	%FSR
	External R_{SET}	T_A = –40°C to +125°C	–0.2		+0.2	%FSR
		T_A = –40°C to +85°C	–0.18		+0.18	%FSR
	Internal and External R_{SET}	T_A = +25°C	–0.07	±0.01	+0.07	%FSR

(1) DAC8750 and DAC7750 current output range is set by writing to RANGE bits in control register at address 0x55.
(2) For 0-mA to 20-mA and 0-mA to 24-mA ranges, INL is calculated beginning from code 0x0100 for DAC8750 and from code 0x0010 for DAC7750.

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Electrical Characteristics (continued)

At AVDD = +10 V to +36 V, GND = 0 V, REFIN = +5 V external, DVDD = +2.7 V to +5.5 V, and all specifications are from –40°C to +125°C (unless otherwise noted). For IOUT: R_L = 300 Ω. Typical specifications are at +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset error temperature coefficient				±3		ppm FSR/°C
Full-scale error	Internal R_{SET}	T_A = –40°C to +125°C	–0.25		+0.25	%FSR
		T_A = +25°C	–0 .08	±0.015	+0.08	%FSR
	External R_{SET}	T_A = –40°C to +125°C	–0.29		+0.29	%FSR
		T_A = –40°C to +85°C	–0.25		+0.25	%FSR
		T_A = +25°C	–0 .1	±0.015	+0.1	%FSR
Full-scale error temperature coefficient	Internal R_{SET}			±5		ppm FSR/°C
	External R_{SET}			±10		ppm FSR/°C
Gain error	Internal R_{SET}	T_A = –40°C to +125°C	–0.2		+0.2	%FSR
		T_A = –40°C to +85°C	–0.15		+0.15	%FSR
		T_A = +25°C	–0.08	±0.01	+0.08	%FSR
	External R_{SET}	T_A = –40°C to +125°C	–0.16		+0.16	%FSR
		T_A = –40°C to +85°C	–0.12		+0.12	%FSR
		T_A = +25°C	–0.05	±0.01	+0.05	%FSR
Gain error temperature coefficient	Internal R_{SET}			±3		ppm FSR/°C
	External R_{SET}			±8		ppm FSR/°C
Output current drift vs time	Internal R_{SET}	T_A = +125°C, 1000 hrs		±50		ppm FSR
	External R_{SET}	T_A = +125°C, 1000 hrs		±75		ppm FSR
CURRENT OUTPUT STAGE(3)						
Loop compliance voltage(4)		Output = 24 mA			AVDD – 2	V
Inductive load(5)				50		mH
DC PSRR					1	µA/V
Output impedance		Code = 0x8000		50		MΩ
R3 RESISTOR						
R3 resistor value			36	40	44	Ω
R3 resistor temperature coefficient				40		ppm/°C
EXTERNAL REFERENCE INPUT						
Reference input voltage			4.95	5	5.05	V
External reference current		REFIN = 5.0 V		30		µA
Reference input capacitance				10		pF
INTERNAL REFERENCE OUTPUT						
Reference output		T_A = +25°C	4.995		5.005	V
Reference temperature coefficient(3)		T_A = –40°C to +85°C			±10	ppm/°C
Output noise (0.1 Hz to 10 Hz)		T_A = +25°C		14		μV_{PP}
Noise spectral density		T_A = +25°C, 10 kHz		185		nV/√Hz
Capacitive load				600		nF
Load current				±5		mA
Short-circuit current (REFOUT shorted to GND)				25		mA
Load regulation		AVDD = 24 V, T_A = +25°C, sourcing		55		µV/mA
		AVDD = 24 V, T_A = +25°C, sinking		120		µV/mA
Line regulation				±1.2		µV/V
DVDD INTERNAL REGULATOR						
Output voltage		AVDD = 24 V		4.6		V
Output load current(3)					10	mA
Load regulation				3.5		mV/mA
Line regulation				1		mV/V
Short-circuit current		AVDD = 24 V, to GND		35		mA

(3) Specified by design and characterization; not production tested.
(4) Loop compliance voltage is defined as the voltage at the IOUT terminal.
(5) For stability, use slew rate limit feature or add a capacitor between IOUT and GND

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Electrical Characteristics (continued)

At AVDD = +10 V to +36 V, GND = 0 V, REFIN = +5 V external, DVDD = +2.7 V to +5.5 V, and all specifications are from –40°C to +125°C (unless otherwise noted). For IOUT: R_L = 300 Ω. Typical specifications are at +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitive load stability[3]					2.5	µF
DIGITAL INPUTS						
High-level input voltage, V_{IH}			2			V
Low-level input voltage, V_{IL}		3.6 V < AVDD < 5.5 V			0.8	V
		2.7 V < AVDD < 3.6 V			0.6	V
Hysteresis voltage				0.4		V
Input current		DVDD-EN, V_{IN} ≤ 5 V	–2.7			µA
		All terminals other than DVDD-EN			±1	µA
Terminal capacitance		Per terminal		10		pF
DIGITAL OUTPUTS						
SDO	Low-level output voltage, V_{OL}	Sinking 200 µA			0.4	V
	HIgh-level output voltage, V_{OH}	Sourcing 200 µA	DVDD – 0.5			V
	High-impedance leakage				±1	µA
$\overline{\text{ALARM}}$	Low-level output voltage, V_{OL}	10-kΩ pull-up resistor to DVDD			0.4	V
		2.5 mA			0.6	V
	High-impedance leakage				±1	µA
High-impedance output capacitance				10		pF
POWER-SUPPLY						
AVDD			10		36	V
DVDD		Internal regulator disabled	2.7		5.5	V
AIDD		Outputs disabled, external DVDD			3	mA
		Outputs disabled, internal DVDD			4	
		Code = 0x0000, IOUT enabled			3	
DIDD		V_{IH} = DVDD, V_{IL} = GND, interface idle			1	mA
Power dissipation		AVDD = 36 V, IOUT = 0 mA, DVDD = 5 V		95	115	mW
TEMPERATURE						
Specified performance range			–40		+125	°C
Thermal alarm				142		°C
Thermal alarm hysteresis				18		°C

6.6 Electrical Characteristics: AC

At AVDD = +10 V to +36 V, GND = 0 V, REFIN= +5 V external; and DVDD = +2.7 V to +5.5 V. For IOUT: R_L = 300 Ω. All specifications –40°C to +125°C, unless otherwise noted. Typical specifications are at +25°C.

PARAMETER[1]	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE					
Output current settling time	16-mA step, to 0.1% FSR, no L (inductance)		10		µs
	16-mA step, to 0.1% FSR, L < 1 mH		25		µs
AC PSRR	200-mV, 50-Hz or 60-Hz sine wave superimposed on power-supply voltage		–75		dB

(1) Specified by characterization, not production tested.

6.7 Timing Requirements: Write Mode(1)

At T_A = –40°C to +125°C and DVDD = +2.7 V to +5.5 V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_1	SCLK cycle time	33		ns
t_2	SCLK low time	13		ns
t_3	SCLK high time	13		ns
t_4	LATCH delay time	13		ns
t_5	LATCH high time(2)	40		ns
t_6	Data setup time	5		ns
t_7	Data hold time	7		ns
t_8	LATCH low time	40		ns
t_9	CLR pulse duration	20		ns
t_{10}	CLR activation time		5	µs

(1) Specified by design, not production tested.
(2) Based on digital interface circuitry only. When writing to DAC control and configuration registers, consider the analog output specifications in Electrical Characteristics: AC.

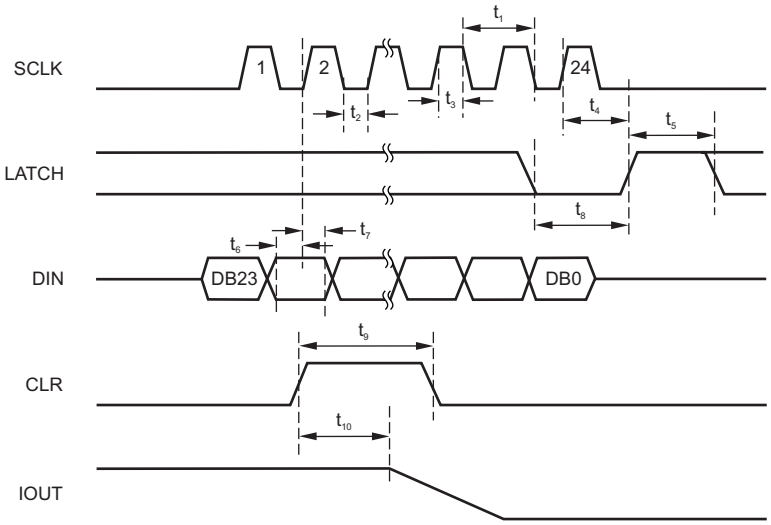

Figure 1. Write Mode Timing

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6.8 Timing Requirements: Readback Mode(1)

At T_A = –40°C to +125°C and DVDD = +2.7 V to +5.5 V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{11}	SCLK cycle time	60		ns
t_{12}	SCLK low time	25		ns
t_{13}	SCLK high time	25		ns
t_{14}	LATCH delay time	13		ns
t_{15}	LATCH high time	40		ns
t_{16}	Data setup time	5		ns
t_{17}	Data hold time	7		ns
t_{18}	LATCH low time	40		ns
t_{19}	Serial output delay time ($C_{L,\ SDO}$ = 15 pF)		35	ns
t_{20}	LATCH rising edge to SDO 3-state ($C_{L,\ SDO}$ = 15 pF)		35	ns

(1) Specified by design, not production tested.

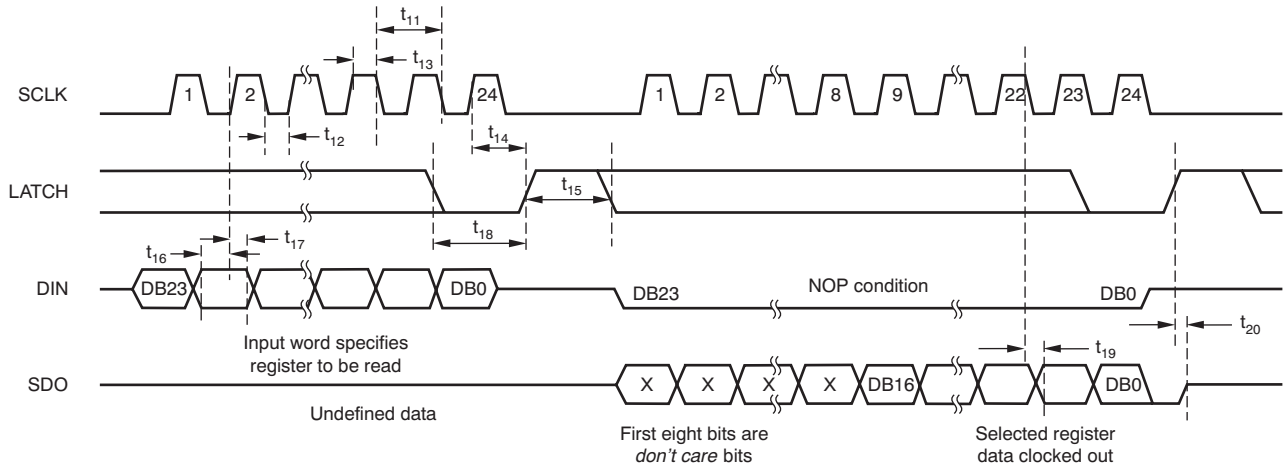

Figure 2. Readback Mode Timing

6.9 Timing Requirements: Daisy-Chain Mode(1)

At T_A = –40°C to +125°C and DVDD = 2.7 V to 5.5 V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{21}	SCLK cycle time	60		ns
t_{22}	SCLK low time	25		ns
t_{23}	SCLK high time	25		ns
t_{24}	LATCH delay time	13		ns
t_{25}	LATCH high time	40		ns
t_{26}	Data setup time	5		ns
t_{27}	Data hold time	7		ns
t_{28}	LATCH low time	40		ns
t_{29}	Serial output delay time ($C_{L,\ SDO}$ = 15 pF)		35	ns

(1) Specified by design, not production tested.

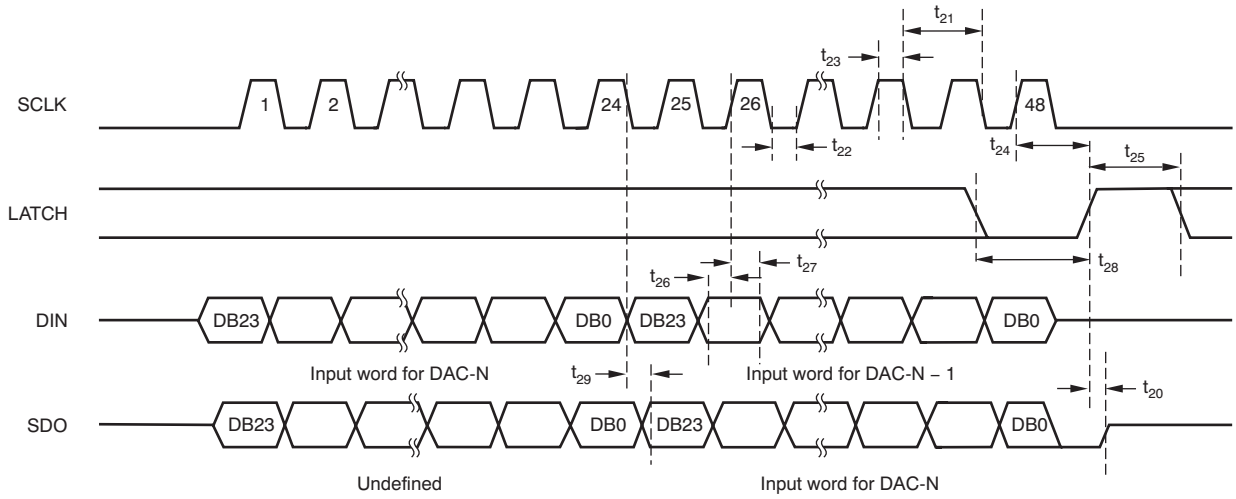

Figure 3. Daisy-Chain Mode Timing

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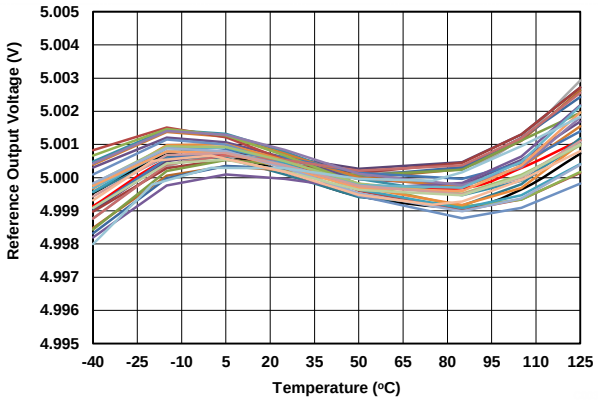
6.10 Typical Characteristics

At T_A = +25°C, unless otherwise noted.



30 units shown AVDD = 24 V

Figure 4. REFOUT vs Temperature

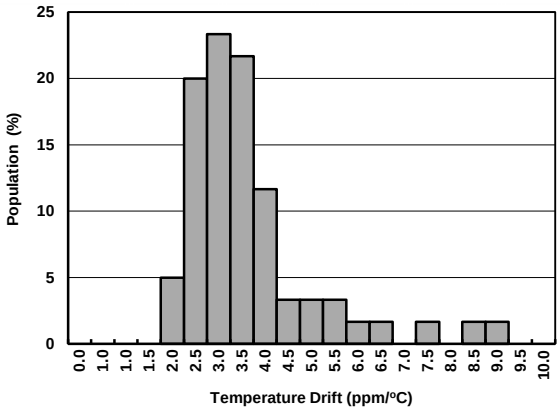
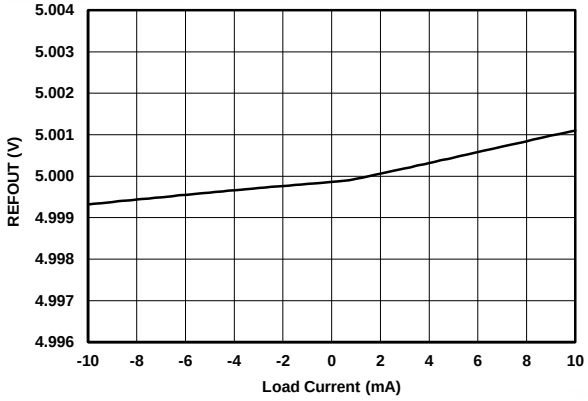
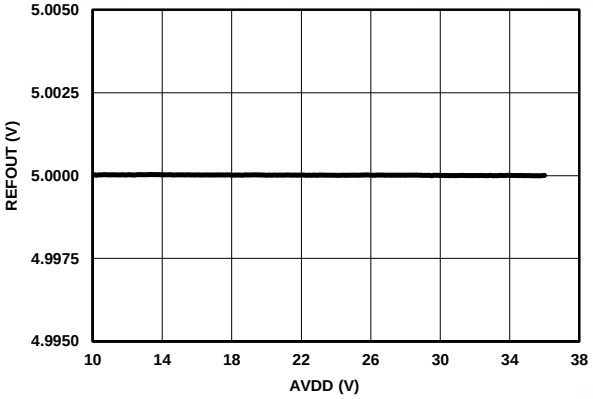


Figure 5. Internal Reference Temperature Drift Histogram



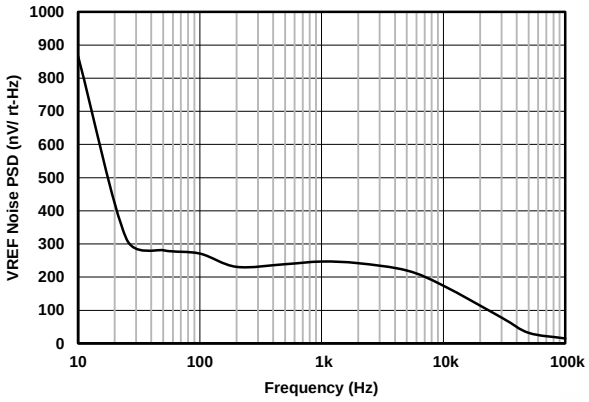
AVDD = 24 V

Figure 6. REFOUT vs Load Current



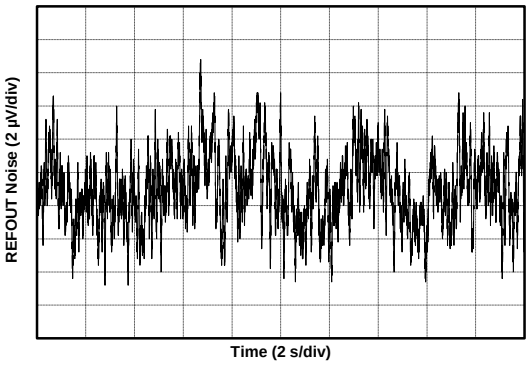
T_A = 25°C

Figure 7. REFOUT vs AVDD



AVDD = 24 V

Figure 8. REFOUT Noise PSD vs Frequency



AVDD = 24 V

Figure 9. Internal Reference, Peak-to-Peak Noise (0.1 Hz to 10 Hz)

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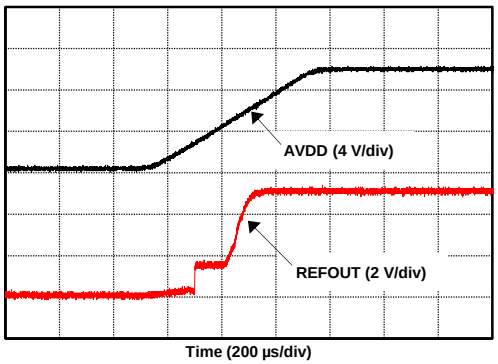
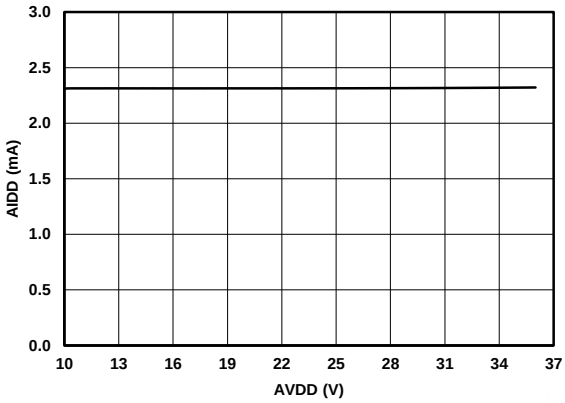
Typical Characteristics (continued)

At T_A = +25°C, unless otherwise noted.



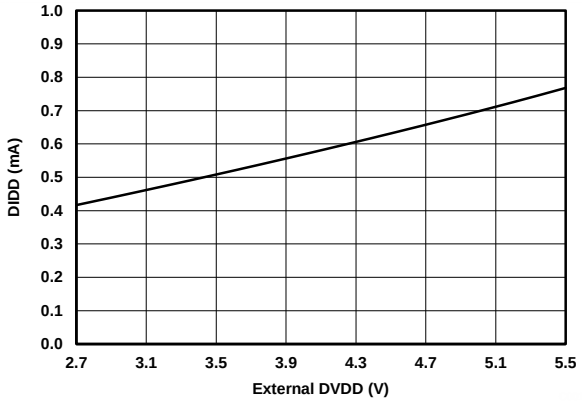
AVDD = 10 V

Figure 10. REFOUT Transient vs Time



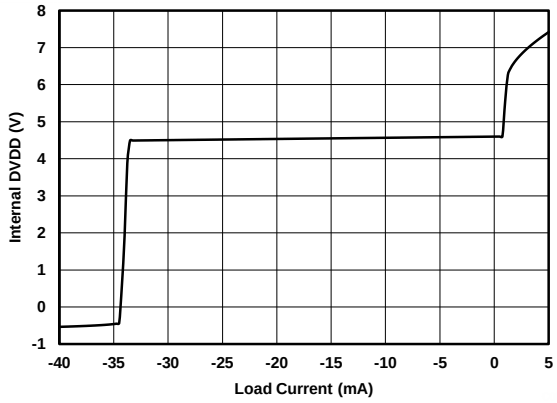
External DVDD IOUT = 0 mA

Figure 11. AIDD vs AVDD



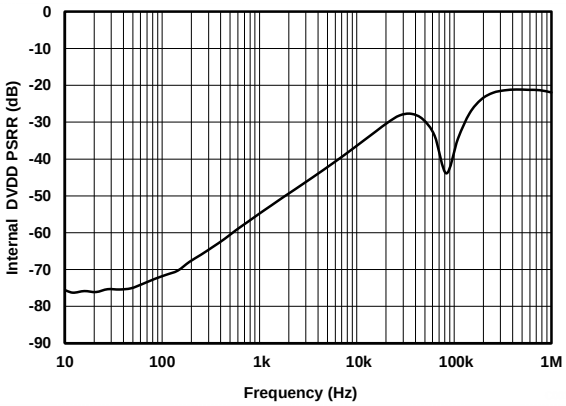
T_A = 25°C External DVDD

Figure 12. DIDD vs External DVDD



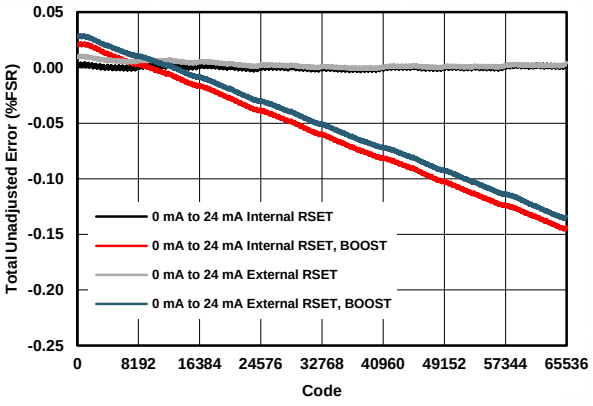
T_A = 25°C Internal DVDD

Figure 13. Internal DVDD vs Load Current



AVDD = 18 V C_{LOAD} = 100 nF

Figure 14. Internal DVDD PSRR vs Frequency



AVDD = 24 V R_{LOAD} = 300 Ω

Figure 15. IOUT TUE vs Code (0 mA to 24 mA)

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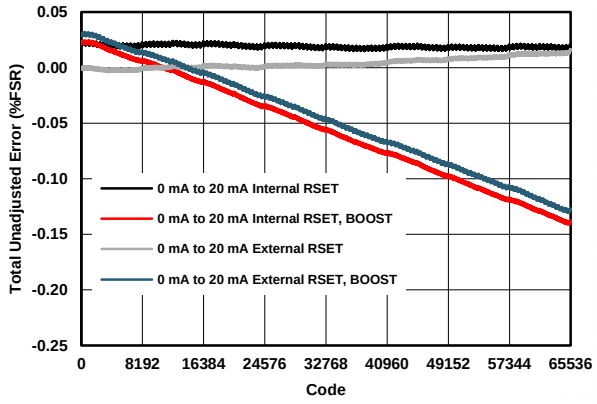
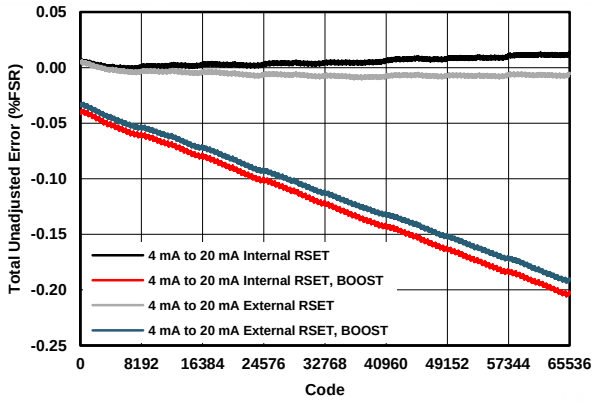
Typical Characteristics (continued)

At T_A = +25°C, unless otherwise noted.



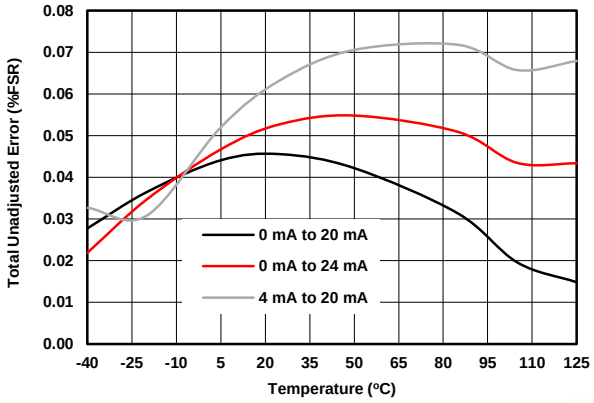
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 16. IOUT TUE vs Code (0 mA to 20 mA)



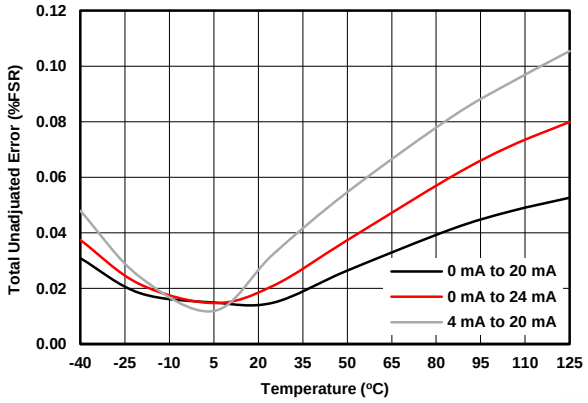
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 17. IOUT TUE vs Code (4 mA to 20 mA)



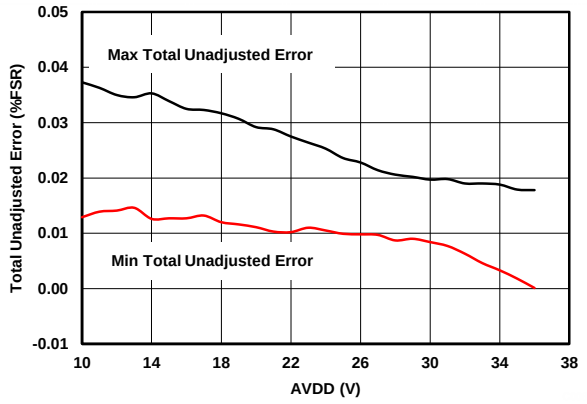
AVDD = 10 V R_{LOAD} = 300 Ω

Figure 18. IOUT TUE vs Temperature (Internal R_{SET})



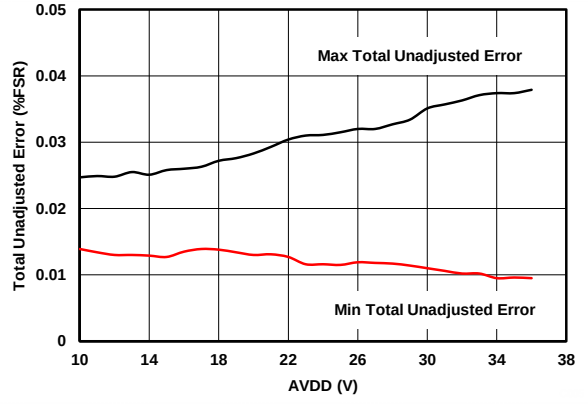
AVDD = 10 V R_{LOAD} = 300 Ω

Figure 19. IOUT TUE vs Temperature (External R_{SET})



R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 20. IOUT TUE vs Supply (Internal R_{SET})



R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 21. IOUT TUE vs Supply (External R_{SET})

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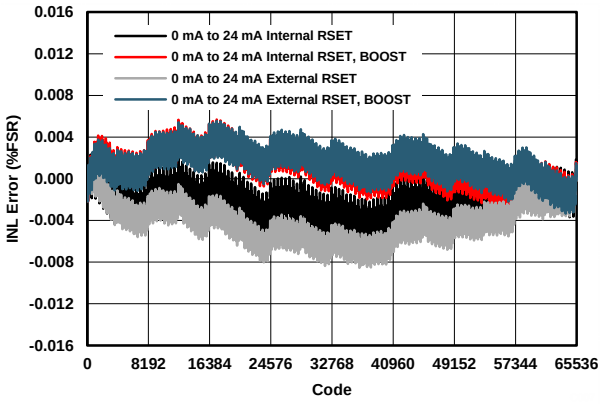
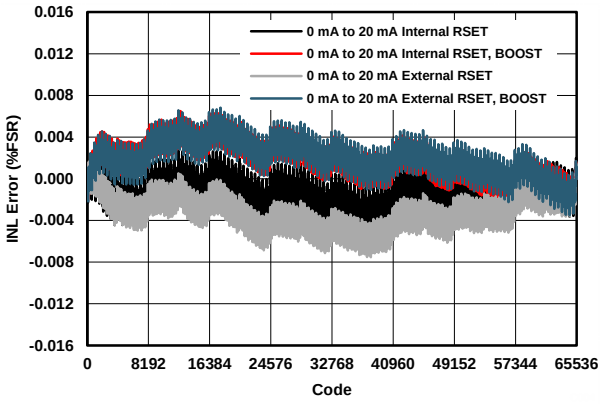
Typical Characteristics (continued)

At T_A = +25°C, unless otherwise noted.



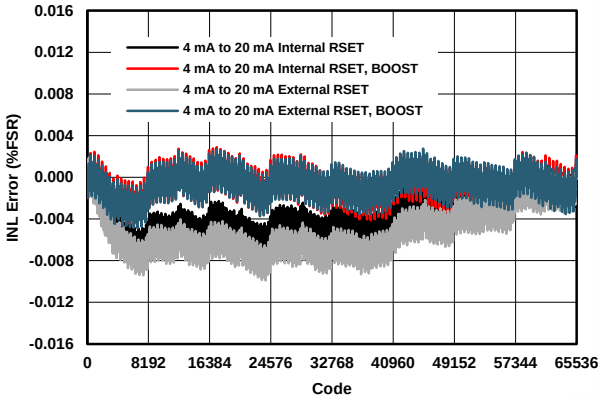
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 22. IOUT INL vs Code (0 mA to 24 mA)



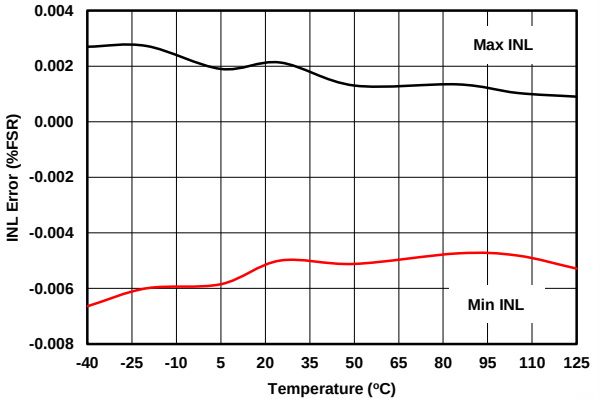
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 23. IOUT INL vs Code (0 mA to 20 mA)



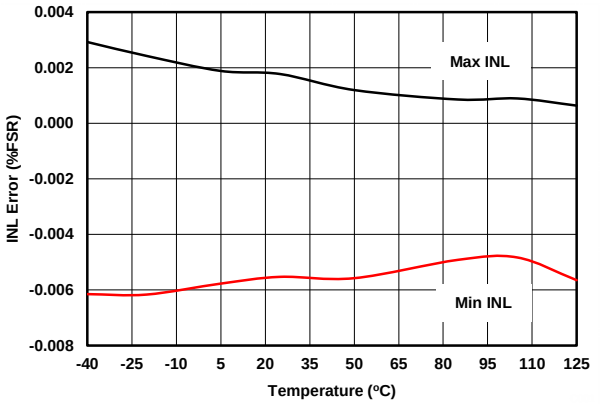
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 24. IOUT INL vs Code (4 mA to 20 mA)



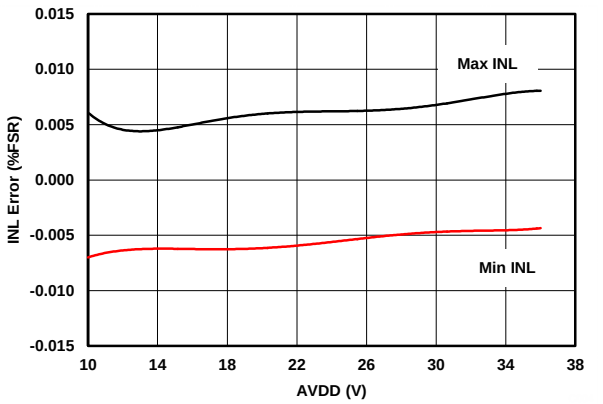
AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

Figure 25. IOUT INL vs Temperature (Internal R_{SET})



AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

Figure 26. IOUT INL vs Temperature (External R_{SET})



R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 27. IOUT INL vs Supply (Internal R_{SET})

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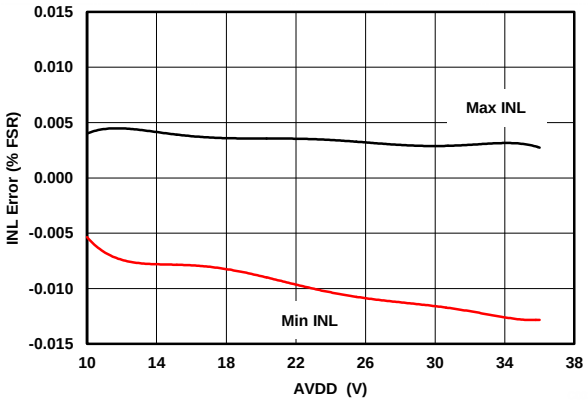
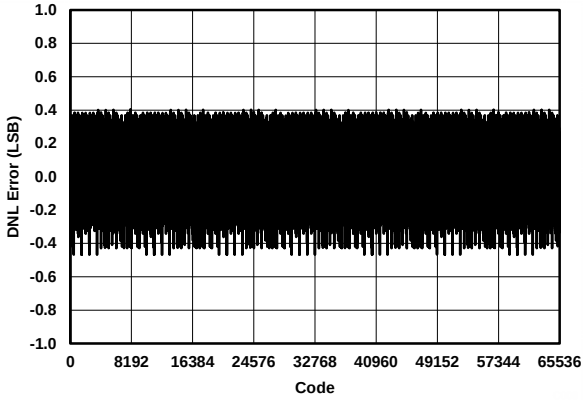
Typical Characteristics (continued)

At T_A = +25°C, unless otherwise noted.



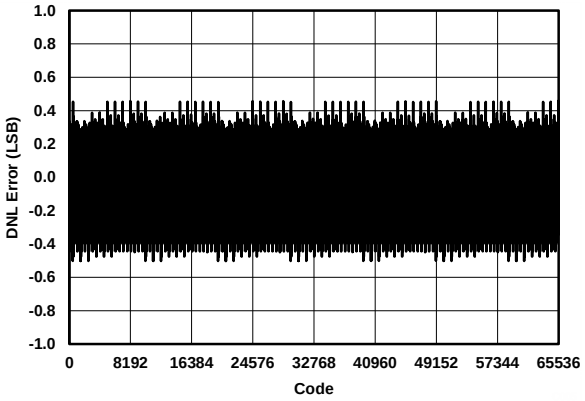
R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 28. IOUT INL vs Supply (External R_{SET})



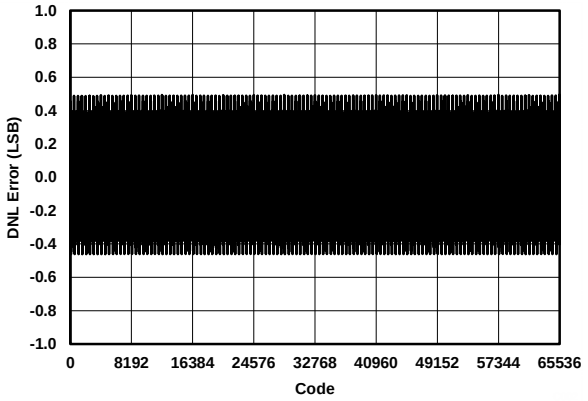
AVDD = 24 V 0-mA to 24-mA range
R_{LOAD} = 300 Ω

Figure 29. IOUT DNL vs Code (0 mA to 24 mA)



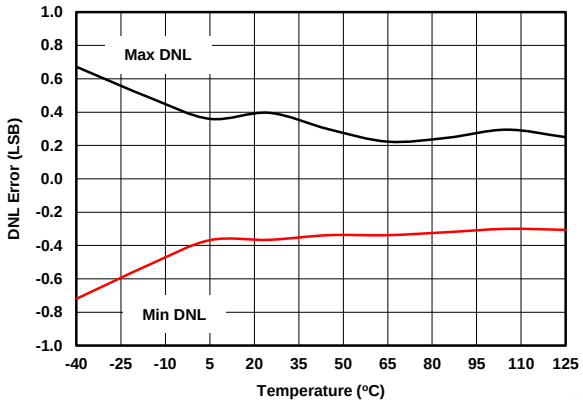
AVDD = 24 V 0-mA to 24-mA range
R_{LOAD} = 300 Ω

Figure 30. IOUT DNL vs Code (0 mA to 20 mA)



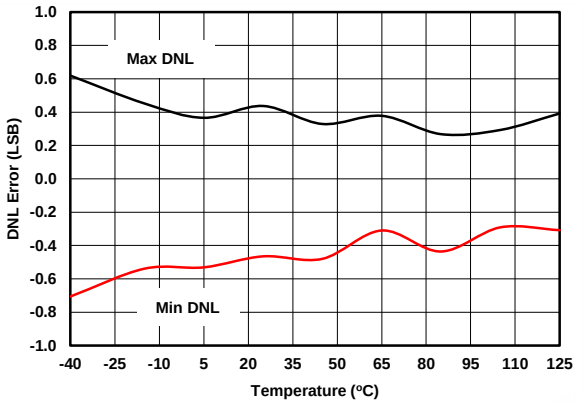
AVDD = 24 V 4-mA to 24-mA range
R_{LOAD} = 300 Ω

Figure 31. IOUT DNL vs Code (4 mA to 20 mA)



AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

Figure 32. IOUT DNL vs Temperature (Internal R_{SET})



AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

Figure 33. IOUT DNL vs Temperature (External R_{SET})

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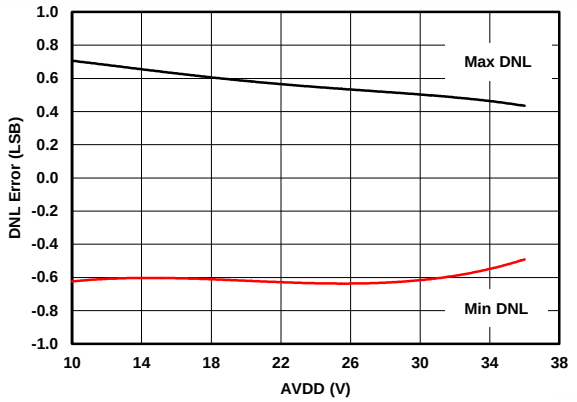
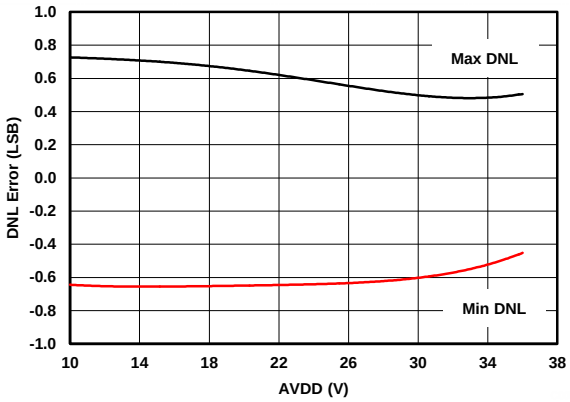
Typical Characteristics (continued)

At T_A = +25°C, unless otherwise noted.



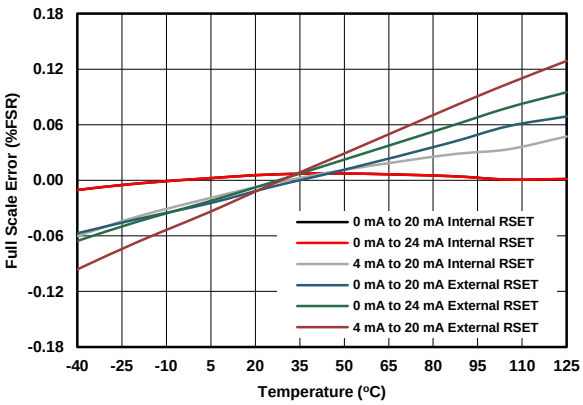
R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 34. IOUT DNL vs Supply (Internal R_{SET})



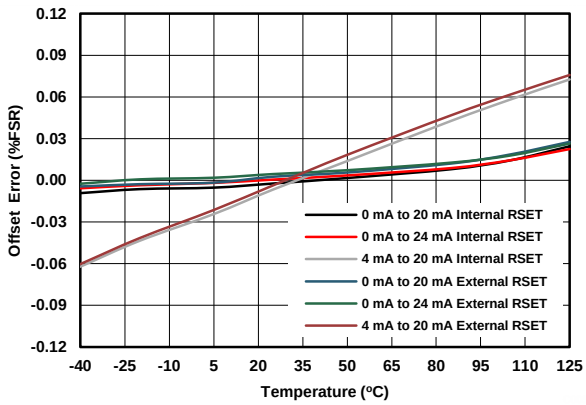
R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 35. IOUT DNL vs Supply (External R_{SET})



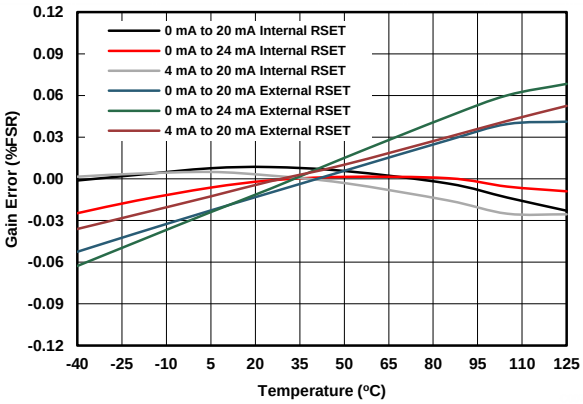
AVDD = 10 V R_{LOAD} = 300 Ω

Figure 36. IOUT Full-Scale Error vs Temperature



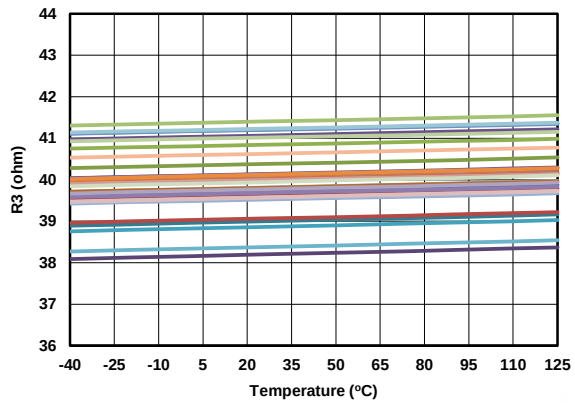
AVDD = 10 V R_{LOAD} = 300 Ω

Figure 37. IOUT Offset Error vs Temperature



AVDD = 10 V R_{LOAD} = 300 Ω

Figure 38. IOUT Gain Error vs Temperature



33 units shown

Figure 39. R3 Resistance vs Temperature

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Typical Characteristics (continued)

At T_A = +25°C, unless otherwise noted.

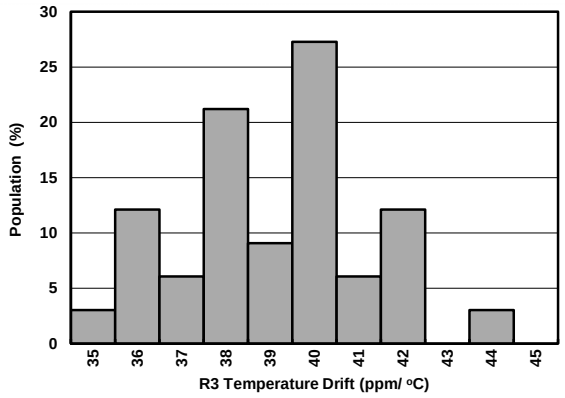
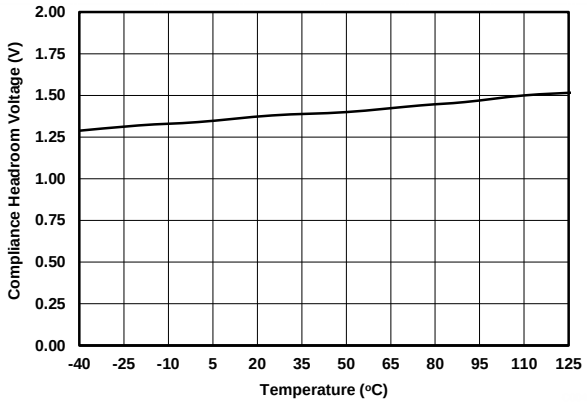
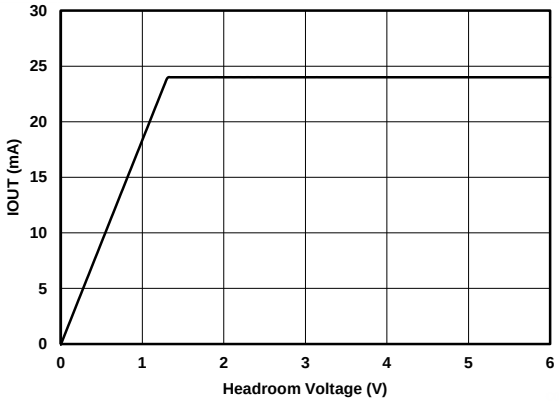


Figure 40. R3 Resistance Temperature Drift Histogram



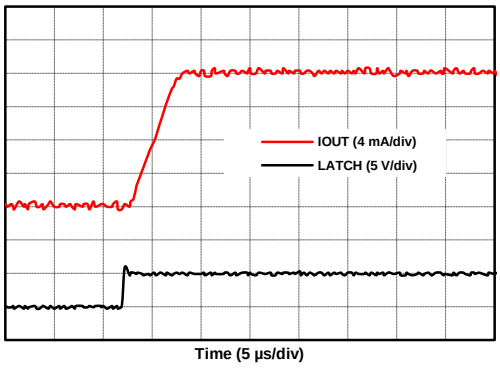
AVDD = 36 V IOUT = 24 mA R_{LOAD} = 300 Ω

Figure 41. Compliance Headroom Voltage(1) vs Temperature



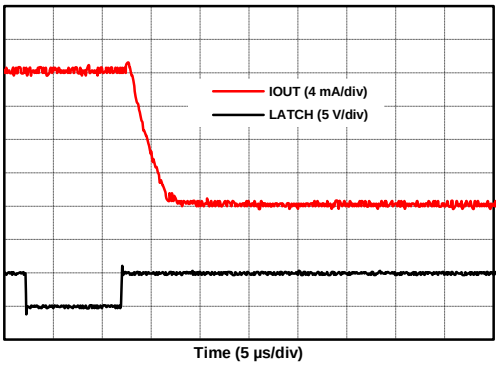
AVDD = 36 V DAC configured to deliver 24 mA
R_{LOAD} = 300 Ω

Figure 42. IOUT vs Compliance Headroom Voltage(1)



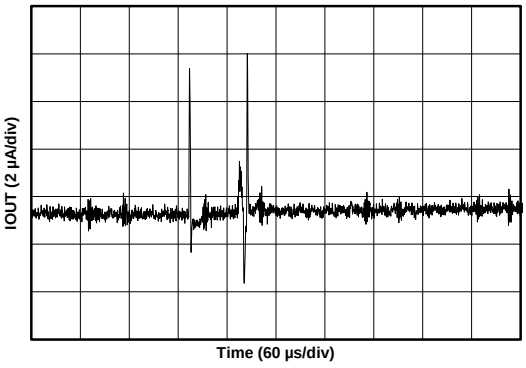
AVDD = 24 V 4-mA to 20-mA range
R_{LOAD} = 300 Ω From code: 0x0000 To code: 0xFFFF

Figure 43. 4-mA to 20-mA Rising



AVDD = 24 V 4-mA to 20-mA range
R_{LOAD} = 300 Ω From code: 0xFFFF To code: 0x0000

Figure 44. 4-mA to 20-mA Falling



AVDD = 24 V R_{LOAD} = 300 Ω

Figure 45. IOUT Power-On Glitch

1. Compliance voltage headroom is defined as the drop from AVDD terminal to the IOUT terminal.

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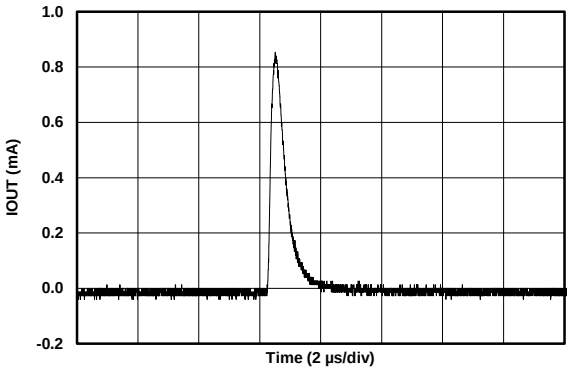
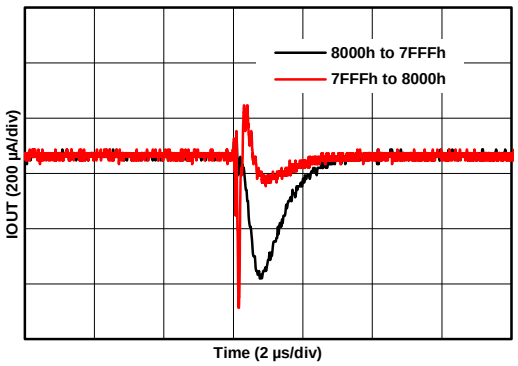
Typical Characteristics (continued)

At T_A = +25°C, unless otherwise noted.



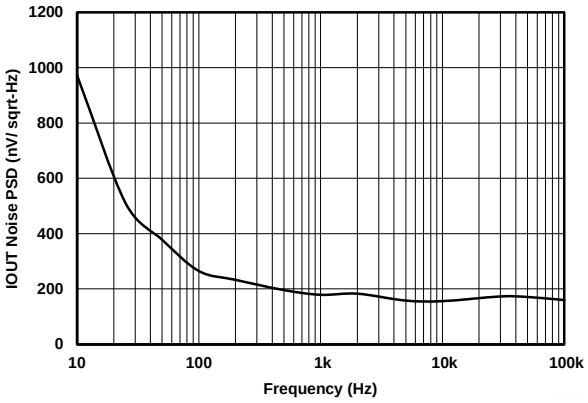
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 46. IOUT Output Enable Glitch



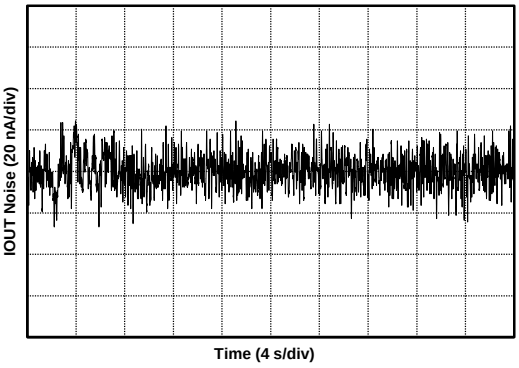
AVDD = 24 V R_{LOAD} = 250 Ω

Figure 47. IOUT Digital-to-Analog Glitch



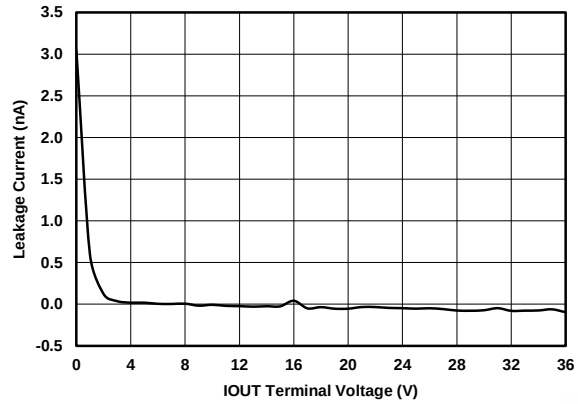
AVDD = 24 V R_{LOAD} = 300 Ω All IOUT ranges

Figure 48. IOUT Noise PSD vs Frequency



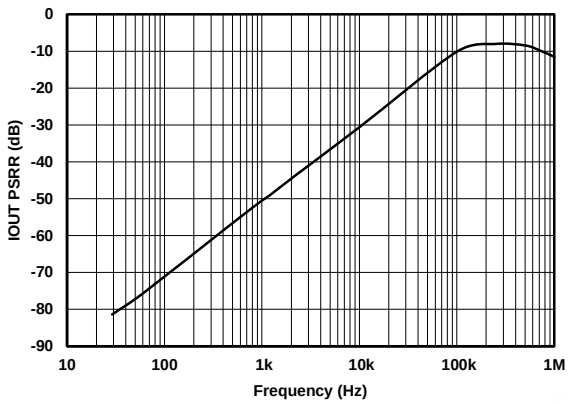
AVDD = 24 V 0-mA to 20-mA range
DAC = midscale

Figure 49. IOUT Peak-to-Peak Noise vs Time (0.1 Hz to 10 Hz)



AVDD = 36 V Output disabled

Figure 50. IOUT Hi-Z Leakage Current vs Voltage



AVDD = 24 V R_{LOAD} = 250 Ω All IOUT ranges

Figure 51. IOUT PSRR vs Frequency

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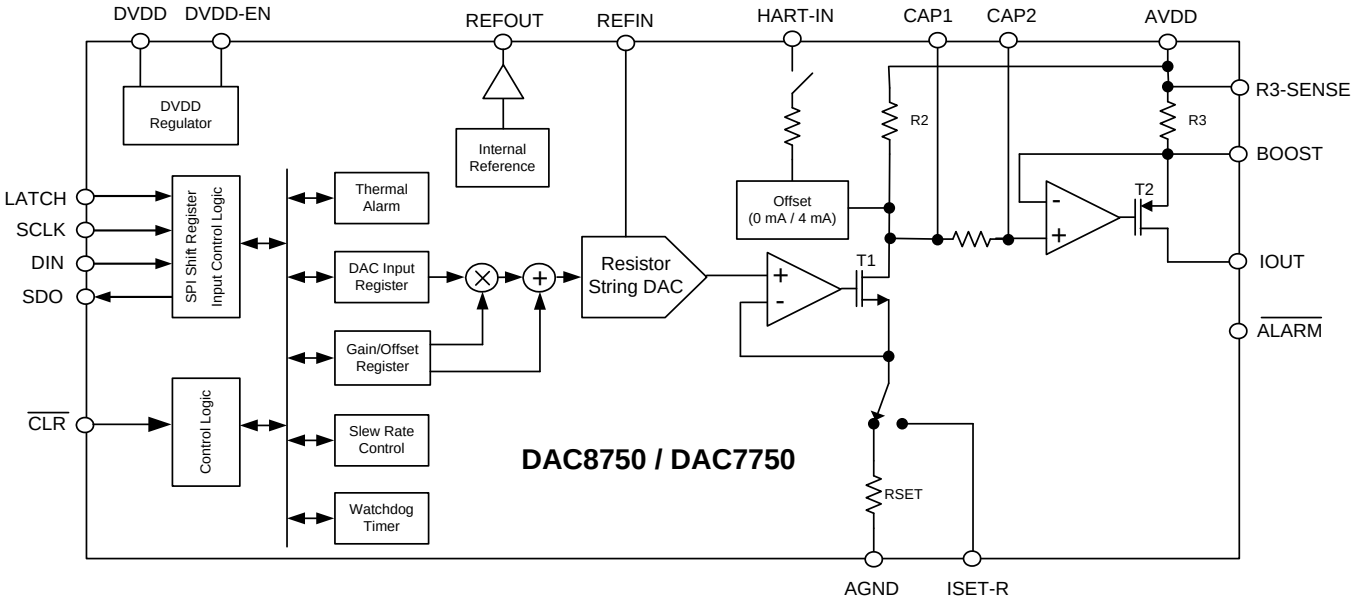
7 Detailed Description

7.1 Overview

The DAC8750 and DAC7750 (DACx750) consist of a resistor-string digital-to-analog converter (DAC) followed by a voltage-to-current conversion stage. The voltage-to-current conversion stage includes a precision-trimmed, low-drift, current-setting resistor, as well as an optional setting to use an external resistor. An integrated low-drift, 5-V reference, as well as an on-chip voltage regulator to provide a digital supply (DVDD) are also included. Alarms exist to indicate fault conditions on the current output or the die temperature.

The device is controlled over a four-wire serial peripheral interface (SPI) with an option to daisy-chain multiple devices. Fault conditions on the interface can be monitored by a CRC error on the SPI frame, as well as a watchdog timer. An asynchronous clear function along with internal power-on-reset circuits are provided to set the current output to a known state. Other features include a user gain and offset calibration (digital only), a programmable slew rate, and the option to use an external transistor for the current output. In addition, the output current can be monitored through access to an internal sense resistor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DAC Architecture

The resistor-string section is simply a string of resistors, each with the same value, from REFIN to GND, as Figure 52 illustrates. This type of architecture makes sure the DAC is monotonic. The 16-bit (DAC8750) or 12-bit (DAC7750) binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before it is fed into the voltage-to-current conversion stage. The current-output stage converts the voltage output from the string to current. When the output is disabled, it is in a high-impedance (Hi-Z) state. After power-on, the output is disabled.

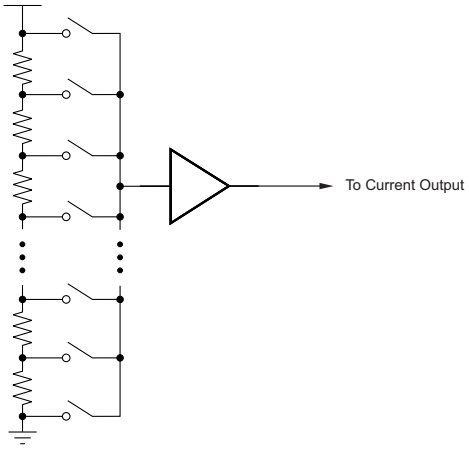


Figure 52. DAC Structure: Resistor String

7.3.2 Current Output Stage

The current output stage consists of a preconditioner and a current source, as illustrated in Figure 53. This stage provides a current output according to the DAC code. The output range can be programmed as 0 mA to 20 mA, 0 mA to 24 mA, or 4 mA to 20 mA. Use an external transistor to reduce the power dissipation of the device. The maximum compliance voltage on IOUT equals (AVDD – 2 V). In single power-supply mode, the maximum AVDD is 36 V, and the maximum compliance voltage is 34 V. After power on, the IOUT terminal is in a Hi-Z state.

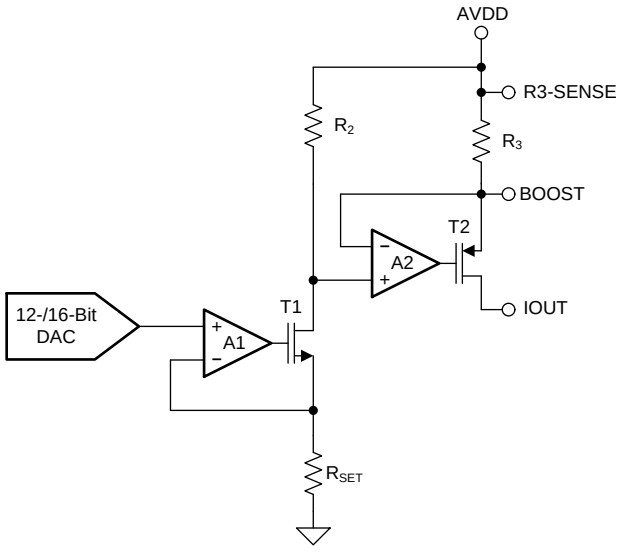


Figure 53. Current Output

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Feature Description (continued)

For a 5-V reference, the output can be expressed as shown in Equation 1 through Equation 3.

For a 0-mA to 20-mA output range:

$$IOUT = 20mA \bullet \frac{CODE}{2^N} \quad (1)$$

For a 0-mA to 24-mA output range:

$$IOUT = 24mA \bullet \frac{CODE}{2^N} \quad (2)$$

For a 4-mA to 20-mA output range:

$$IOUT = 16mA \bullet \frac{CODE}{2^N} + 4mA \quad (3)$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16 for DAC8750, and 12 for DAC7750.

The current-output range is normally set according to the value of the RANGE bits in the Control Register. Refer to the *Setting Current-Output Ranges* section for more details.

7.3.3 Serial Peripheral Interface (SPI)

The device is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, Microwire, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits. The timing for the digital interface is shown in Figure 1, Figure 2, and Figure 3.

7.3.3.1 SPI Shift Register

The default frame is 24 bits wide (refer to the *Frame Error Checking* section for 32-bit frame mode) and begins with the rising edge of SCLK that clocks in the MSB. The subsequent bits are latched on successive rising edges of SCLK. The default 24-bit input frame consists of an 8-bit address byte followed by a 16-bit data word as shown in Table 1.

Table 1. Default SPI Frame

BIT 23:BIT 16	BIT 15:BIT 0
Address byte	Data word

The host processor must issue 24 bits before it issues a rising edge on the LATCH terminal. Input data bits are clocked in regardless of the LATCH terminal and are unconditionally latched on the rising edge of LATCH. By default, the SPI shift register resets to 0x000000 at power on or after a reset.

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7.3.3.2 Write Operation

A write operation is accomplished when the address byte is set according to Table 2. For more information on the DACx750 registers, see the *Register Map* section.

Table 2. Write Address Functions

ADDRESS BYTE (HEX)	FUNCTION
00	No operation (NOP)
01	Write DAC Data register
02	Register read
55	Write control register
56	Write reset register
57	Write configuration register
58	Write DAC gain calibration register
59	Write DAC zero calibration register
95	Watchdog timer reset

7.3.3.3 Read Operation

A read operation is accomplished when the address byte is 0x02. Follow the read operation with a no-operation (NOP) command to clock out an addressed register, as shown in Figure 2. To read from a register, the address byte and data word is as shown in Table 3. The read register value is output MSB first on SDO on successive falling edges of SCLK.

Table 3. Default SPI Frame for Register Read

ADDRESS BYTE (HEX)	DATA WORD	
	BIT 15:BIT 6	BIT 5:BIT 0
02	X (*don't care*)	Register read address (see Table 4)

Table 4 shows the register read addresses available on the DACx750 devices.

Table 4. Register Read Address Functions

READ ADDRESS(1)	FUNCTION
XX XX00	Read status register
XX XX01	Read DAC data register
XX XX10	Read control register
00 1011	Read configuration register
01 0011	Read DAC gain calibration register
01 0111	Read DAC zero calibration register

(1) X denotes *don't care* bits.

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7.3.3.4 Stand-Alone Operation

SCLK can operate in either continuous or burst mode, as long as the LATCH rising edge occurs after the appropriate number of SCLK cycles. Providing more than or less than 24 SCLK cycles before the rising edge of LATCH results in incorrect data being programmed into the device registers, and incorrect data sent out on SDO. The rising edge of SCLK that clocks in the MSB of the 24-bit input frame marks the beginning of the write cycle, and data are written to the addressed registers on the rising edge of LATCH.

7.3.3.5 Daisy-Chain Operation

For systems that contain multiple DACx750s, use the SDO terminal to daisy-chain several devices. This mode is useful in reducing the number of serial interface lines in applications that use multiple SPI devices. Daisy-chain mode is enabled by setting the DCEN bit of the control register to 1. By connecting the SDO of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed, as Figure 54 illustrates.

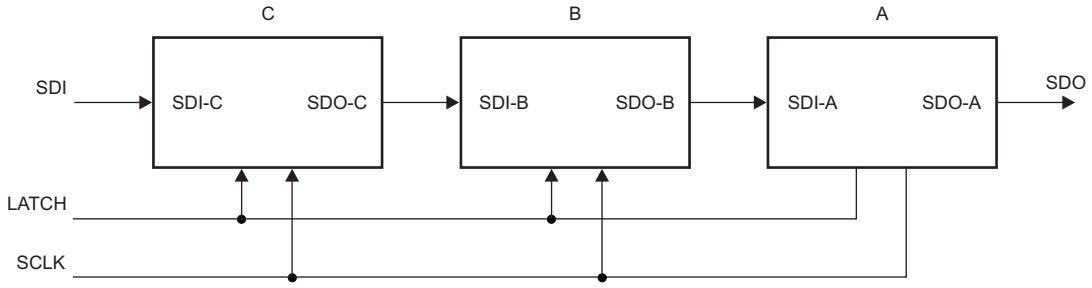

Figure 54. Three DACx750s in Daisy-Chain Mode

Like stand-alone operation, the SPI daisy-chain write operation requires one frame, and the read requires two frames. The rising edge of SCLK that clocks in the MSB of the input frame marks the beginning of the write cycle. When the serial transfer to all devices is complete, LATCH is taken high. This action transfers the data from the SPI shift registers to the device internal register of each DACx750 in the daisy-chain. However, the number of clocks in each frame in this case depends on the number of devices in the daisy chain. For two devices, each frame is 48 clocks; the first 24 clocks are for the second DAC and the next 24 bits are for the first DAC. For a readback, the data are read from the two DACs in the following 48-bit frame; the first 24 clocks are for the second DAC, and the next 24 clocks are for the first DAC. The input data to the DACs during the second frame can be another command or NOP. Similar to the two-device case described, for N devices, each frame is N × 24 clocks, where *N* is the total number of DACx750s in the chain.

The serial clock can be a continuous or gated clock. A continuous SCLK source can only be used if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data.

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7.3.4 Internal Reference

The DACx750 includes an integrated 5-V reference with a buffered output (REFOUT) capable of driving up to 5 mA (source or sink) with an initial accuracy of ±5 mV maximum and a temperature drift coefficient of 10 ppm/°C maximum.

7.3.5 Digital Power Supply

An internally generated 4.6-V supply capable of driving up to 10 mA can be output on DVDD by leaving the DVDD-EN terminal unconnected. This eases the system power supply design when an isolation barrier needs to be crossed to generate the digital supply. It can be used to drive isolation components used for the digital data lines and other miscellaneous components like references and temp sensors; see Figure 62 for an example application.

If an external supply is preferred, the DVDD terminal (which can be driven up to 5.5 V in this case) can become an input by tying DVDD-EN to GND. Refer to Electrical Characteristics for detailed specifications.

7.3.6 DAC Clear

The DAC has an asynchronous clear function through the CLR terminal that is active-high and allows the current output to be cleared to zero-scale code. When the CLR signal returns to low, the output remains at the cleared value. The preclear value can be restored by pulsing the LATCH signal without clocking any data. A new value cannot be programmed until the CLR terminal returns to low. To avoid glitches on the output, disable the output by writing a 0 to the OUTEN bit of the Control Register before changing the current range.

7.3.7 Power-Supply Sequence

The DACx750 has internal power on reset (POR) circuitry for both the digital DVDD and analog AVDD supplies. This circuitry makes sure that the internal logic and power-on state of the DAC power up to the proper state, independent of the supply sequence. While there is no required supply power-on sequence, the recommendation is to first have the digital DVDD supply power on, followed by the analog AVDD supply.

7.3.8 Power-On Reset

The DACx750 incorporates two internal POR circuits for the DVDD and AVDD supplies. The DVDD and AVDD POR signals are ANDed together so that both supplies must be at their minimal specified values for the device to *not* be in a reset condition. These POR circuits initialize internal logic and registers, as well as set the analog outputs to a known state while the device supplies are ramping. All registers are reset to their default values. Typically the POR function can be ignored, as long as the device supplies power-up and maintains the specified minimum voltage levels. However, in the case of a supply drop or brownout, the DACx750 can have an internal POR reset event or lose digital memory integrity. Figure 55 represents the threshold levels for the internal POR for both the DVDD and AVDD supplies.

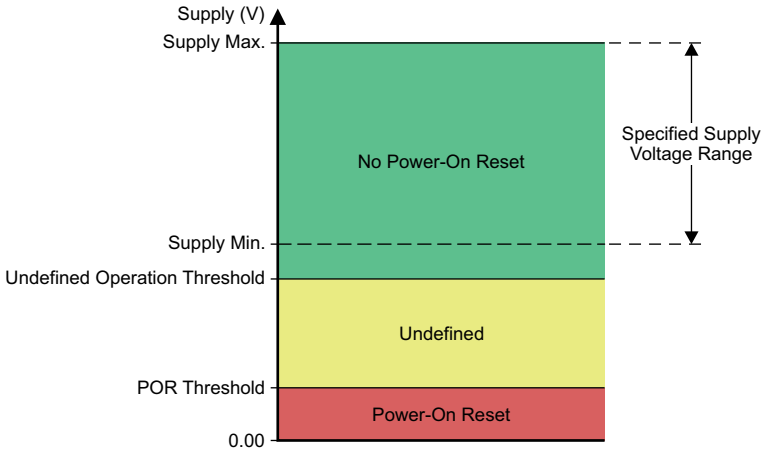

Figure 55. Relevant Voltage Levels for POR Circuit

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For the DVDD supply, no internal POR occurs for nominal supply operation from 2.7 V (supply min) to 5.5 V (supply max). For the DVDD supply region between 2.4 V (undefined operation threshold) and 0.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the DVDD supply below 0.8 V (POR threshold), the internal POR resets if the supply voltage remains less than 0.8 V for approximately 1 ms.

For the AVDD supply, no internal POR occurs for nominal supply operation from 10 V (supply min) to 36 V (supply max). For AVDD supply voltages between 8 V (undefined operation threshold) and 1 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the AVDD supply below 1 V (POR threshold), the internal POR resets if the supply voltage remains less than 1 V for approximately 1 ms. In case the DVDD or AVDD supply drops to a level where the internal POR signal is indeterminate, either power cycle the device, or toggle the LATCH terminal and then perform a software reset. Both options initialize the internal circuitry to a known state and provide proper operation.

7.3.9 Alarm Detection

These devices also provide an alarm detection feature. When one or more of following events occur, the $\overline{\text{ALARM}}$ terminal goes low:

- The current output load is in open circuit; or
- The voltage at IOUT reaches a level where accuracy of the output current is compromised. This condition is detected by monitoring internal voltage levels of the IOUT circuitry and is typically below the specified compliance voltage headroom (defined as the voltage drop between the AVDD and IOUT terminals) minimum of 2 V; or
- The die temperature has exceeded +142°C; or
- The SPI watchdog timer exceeded the timeout period (if enabled); or
- The SPI frame error CRC check encountered an error (if enabled).

When the $\overline{\text{ALARM}}$ terminals of multiple DACx750 devices are connected together to form a wired-AND function, the host processor must read the status register of each device to know all the fault conditions that are present. Note that the thermal alarm has hysteresis of approximately 18°C. After being set, the alarm only resets when the die temperature drops below +124°C.

7.3.10 Watchdog Timer

This feature is useful to make sure that communication between the host processor and the DACx750 has not been lost. It can be enabled by setting the WDEN bit of the Configuration Register to 1. The watchdog timeout period can be set using the WDPD bits of the configuration register, as shown in Table 5. The timer period is based off an internal oscillator with a typical value of 8 MHz.

Table 5. Watchdog Timeout Period

WDPD BITS	WATCHDOG TIMEOUT PERIOD (Typical)
00	10 ms
01	51 ms
10	102 ms
11	204 ms

If the watchdog timer is enabled, these devices must have an SPI frame with 0x95 as the write address byte written to the device within the programmed timeout period. Otherwise, the $\overline{\text{ALARM}}$ terminal asserts low and the WD-FLT bit of the status register is set to 1. Note that the $\overline{\text{ALARM}}$ terminal can be asserted low for any of the different conditions as explained in the *Alarm Detection* section. The WD-FLT bit is reset to 0 with a software reset, by disabling the watchdog timer, or by powering down the device.

When using multiple DACx750 devices in a daisy-chain configuration, the open-drain $\overline{\text{ALARM}}$ terminals of all devices can be connected together in a wired-AND function. The watchdog timer can be enabled in any number of the devices in the chain although enabling it in one device is sufficient. The wired-AND $\overline{\text{ALARM}}$ terminal may get pulled low because of the simultaneous presence of different trigger conditions in the daisy-chained devices. The host processor reads the status register of each device to know all the fault conditions present in the chain.

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7.3.11 Frame Error Checking

In noisy environments, error checking can be used to check the integrity of SPI data communication between the DACx750 and the host processor. To enable this feature, set the CRCEN bit of the Configuration Register to 1. The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, *100000111*). When error checking is enabled, the SPI frame width is 32 bits, as shown in Table 6. Start with the default 24-bit frame, enable frame error checking, and then switch to the 32-bit frame. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding to the device. For a register readback, the CRC polynomial is output on the SDO terminals by the device as part of the 32-bit frame.

Table 6. SPI Frame with Frame Error Checking Enabled

BIT 31:BIT 8	BIT 7:BIT 0
Normal SPI frame data	8-bit CRC polynomial

The DACx750 decodes the 32-bit input frame data to compute the CRC remainder. If no error exists in the frame, the CRC remainder is zero. When the remainder is non-zero (that is, the input frame has single- or multiple-bit errors), the $\overline{\text{ALARM}}$ terminal asserts low and the CRC-FLT bit of the status register is set to 1. The $\overline{\text{ALARM}}$ terminal can be asserted low for any of the different conditions as explained in the *Alarm Detection* section. The CRC-FLT bit is reset to 0 with a software reset, by disabling the frame error checking, or by powering down the device. In the case of a CRC error, the specific SPI frame is blocked from writing to the device.

Frame error checking can be enabled for any number of DACx750 devices connected in a daisy-chain configuration. However, it is recommended to enable error checking for either none or all devices in the chain. When connecting the $\overline{\text{ALARM}}$ terminals of multiple devices, forming a wired-AND function, the host processor reads the status register of each device to know all the fault conditions present in the chain. For proper operation, the host processor must provide the correct number of SCLK cycles in each frame, taking care to identify whether or not error checking is enabled in each device in the daisy-chain.

7.3.12 User Calibration

The device implements a user-calibration function (enabled by the CALEN bit in the Configuration Register) to trim system gain and zero errors. The DAC output is calibrated according to the value of the gain calibration and zero calibration registers. The range of gain adjustment is typically ±50% of full-scale with 1 LSB per step. The gain register must be programmed to 0x8000 to achieve the default gain of 1 because the power-on value of the register is 0x0000, equivalent to a gain of 0.5. The zero code adjustment is typically ±32,768 LSBs with 1 LSB per step. The input data format of the gain register is unsigned straight binary, and the input data format of the zero register is twos complement. The gain and offset calibration is described by Equation 4:

$$\text{CODE_OUT} = \text{CODE} \bullet \frac{\text{User_GAIN} + 2^{15}}{2^{16}} + \text{User_ZERO} \quad (4)$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC data register at address 0x01.
- *N* is the bits of resolution; 16 for DAC8750 and 12 for DAC7750.
- *User_ZERO* is the signed 16-bit code in the zero register.
- *User_GAIN* is the unsigned 16-bit code in the gain register.
- *CODE_OUT* is the decimal equivalent of the code loaded to the DAC (limited between 0x0000 to 0xFFFF for DAC8750 and 0x000 to 0xFFF for DAC7750).

This is a purely digital implementation and the output is still limited by the programmed value at both ends of the current output range (set by the RANGE bits, as described in the *Setting Current-Output Ranges* section). In addition, the correction only makes sense for endpoints inside of the true device end points. To correct more than just the actual device error, for example a system offset, the valid range for the adjustment changes accordingly and must be taken into account.

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7.3.13 Programmable Slew Rate

The slew rate control feature controls the rate at which the output current changes. With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the slew rate control feature through bit 4 of the Control Register. With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by bits [7:5] (SRSTEP) and bits [11:8] (SRCLK) of the Control Register. SRCLK defines the rate at which the digital slew updates; SRSTEP defines the amount by which the output value changes at each update. If the DAC data register is read while the DAC output is still changing, the instantaneous value is read. Table 7 lists the slew rate step-size options. Table 8 summarizes the slew rate update clock options.

Table 7. Slew Rate Step-Size (SRSTEP) Options

SRSTEP	STEP SIZE (LSB)	
	DAC7750	DAC8750
000	0.0625	1
001	0.125	2
010	0.125	4
011	0.5	8
100	1	16
101	2	32
110	4	64
111	8	128

Table 8. Slew Rate Update Clock (SRCLK) Options

SRCLK	DAC UPDATE FREQUENCY (Hz)
0000	258,065
0001	200,000
0010	153,845
0011	131,145
0100	115,940
0101	69,565
0110	37,560
0111	25,805
1000	20,150
1001	16,030
1010	10,295
1011	8,280
1100	6,900
1101	5,530
1110	4,240
1111	3,300

The time required for the output to slew over a given range is expressed as Equation 5:

$$\text{Slew Time} = \frac{\text{Output Change}}{\text{Step Size} \cdot \text{Update Clock Frequency} \cdot \text{LSB Size}} \quad (5)$$

where

- *Slew Time* is expressed in seconds
- *Output Change* is expressed in amps (A) for IOUT or volts (V) for VOUT

When the slew rate control feature is enabled, all output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. If the CLR terminal is asserted, the output slews to the zero-scale value at the programmed slew rate. Bit 1 (SR-ON) of the Status Register can be read to verify that the slew operation has completed. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. Figure 56 shows an example of IOUT slewing at a rate set by the above described parameters. In this example for the DAC8750 (LSB size of 305 nA for the 0-mA to 20-mA range), the settings correspond to an update clock frequency of 6.9 kHz and a step size of 128 LSB. As is shown in the case with no capacitors on CAP1 or CAP2, the steps occur at the update clock frequency (6.9 kHz corresponds to a period close to 150 µs), and the size of each step is approximately 38 µA (128 × 305 nA). Calculate the slew time for a specific code change by using Equation 5.

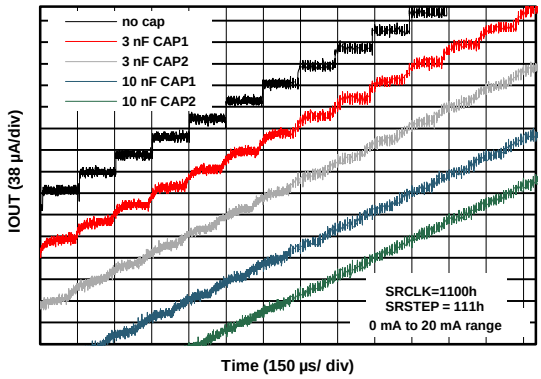

Figure 56. IOUT vs Time with Digital Slew Rate Control

7.3.14 Filtering The Current Output

The DACx750 provides access to internal nodes of the circuit as shown in Figure 60. Place capacitors on these terminals and AVDD to form a filter on the output current, reducing bandwidth and the slew rate of the output, especially useful for driving inductive loads. However, to achieve large reductions in slew rate, use the programmable slew rate to avoid having to use large capacitors. Even in that case, use the capacitors on CAP1 and CAP2 to smooth out the stairsteps caused by the digital code changes as shown in Figure 57. However, note that power supply ripple also couples into the devices through these capacitors.

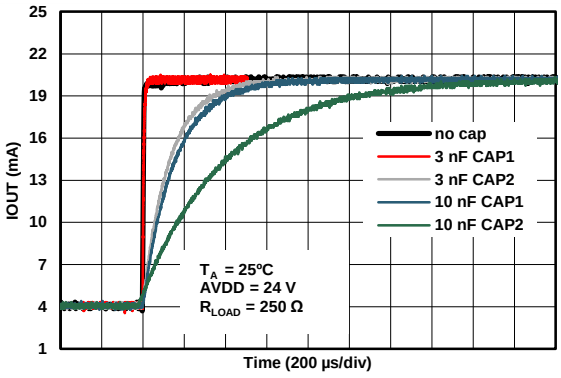

Figure 57. IOUT vs Time for Different Cap Values on CAP1 and CAP2

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7.3.15 Output Current Monitoring

Many applications, especially for functional safety, require monitoring of the output current to ensure it stays close to the programmed value. Place a sense resistor in series to the output to measure the voltage across it. However, this resistor reduces the compliance voltage available for the load. The DACx750 provides access to an internal precision resistor (R3 in Figure 53) through the R3-SENSE and BOOST terminals to perform analog readback for monitoring the output current. Measure the voltage between the R3-SENSE and BOOST terminals and divide by the value of the R3 resistor to determine the magnitude of the output current. The R3 resistor has a typical value of 40 Ω (see Figure 39 for a plot of resistance versus temperature) with a temperature drift coefficient of 40 ppm/°C (see Figure 40 for a histogram of R3 resistance temperature drift). The R3 resistor is tested to stay within the minimum (36 Ω) and maximum (44 Ω) resistance values shown in the *R3 Resistor* section of Electrical Characteristics. To remove the tolerance error, perform a simple calibration by programming a certain value of output current, measuring the voltage across R3-SENSE and BOOST, and calculating the exact value of R3.

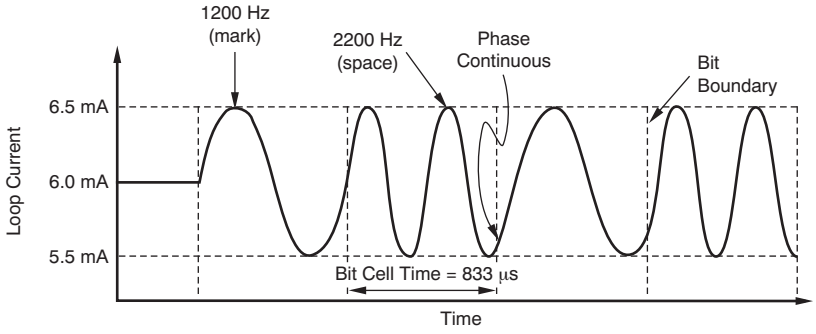
7.3.16 HART Interface

On the DACx750, HART digital communication can be modulated onto the input signal by the methods shown in the following subsections. For more detail, see Application Report SLAA572, *Implementing HART Communication with the DAC8760 Family.*

7.3.16.1 Implementing HART in 4-mA to 20-mA Mode

This method is limited to the case where the RANGE bits of the Control Register are programmed to the 4-mA to 20-mA range. Some applications require going beyond the 4-mA to 20-mA range. In those cases, refer to the methods described in the next subsection.

The external HART signal (ac voltage; 500 mV_{PP}, 1200 Hz, and 2200 Hz) can be capacitively coupled in through the HART-IN terminal and transferred to a current that is superimposed on the 4-mA to 20-mA current output. The HART-IN terminal has a typical input impedance of 35 kΩ that together with the input capacitor used to couple the external HART signal, forms a filter to attenuate frequencies beyond the HART band-pass region. In addition to this filter, an external passive filter is recommended to complete the filtering requirements of the HART specifications. Figure 58 illustrates the output current versus time operation for a typical HART signal. Table 9 specifies the performance of the HART-IN terminal.



NOTE: DC current = 6 mA.

Figure 58. Output Current vs Time

Table 9. HART-IN Terminal Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance	HART signal ac-coupled into terminal		35		kΩ
Output current (peak-to-peak)	Input signal of 500 mV (peak-to-peak)	0.9	1	1.1	mA

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7.3.16.2 Implementing HART in All Current Output Modes

The use of the HART-IN terminal to implement HART modulation is limited to the case where the RANGE bits of the Control Register are set to the 4-mA to 20-mA range. If it is desirable to implement HART irrespective of the RANGE bit settings, the following subsections describe the two possible methods.

7.3.16.2.1 Using CAP2 Terminal

The first method of implementing HART is to couple the signal through the CAP2 terminal, as illustrated in Figure 59.

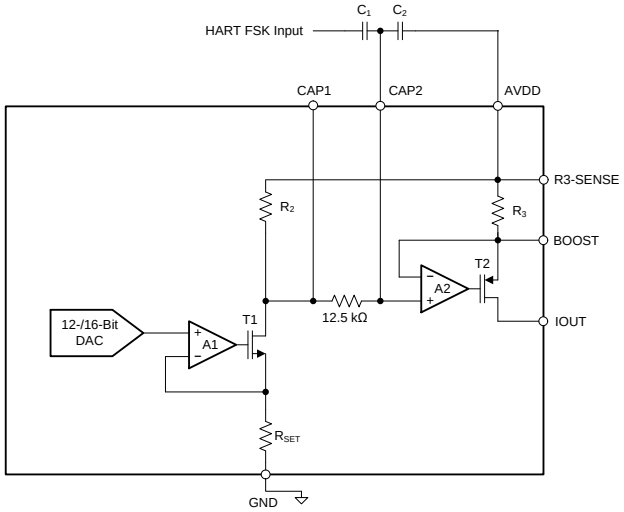

Figure 59. Implementing HART on IOUT Using the CAP2 Terminal

In Figure 59, R_3 is nominally 40 Ω, and R_2 is dependent on the current output range (set by the RANGE bits), described as follows:

- 4-mA to 20-mA range: R_2 = 2.4 kΩ typical
- 0-mA to 20-mA range: R_2 = 3 kΩ typical
- 0-mA to 24-mA range: R_2 = 3.6 kΩ typical

The purpose of the 12.5-kΩ resistor is to create a filter when CAP1 and CAP2 are used.

To insert the external HART signal on the CAP2 terminal, an external ac-coupling capacitor is typically connected to CAP2. The high pass filter 3-dB frequency is determined by the resistive impedance looking into CAP2 (R_2 + 12.5 kΩ) and the coupling-capacitor value. The 3-dB frequency is 1 / (2 × π × [R_2 + 12.5 kΩ] × [Coupling Capacitor Value]).

When the input HART frequency is greater than the 3-dB frequency, the ac signal is seen at the plus input of amplifier A2 and is therefore seen across the 40-Ω resistor. To generate a 1-mA signal on the output therefore requires a 40-mV peak-to-peak signal on CAP2. Because most HART modems do not output a 40-mV signal, a capacitive divider is used in Figure 59 to attenuate the FSK signal from the modem. In Figure 59, the high-pass cutoff frequency is 1 / (2 × π × [R_2+ 12.5 kΩ] × [C_1 + C_2]). There is one disadvantage to this approach: if the AVDD supply is not clean, any ripple on it could couple into the part.

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7.3.16.2.2 Using the ISET-R Terminal

The second method to implement HART is to couple the HART signal through the ISET-R terminal when IOUT is operated using an external R_{SET} resistor. The FSK signal from the modem is ac-coupled into the terminal through a series combination of Rin and Cin as shown in Figure 60

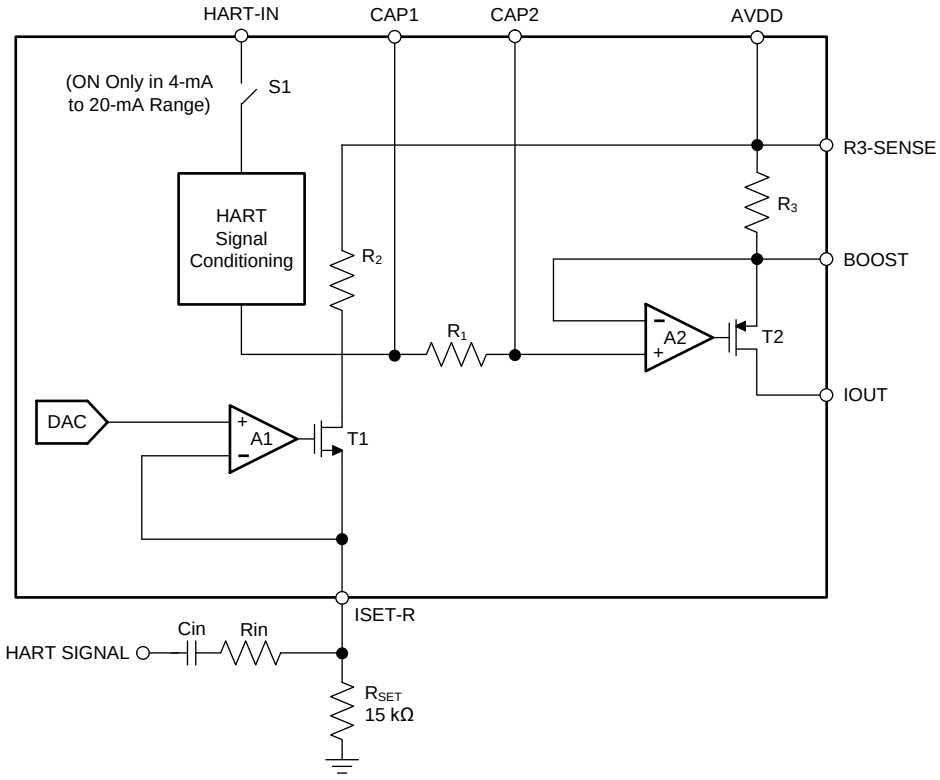

Figure 60. Implementing HART with the ISET-R Terminal

The magnitude of the ac-current output is calculated as:

$$(V_{HART} \times k) / Rin \quad (6)$$

where

- V_{HART} is the amplitude of the HART FSK signal from the modem
- k is a constant that represents the gain transfer function from the ISET-R terminal to the IOUT terminal and depends on the selected current output range as follows:
  - k = 60 for the 4-mA to 20-mA range
  - k = 75 for the 0-mA to 20-mA range
  - k = 90 for the 0-mA to 24-mA range

The series input resistor and capacitor form a high-pass filter at the ISET-R terminal. Select Cin to make sure that all signals in the HART extended-frequency band pass through unattenuated.

7.4 Device Functional Modes

7.4.1 Setting Current-Output Ranges

The current output range is set according to Table 10.

Table 10. RANGE Bits vs Output Range

RANGE	OUTPUT RANGE
101	4 mA to 20 mA
110	0 mA to 20 mA
111	0 mA to 24 mA

Note that changing the RANGE bits at any time causes the DAC data register to be cleared.

7.4.2 Current-Setting Resistor

Resistor R_{SET} (used to convert the DAC voltage to current) shown in Figure 53 determines the stability of the output current over temperature. If desired, an external, low-drift, precision 15-kΩ resistor can be connected to the ISET-R terminal and used instead of the internal R_{SET} resistor.

7.4.3 BOOST Configuration for IOUT

Figure 61 shows an external NPN transistor used to reduce power dissipation on the die. Most of the load current flows through the NPN transistor with a small amount flowing through the on-chip PMOS transistor based on the gain of the NPN transistor. This configuration reduces the temperature induced drift on the die and internal reference and is an option for use cases at the extreme end of the supply, load current, and ambient temperature ranges.

The inclusion of the bipolar junction transistor (BJT) adds an additional open loop gain to internal amplifier A2 (see Figure 53) and thus, can cause possible instability. Adding series emitter resistor R2 decreases the gain of the stage created by the BJT and internal R3 resistor (see Figure 53) especially for cases where R_{LOAD} is a short or a very small load, such as a multimeter. Recommended values for R_1, R_2, and C_1 in this circuit are 1 kΩ, 30 Ω and 22 nF, respectively. An equivalent solution is to place R_2 (with a recommended value of 3 kΩ instead of 30 Ω) in series with the base of the transistor instead of the configuration shown in Figure 61. Note that there is some gain error introduced by this configuration, as seen in Figure 15, Figure 16 and Figure 17. Use the internal transistor in most cases because the values in the Electrical Characteristics section are based on the configuration with the internal on-chip PMOS transistor.

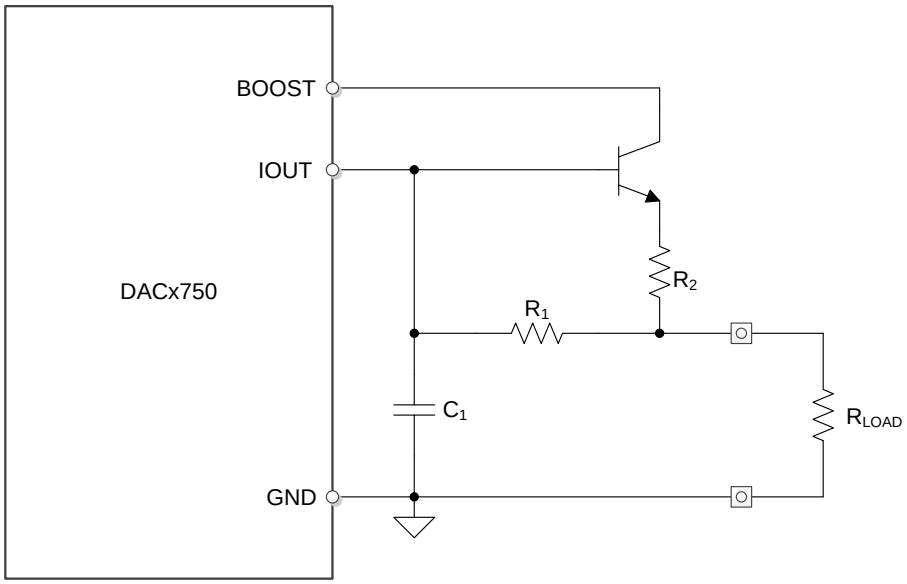

Figure 61. Boost Mode Configuration

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7.5 Programming

Table 11 shows the available commands and registers on the DACx750 devices. *No operation*, *read operation*, and *watchdog timer* refer to commands and are not explicit registers. For more information on these commands, see the *Read Operation* and *Watchdog Timer* sections.

7.6 Register Map

Table 11 shows the available registers on the DACx750 devices. See the *DACx750 Register Descriptions* section for descriptions of all DACx750 registers.

Table 11. Command and Register Map

REGISTER OR COMMAND	READ AND WRITE ACCESS	DATA BITS (DB15:DB0)													
		15:14	13	12	11	10:9	8	7	6	5	4	3	2	1	0
Control	RW	X	REXT	OUTEN	SRCLK			SRSTEP			SREN	DCEN	RANGE		
Configuration	RW	X(1)								CALEN	HARTEN	CRCEN	WDEN	WDPD	
DAC Data(2)	RW	D15:D0													
No operation(3)	—	X													
Read Operation(3)	—	X								READ ADDRESS					
Reset	W														RESET
Status	R	Reserved									CRC-FLT	WD-FLT	I-FLT	SR-ON	T-FLT
DAC Gain Calibration(2)	RW	G15:G0, unsigned													
DAC Zero Calibration(2)	RW	Z15:Z0, signed													
Watchdog Timer(3)	—	X													

(1) X denotes *don't care* bits.
(2) DAC8750 (16-bit version) shown. DAC7750 (12-bit version) contents are located in DB15:DB4. For DAC7750, DB3:DB0 are *don't care* bits when writing and zeros when reading.
(3) *No operation*, *read operation*, and *watchdog timer* are commands and not registers.

7.6.1 DACx750 Register Descriptions

7.6.1.1 Control Register

The DACx750 control register is written to at address 0x55. Table 12 shows the description for the control register bits.

Table 12. Control Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB14	Reserved	00	Reserved. Do not write any value other than zero to these bits.
DB13	REXT	0	External current setting resistor enable.
DB12	OUTEN	0	Output enable. Bit = 1: Output is determined by RANGE bits. Bit = 0: Output is disabled. IOUT is Hi-Z.
DB11:DB8	SRCLK[3:0]	0000	Slew rate clock control. Ignored when bit SREN = 0.
DB7:DB5	SRSTEP[2:0]	000	Slew rate step size control. Ignored when bit SREN = 0.
DB4	SREN	0	Slew Rate Enable. Bit = 1: Slew rate control is enabled, and the ramp speed of the output change is determined by SRCLK and SRSTEP. Bit = 0: Slew rate control is disabled. Bits SRCLK and SRSTEP are ignored. The output changes to the new level immediately.
DB3	DCEN	0	Daisy-chain enable.
DB2:DB0	RANGE[2:0]	000	Output range bits.

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7.6.1.2 Configuration Register

The DACx750 configuration register is written to at address 0x57. Table 13 summarizes the description for the configuration register bits.

Table 13. Configuration Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB6	Reserved	00 0000 0000	Reserved. Do not write any value other than zero to these bits.
DB5	CALEN	0	User calibration enable. When user calibration is enabled, the DAC data are adjusted according to the contents of the gain and zero calibration registers. See the *User Calibration* section.
DB4	HARTEN	0	Enable interface through HART-IN terminal (only valid for IOUT set to 4-mA to 20-mA range via RANGE bits). Bit = 1: HART signal is connected through internal resistor and modulates output current. Bit = 0: HART interface is disabled.
DB3	CRCEN	0	Enable frame error checking.
DB2	WDEN	0	Watchdog timer enable.
DB1:DB0	WDPD[1:0]	00	Watchdog timeout period.

7.6.1.3 DAC Registers

The DAC registers consist of a DAC data register (Table 14), a DAC gain calibration register (Table 15), and a DAC zero calibration register (Table 16). User calibration as described in the *User Calibration* section is a feature that allows for trimming the system gain and zero errors. Table 14 through Table 16 show the DAC8750, 16-bit version of these registers. The DAC7750 (12-bit version) register contents are located in DB15:DB4. For DAC7750, DB3:DB0 are *don't care* bits when writing and zeros when reading.

Table 14. DAC Data Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	D15:D0	0x0000	DAC data register. Format is unsigned straight binary.

Table 15. DAC Gain Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	G15:G0	0x0000	Gain calibration register for user calibration. Format is unsigned straight binary.

Table 16. DAC Zero Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	Z15:Z0	0x0000	Zero calibration register for user calibration. Format is twos complement.

7.6.1.4 Reset Register

The DACx750 reset register is written to at address 0x56. Table 17 provides the description.

Table 17. Reset Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB1	Reserved	000 0000 0000 0000	Reserved. Writing to these bits does not cause any change.
DB0	RESET	0	Software reset bit. Writing 1 to the bit performs a software reset that resets all registers and the ALARM status to the respective power-on reset default value. After reset completes, the RESET bit clears itself.

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7.6.1.5 Status Register

This read-only register consists of four $\overline{\text{ALARM}}$ status bits (CRC-FLT, WD-FLT, I-FLT, and T-FLT) and the SR-ON bit that shows the slew rate status, as shown in Table 18.

Table 18. Status Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB5	Reserved	000 0000 0000	Reserved. Reading these bits returns 0.
DB4	CRC-FLT	0	Bit = 1 indicates CRC error on SPI frame. Bit = 0 indicates normal operation.
DB3	WD-FLT	0	Bit = 1 indicates watchdog timer timeout. Bit = 0 indicates normal operation.
DB2	I-FLT	0	Bit = 1 indicates an open circuit or a compliance voltage violation in IOUT loading. Bit = 0 indicates IOUT load is at normal condition.
DB1	SR-ON	0	Bit = 1 when DAC code is slewing as determined by SRCLK and SRSTEP. Bit = 0 when DAC code is not slewing.
DB0	T-FLT	0	Bit = 1 indicates die temperature is over +142°C. Bit = 0 indicates die temperature is not over +142°C.

These devices continuously monitor the current output and die temperature. When an alarm occurs, the corresponding $\overline{\text{ALARM}}$ status bit is set (1). Whenever an $\overline{\text{ALARM}}$ status bit is set, it remains set until the event that caused it is resolved. The $\overline{\text{ALARM}}$ bit can only be cleared by performing a software reset, a power-on reset (by cycling power), or by having the error condition resolved. These bits are reasserted if the alarm condition continues to exist in the next monitoring cycle.

The $\overline{\text{ALARM}}$ bit goes to 0 when the error condition is resolved.

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8 Application and Implementation

8.1 Application Information

The DAC8750 and DAC7750 are 16-bit and 12-bit, respectively, digital-to-analog converters featuring current outputs commonly required for analog outputs in industrial-control applications such as programmable logic controllers (PLCs) and distributed control systems (DCSs), as well as field instruments such as pressure, temperature, level, and flow transmitters. The DACx750 family provides the high accuracy required for these applications, as well as high levels of integration and diagnostic features.

8.2 Typical Applications

8.2.1 Analog Output Module for PLC- and DCS-Based Industrial-Control Systems

Analog I/O modules in PLC- and DCS-based systems interface to sensors, actuators, and other field instruments. These modules must deliver high performance while also passing stringent EMI and EMC certification tests. Figure 62 shows a circuit example for an analog output module. A field supply terminal is shown instead of the more common use case of a backplane supply. The design uses two triple-channel isolators (ISO7631FC) to provide galvanic isolation for the digital lines to communicate to the main controller. The isolators can be driven by the internally-generated supply (DVDD) from the DACx750 to save components and cost. The DACx750 supplies up to 10 mA, which meets the supply requirements of the two isolators running at up to 10 Mbps. Additional cost savings are possible if noncritical signals such as CLR and $\overline{\text{ALARM}}$ are tied to GND or left unconnected.

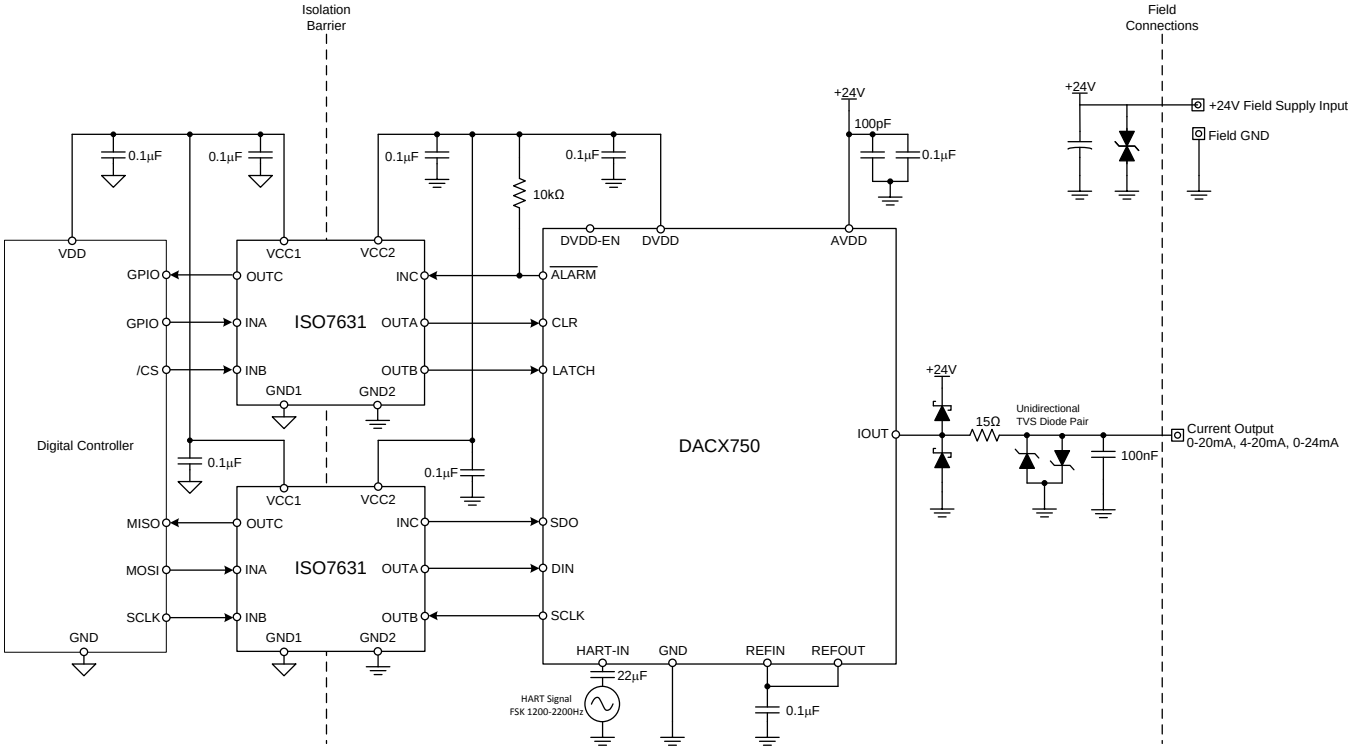

Figure 62. DACx750 in an Analog Output (AO) Module

The rest of this section presents a simplified discussion of the design process to pass the most common certification tests for analog output modules. For more information, please consult TI Precision Design TIPD153, *Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested*. Note that the same design can be modified and adapted to field instruments such as pressure and temperature transmitters.

Evaluation hardware and software are available for both the DAC8750 and DAC7750 that enable fast evaluation of all device parameters. Additionally, an EMC-enhanced edition of the EVM is available that demonstrates an example protection circuit based on the following design procedure.

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Typical Applications (continued)

8.2.1.1 Design Requirements

Table 19 lists the input, output, and EMI/EMC requirements for this example design.

Table 19. Design Parameters

DESIGN PARAMETER	VALUE
Power supply range	10 V to 36 V
Current output range	4 mA to 20 mA, 0 mA to 20 mA, 0 mA to 24 mA
IEC61000-4-2 (ESD)	±15 kV air discharge, ±8 kV coupling plane discharge
IEC61000-4-3 (RI)	20 V/m
IEC61000-4-4 (EFT)	±4 kV
IEC61000-4-5 (CI)	10 V/m

8.2.1.2 Detailed Design Procedure

The IEC61000-4 transients in the design requirements are high frequency and high energy signals. A protection scheme utilizes attenuation and diversion elements to capitalize on these properties to deliver robust immunity. The following sections detail the selection criteria for each component shown in Figure 62.

8.2.1.2.1 TVS Diodes

A TVS diode can be used to divert high-voltage transients to ground. Base diode selection primarily on working voltage, breakdown voltage, power rating, and leakage current. Working voltage specifies the largest reverse voltage that the TVS diode is meant to be exposed to continuously without conducting. As the voltage increases above the working voltage, more current begins to flow through the diode. The breakdown voltage defines the reverse voltage at which the diode allows full current flow.

Make sure that the working voltage is high enough to have minimal impact on the performance of the circuit during normal operation. Make sure that the breakdown voltage is low enough to protect all components connected to the output node. When the diode is not operating in the breakdown region, some current still flows through the diode and can impact system accuracy. Select a diode with minimal leakage current.

8.2.1.2.2 Schottky Diodes

All Schottky diodes feature low forward-voltage drop for reasonable current, but the forward voltage drop may increase beyond the point of being useful for a clamp to rail when exposed to excessive current. The diodes used in this design must maintain low forward-voltage drop to keep the voltage at the output terminals within the absolute maximum supply voltages of the device during exposure to high-energy transients.

Take into consideration the clamp-to-rail diodes reverse leakage current parameter. Reverse leakage current is the amount of current that flows in the reverse path of the diode when exposed to a specific reverse bias voltage. Select a diode with minimal reverse leakage current.

8.2.1.2.3 Other Passive Elements

The capacitor at the output terminal is used in combination with the transient generator source impedance to attenuate and slow down signals before they are clamped by the TVS diodes or Schottky diodes.

A resistor is placed between the TVS diodes and Schottky diodes to provide a pass element that limits current in order to increase the effectiveness of the Schottky diodes. Size this resistor appropriately to provide some series current limit without causing substantial compliance voltage limitations for the current output.

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8.2.1.3 Application Performance Plots

The protection circuit has minimal impact on the DACx750 output, as shown in Figure 63. All analog output specifications remain within the bounds defined by the DACx750 Electrical Characteristics.

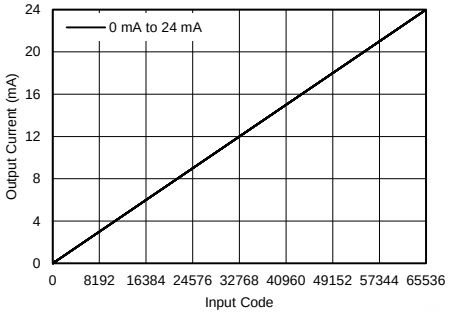

Figure 63. Measured Current Output

9 Power-Supply Recommendations

The DACx750 devices are designed to operate with a unipolar analog supply ranging from 10 V to 36 V. Take care when choosing the supply voltage to make sure that loop compliance requirements for the current output are met based on the maximum current output and the maximum load impedance.

The DACx750 devices also require a digital supply with a range from 2.7 V to 5.5 V. If an external digital supply is not available, the DACx750 features an internal LDO that can generate a 4.6-V supply. The internal LDO is enabled or disabled by connecting the DVDD-EN terminal to ground, or by leaving it unconnected.

9.1 Thermal Considerations

The DACx750 is designed for a maximum junction temperature of +150°C. In cases where the maximum AVDD is driving maximum current into ground, this junction temperature can be exceeded. Use the following equation to determine the maximum junction temperature that can be reached:

$$\text{Power Dissipation} = (T_J \text{ max} - T_A) / \theta_{JA} \quad (7)$$

where

- T_J max = +150°C
- T_A is the ambient temperature
- θ_{JA} is the package-dependent, junction-to-ambient thermal resistance, found in the *Thermal Information* table.

The power dissipation is calculated by multiplying all the supply voltages with the currents supplied, which are found in the *Power Requirements* subsection of the Electrical Characteristics.

Consider an example: IOUT is enabled, supplying 24 mA into GND with a 25°C ambient temperature, AVDD of 24 V, and DVDD is generated internally. From the Electrical Characteristics, the max value of AIDD = 3 mA when IOUT is enabled and DAC code = 0x0000. Also, the max value of DIDD = 1 mA. Accordingly, the worst-case power dissipation is 24 V × (24 mA + 3 mA + 1 mA) = 672 mW. Using the θ_{JA} value for the TSSOP package, we get T_J max = +25°C + (32.3 × 0.672)°C = +46.7°C. At +85°C ambient temperature, the corresponding value of T_J max is +106.7°C. Using this type of analysis, the system designer can both specify and design for the equipment operating conditions. Note that for enhanced thermal performance, connect the thermal pad in both packages to a copper plane.

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10 Layout

10.1 Layout Guidelines

To maximize the performance of the DACx750 in any application, good layout practices and proper circuit design must be followed. A few recommendations specific to the DACx750 are:

1. As is seen in Figure 59, CAP2 is directly connected to the input of the final IOUT amplifier. Any noise or unwanted ac signal routed near the CAP1 and CAP2 terminals could capacitively couple onto internal nodes and affect IOUT. Therefore, it is important to avoid routing any digital or HART signal traces over the CAP1 and CAP2 traces.
2. Connect the thermal PAD to the lowest potential in the system.
3. Make sure that AVDD has decoupling capacitors local to the respective terminals.
4. Place the reference capacitor close to the reference input terminal.
5. Avoid routing switching signals near the reference input.
6. For designs that include protection circuits:
   (a) Place diversion elements, such as TVS diodes or capacitors, close to off-board connectors to make sure that return current from high-energy transients does not cause damage to sensitive devices.
   (b) Use large, wide traces to provide a low-impedance path to divert high-energy transients away from I/O terminals.

10.2 Layout Example

Figure 64 shows an example layout for the DAC8760 and DAC7760 devices from TIPD153. A similar layout can be used for the DACx750 with a few modifications to account for pinout differences.

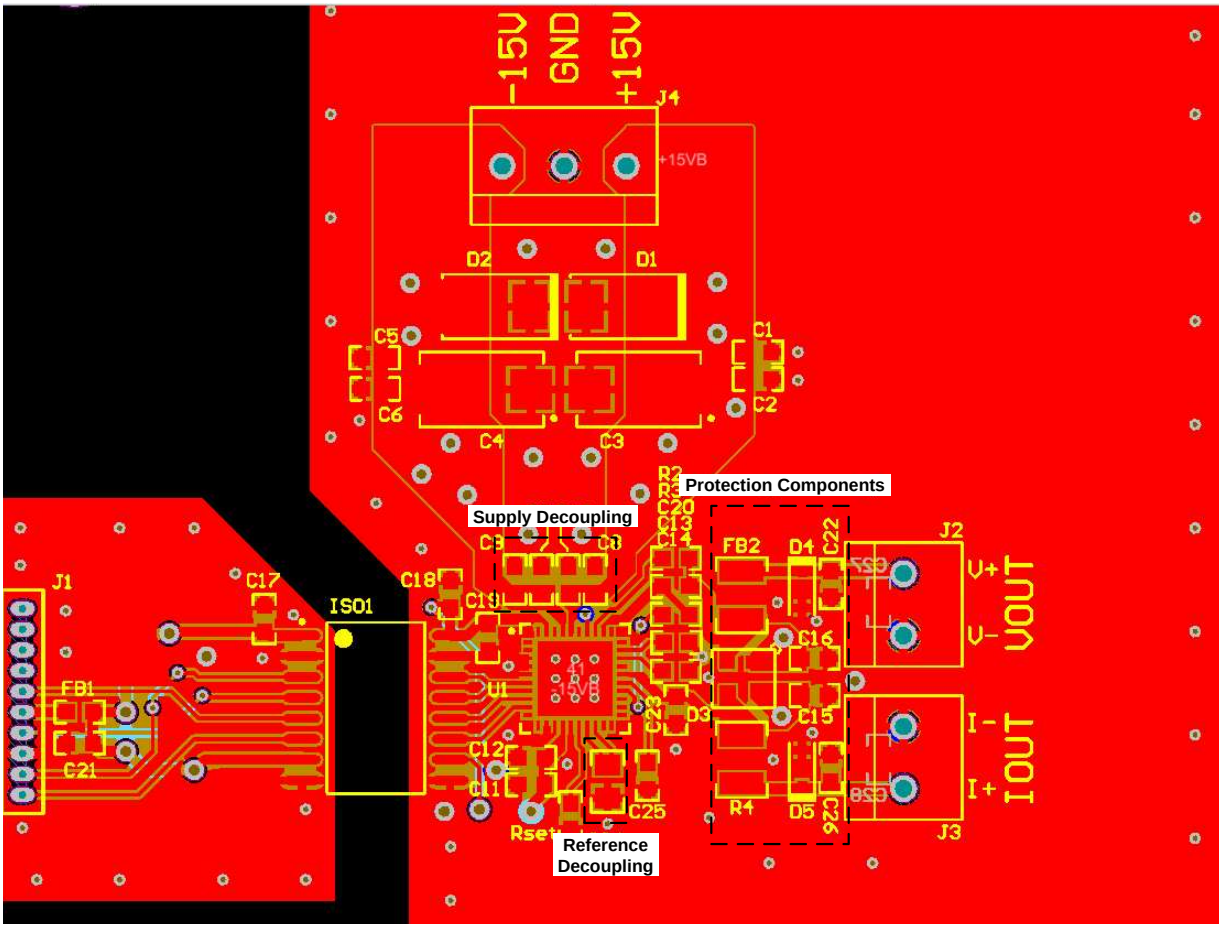

Figure 64. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

TI Precision Design TIPD153, *Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested*.

Application Report SLAA572, *Implementing HART Communication with the DAC8760 Family.*

11.2 Related Links

Table 20 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 20. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC7750	Click here	Click here	Click here	Click here	Click here
DAC8750	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

HART is a registered trademark of HART Communication Foundation.
SPI, QSPI are trademarks of Motorola, Inc.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7750IPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750	Samples
DAC7750IPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750	Samples
DAC7750IRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC7750	Samples
DAC7750IRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC7750	Samples
DAC8750IPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750	Samples
DAC8750IPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750	Samples
DAC8750IRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC8750	Samples
DAC8750IRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC8750	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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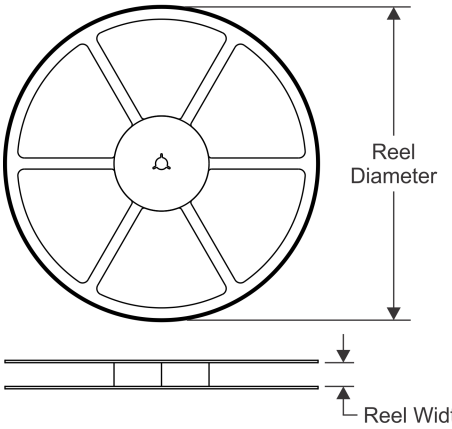
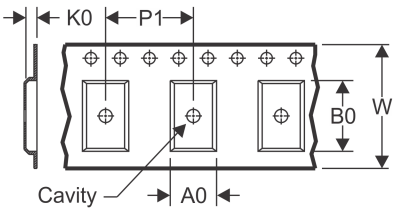
TAPE AND REEL INFORMATION

REEL DIMENSIONS

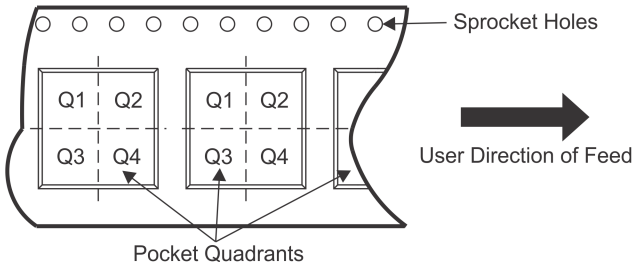


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

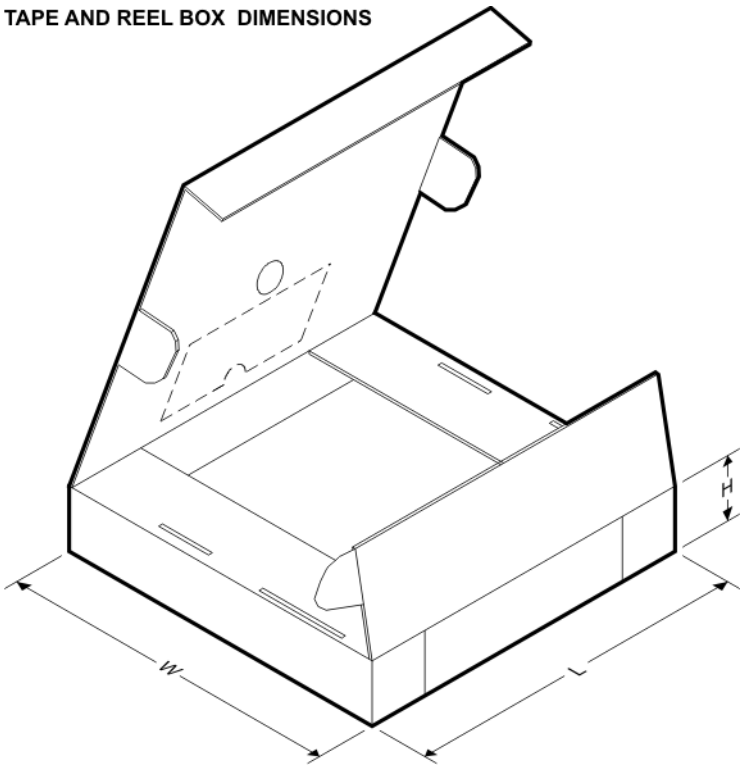
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7750IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC7750IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC7750IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8750IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC8750IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8750IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

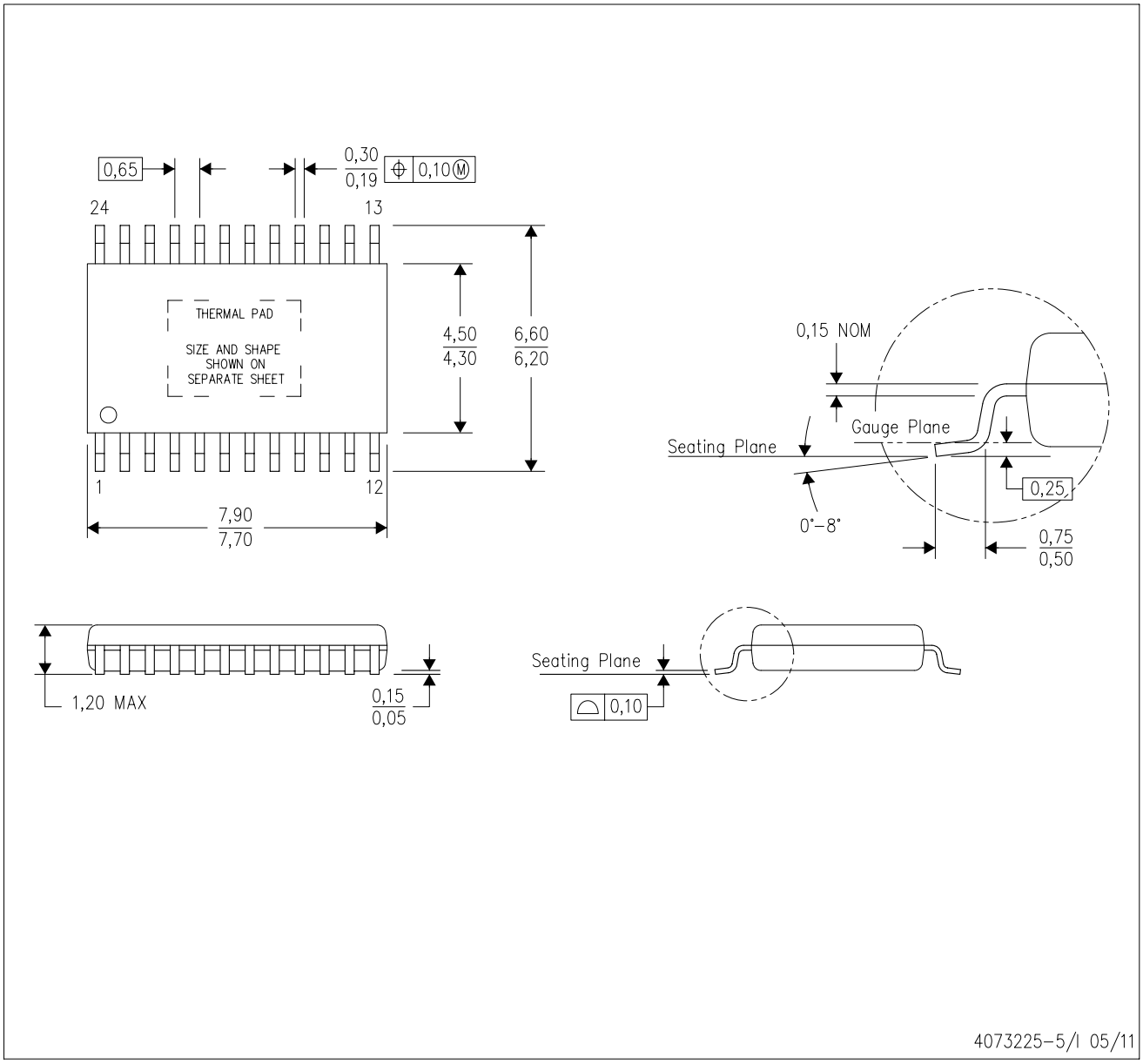
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7750IPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
DAC7750IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC7750IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
DAC8750IPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
DAC8750IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC8750IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

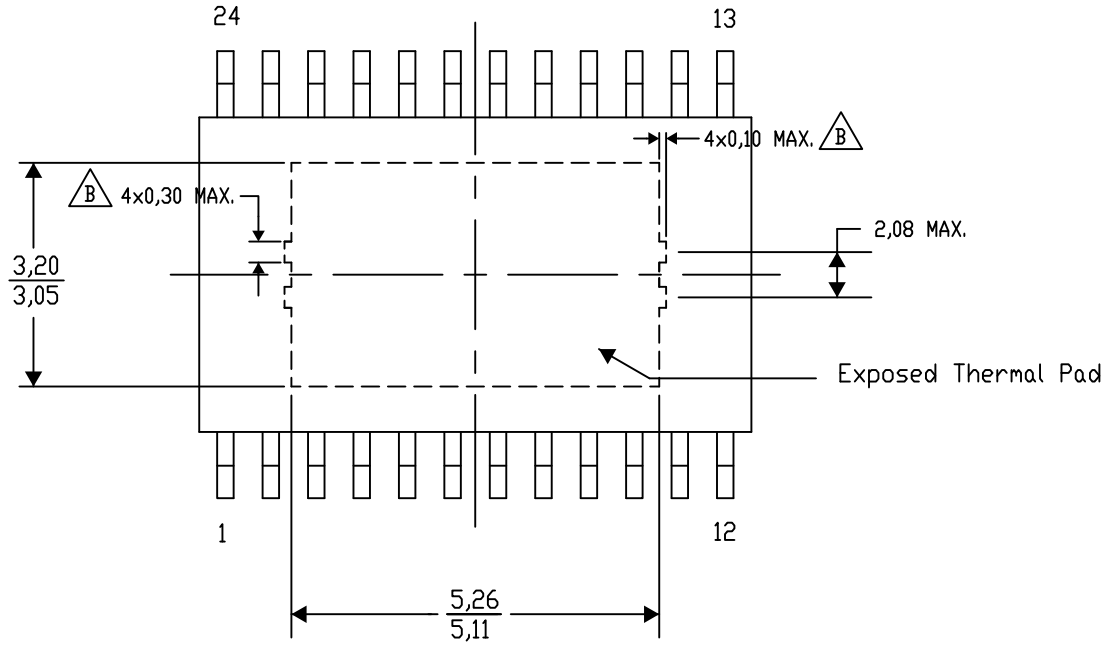
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

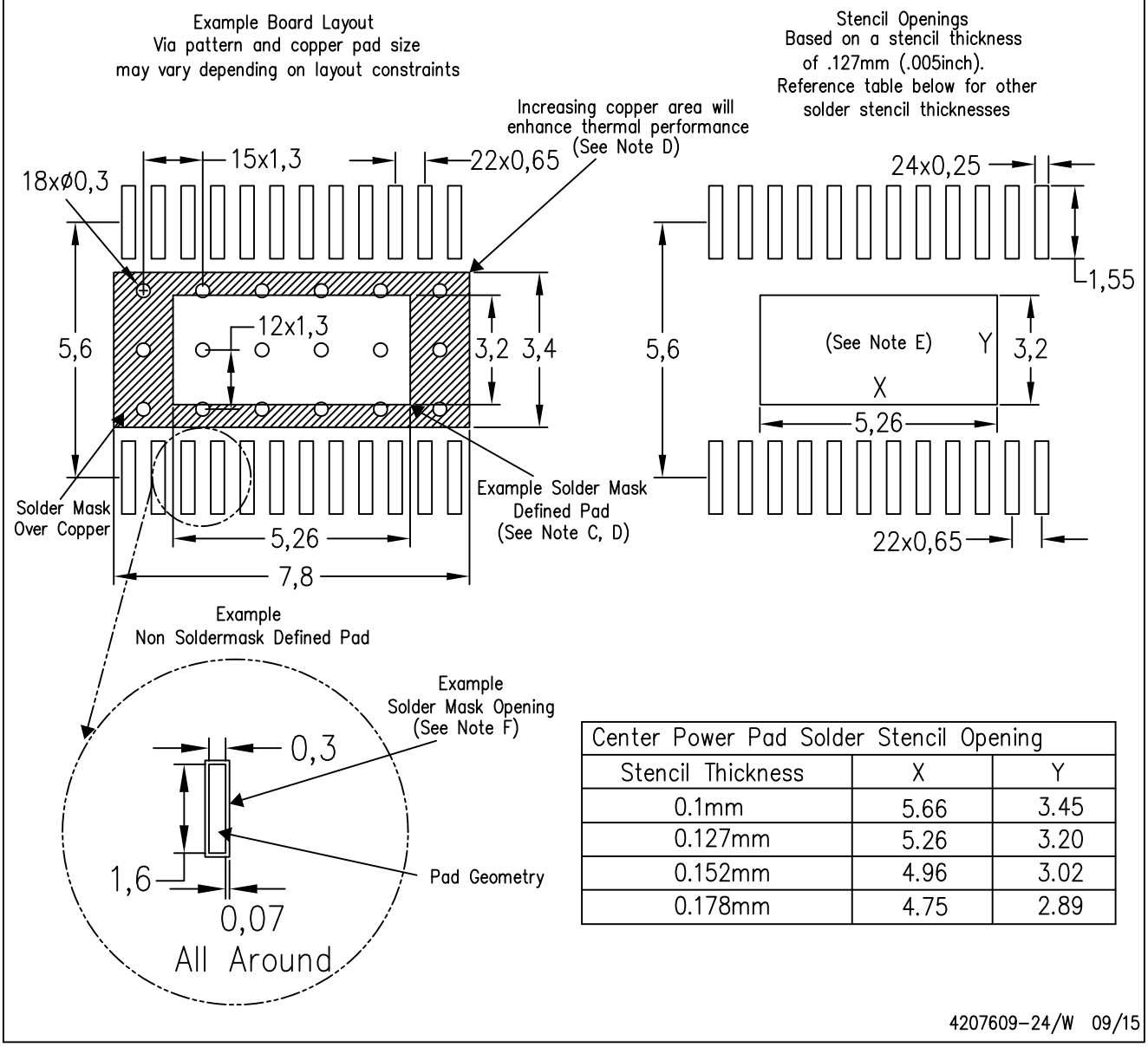
4206332–46/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE

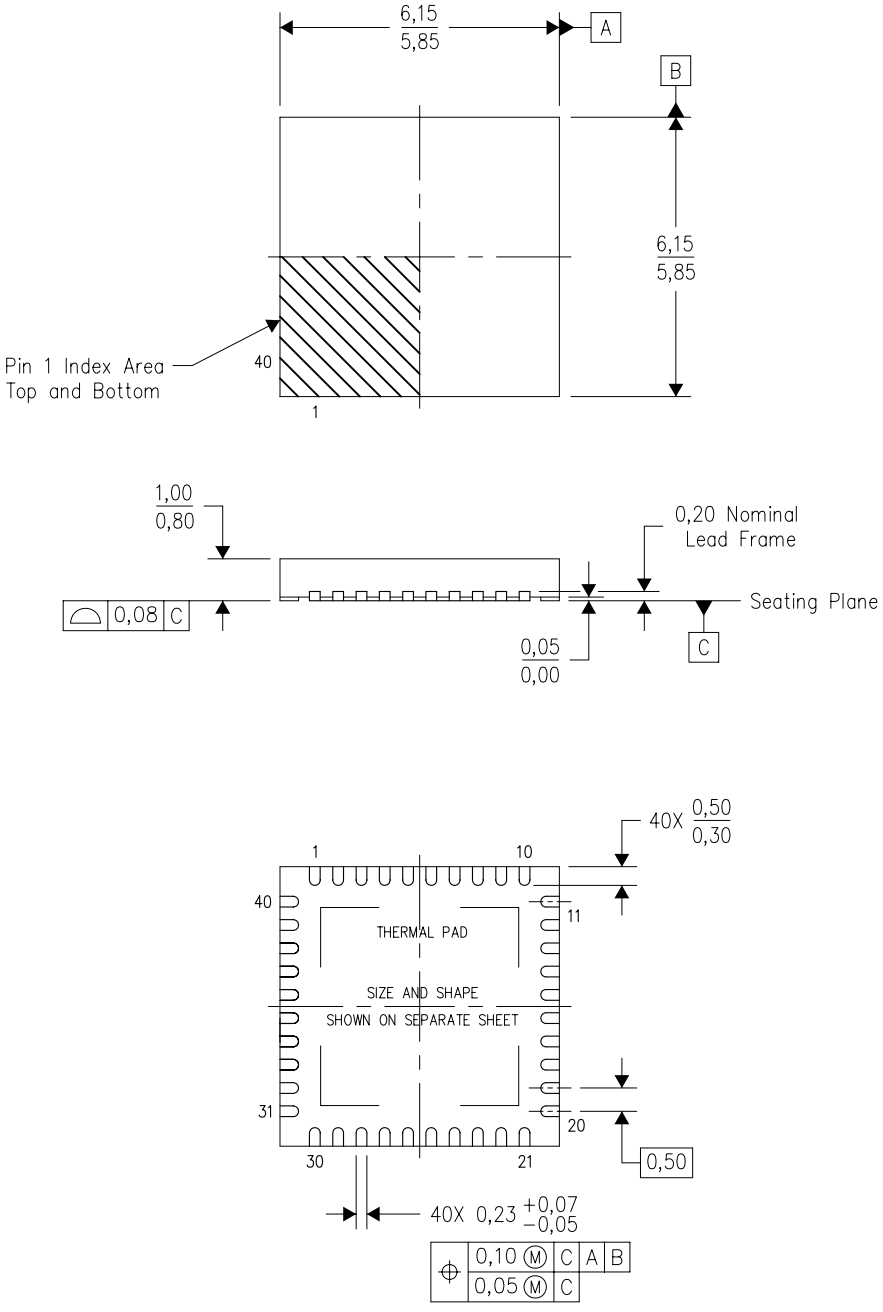


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.66	3.45
0.127mm	5.26	3.20
0.152mm	4.96	3.02
0.178mm	4.75	2.89

4207609–24/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

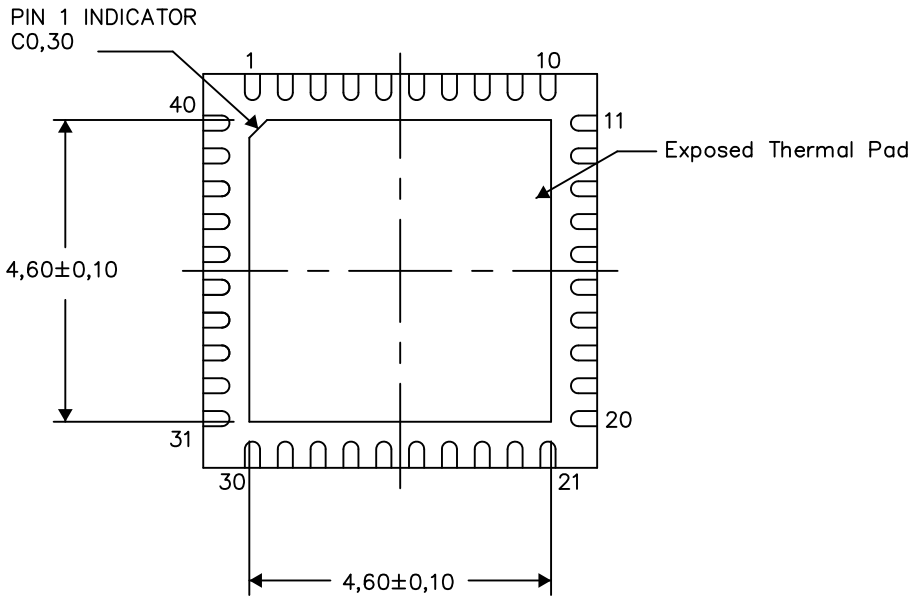
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



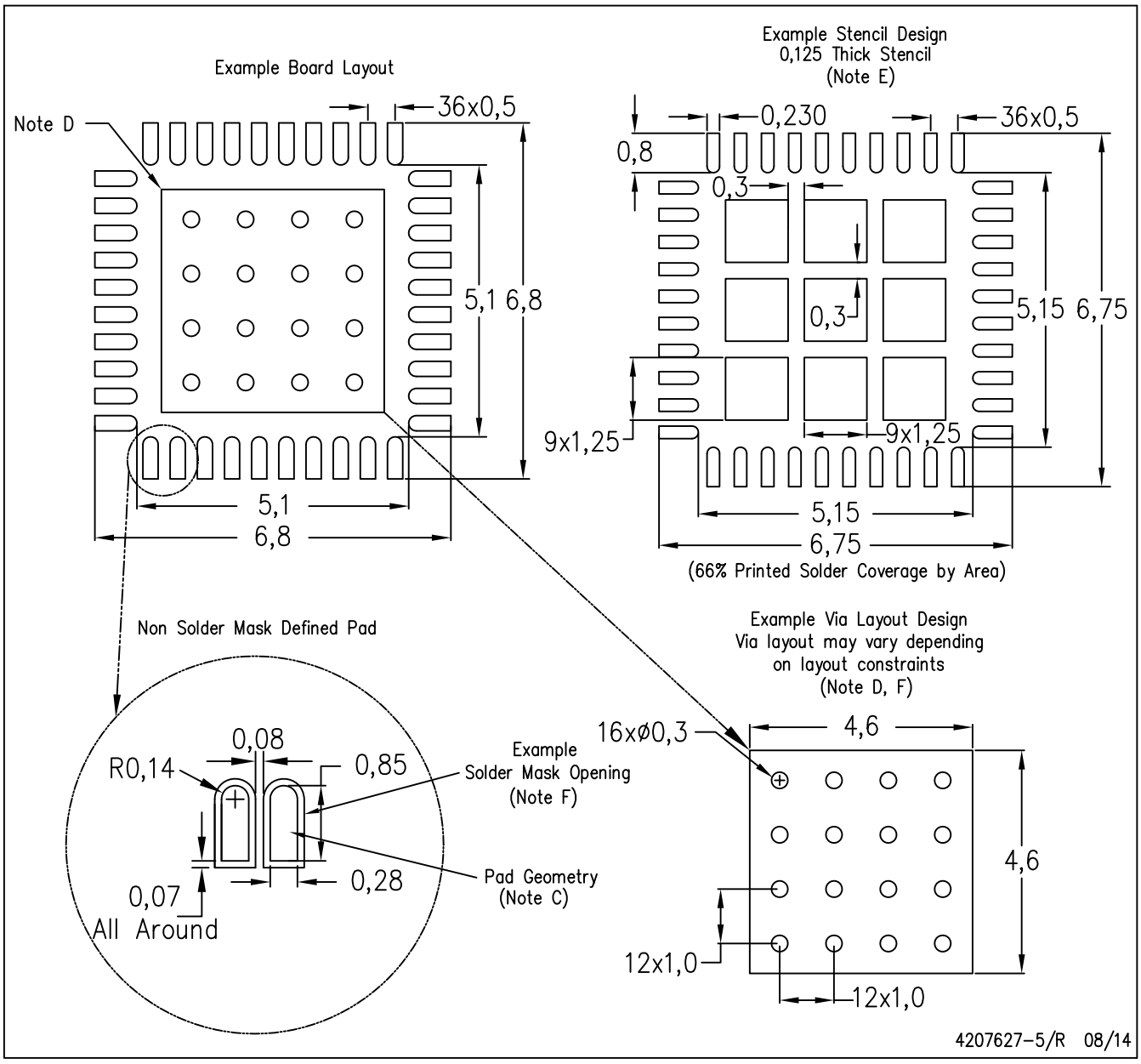
Bottom View

Exposed Thermal Pad Dimensions

4206355–5/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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