

DAC7611

## 12-Bit Serial Input DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- **LOW POWER:** 2.5mW
- **FAST SETTLING:** 7 $\mu$ s to 1 LSB
- **1mV LSB WITH 4.095V FULL-SCALE RANGE**
- **COMPLETE WITH REFERENCE**
- **12-BIT LINEARITY AND MONOTONICITY OVER INDUSTRIAL TEMP RANGE**
- **ASYNCHRONOUS RESET TO 0V**
- **3-WIRE INTERFACE:** Up to 20MHz Clock
- **ALTERNATE SOURCE TO DAC8512**

### APPLICATIONS

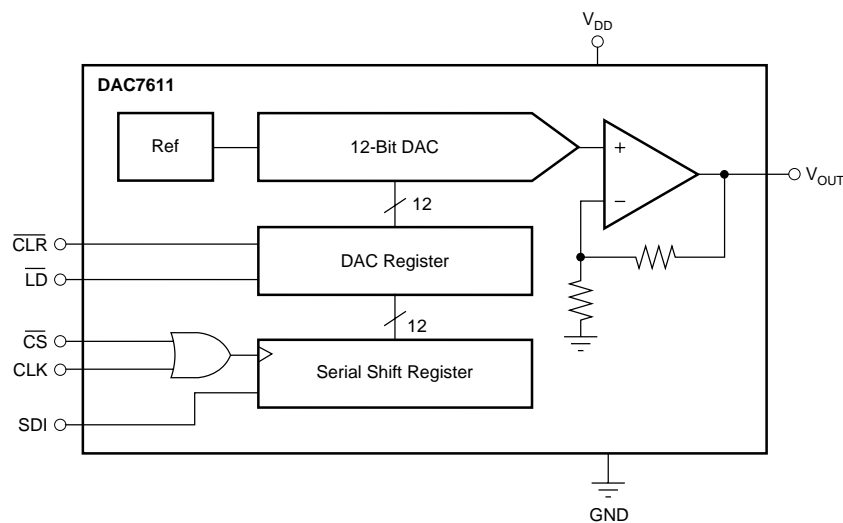
- **PROCESS CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **CLOSED-LOOP SERVO-CONTROL**
- **PC PERIPHERALS**
- **PORTABLE INSTRUMENTATION**

### DESCRIPTION

The DAC7611 is a 12-bit digital-to-analog converter (DAC) with guaranteed 12-bit monotonicity performance over the industrial temperature range. It requires a single +5V supply and contains an input shift register, latch, 2.435V reference, DAC, and high speed rail-to-rail output amplifier. For a full-scale step, the output will settle to 1 LSB within 7 $\mu$ s. The device consumes 2.5mW (0.5mA at 5V).

The synchronous serial interface is compatible with a wide variety of DSPs and microcontrollers. Clock (CLK), serial data in (SDI), and load strobe ( $\overline{LD}$ ) comprise the serial interface. In addition, two control pins provide a chip select (CS) function and an asynchronous clear (CLR) input. The CLR input can be used to ensure that the DAC7611 output is 0V on power-up or as required by the application.

The DAC7611 is available in an 8-lead SOIC or 8-pin plastic DIP package and is fully specified over the industrial temperature range of -40°C to +85°C.



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# SPECIFICATIONS

## ELECTRICAL

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , and  $V_{DD} = +5\text{V}$ , unless otherwise noted.

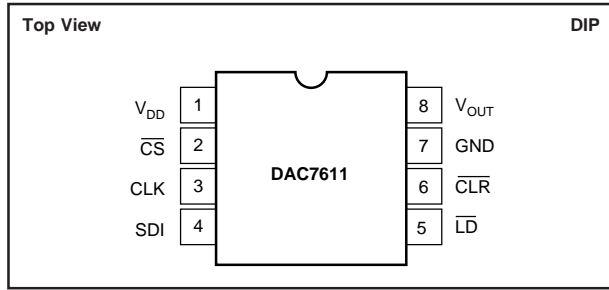
| PARAMETER                              | CONDITIONS  | DAC7611P, U |                 |          | DAC7611PB, UB |           |       | UNITS            |
|--|---|-------------|-----------------|----------|---------------|-----------|-------|------------------|
|  |   | MIN         | TYP             | MAX      | MIN           | TYP       | MAX   |                  |
| <b>ACCURACY</b>                        |   |             |                 |          |               |           |       |                  |
| Resolution                             |   | 12          |                 |          | *             |           |       | Bits             |
| Relative Accuracy <sup>(1)</sup>       |   | -2          | $\pm 1/2$       | +2       | -1            | $\pm 1/4$ | +1    | LSB              |
| Differential Nonlinearity              | Guaranteed Monotonic  | -1          | $\pm 1/2$       | +1       | -1            | $\pm 1/4$ | +1    | LSB              |
| Zero-Scale Error                       | Code 000 <sub>H</sub>   | -1          | +1              | +3       | *             | *         | *     | LSB              |
| Full Scale Voltage                     | Code FFF <sub>H</sub>   | 4.079       | 4.095           | 4.111    | 4.087         | 4.095     | 4.103 | V                |
| <b>ANALOG OUTPUT</b>                   |   |             |                 |          |               |           |       |                  |
| Output Current                         | Code 800 <sub>H</sub>   | $\pm 5$     | $\pm 7$         |          | *             | *         | *     | mA               |
| Load Regulation                        | $R_{LOAD} \geq 402\Omega$ , Code 800 <sub>H</sub>                               |             | 1               | 3        |               | *         | *     | LSB              |
| Capacitive Load                        | No Oscillation  |             | 500             |          |               | *         | *     | pF               |
| Short Circuit Current                  |   |             | $\pm 70$        |          |               | *         | *     | mA               |
| Short Circuit Duration                 | GND or $V_{DD}$   |             | Indefinite      |          |               | *         | *     |                  |
| <b>DIGITAL INPUT</b>                   |   |             |                 |          |               |           |       |                  |
| Data Format                            |   |             | Serial          |          |               | *         | *     |                  |
| Data Coding                            |   |             | Straight Binary |          |               | *         | *     |                  |
| Logic Family                           |   |             | TTL             |          |               | *         | *     |                  |
| Logic Levels                           |   |             |                 |          |               |           |       |                  |
| $V_{IH}$                               |   | 2.4         |                 |          | *             |           |       | V                |
| $V_{IL}$                               |   |             |                 | 0.8      |               | *         | *     | V                |
| $I_{IH}$                               |   |             |                 | $\pm 10$ |               | *         | *     | $\mu\text{A}$    |
| $I_{IL}$                               |   |             |                 | $\pm 10$ |               | *         | *     | $\mu\text{A}$    |
| <b>DYNAMIC PERFORMANCE</b>             |   |             |                 |          |               |           |       |                  |
| Settling Time <sup>(2)</sup> ( $t_s$ ) | To $\pm 1$ LSB of Final Value   |             | 7               |          |               | *         | *     | $\mu\text{s}$    |
| DAC Glitch                             |   |             | 15              |          |               | *         | *     | nV-s             |
| Digital Feedthrough                    |   |             | 2               |          |               | *         | *     | nV-s             |
| <b>POWER SUPPLY</b>                    |   |             |                 |          |               |           |       |                  |
| $V_{DD}$                               |   | +4.75       | +5.0            | +5.25    | *             | *         | *     | V                |
| $I_{DD}$                               | $V_{IH} = 5\text{V}$ , $V_{IL} = 0\text{V}$ , No Load, at Code 000 <sub>H</sub> |             | 0.5             | 1        |               | *         | *     | mA               |
| Power Dissipation                      | $V_{IH} = 5\text{V}$ , $V_{IL} = 0\text{V}$ , No Load                           |             | 2.5             | 5        |               | *         | *     | mW               |
| Power Supply Sensitivity               | $\Delta V_{DD} = \pm 5\%$   |             | 0.001           | 0.004    |               | *         | *     | %/%              |
| <b>TEMPERATURE RANGE</b>               |   |             |                 |          |               |           |       |                  |
| Specified Performance                  |   | -40         |                 | +85      | *             |           | *     | $^\circ\text{C}$ |

\* Same specification as for DAC7611P, U.

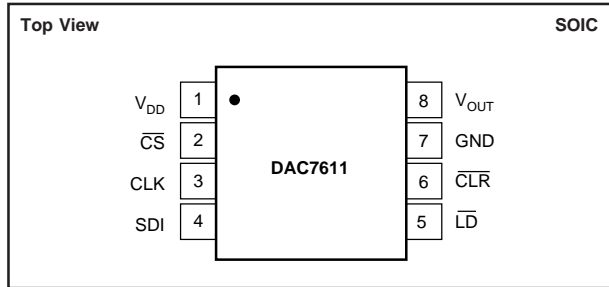
NOTES: (1) This term is sometimes referred to as Linearity Error or Integral Nonlinearity (INL). (2) Specification does not apply to negative-going transitions where the final output voltage will be within 3 LSBs of ground. In this region, settling time may be double the value indicated.

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## PIN CONFIGURATION



## PIN CONFIGURATION



## PIN DESCRIPTION

| PIN | LABEL            | DESCRIPTION   |
|-----|------------------|---|
| 1   | $V_{DD}$         | Power Supply  |
| 2   | $\overline{CS}$  | Chip Select (active LOW).   |
| 3   | CLK              | Synchronous Clock for the Serial Data Input.  |
| 4   | SDI              | Serial Data Input. Data is clocked into the internal serial register on the rising edge of CLK.   |
| 5   | $\overline{LD}$  | Loads the Internal DAC Register. NOTE: The DAC register is a transparent latch and is transparent when $\overline{LD}$ is LOW (regardless of the state of $\overline{CS}$ or CLK).  |
| 6   | $\overline{CLR}$ | Asynchronous Input to Clear the DAC Register. When $\overline{CLR}$ is strobed LOW, the DAC register is set to 000 <sub>H</sub> and the output voltage to 0V.   |
| 7   | GND              | Ground  |
| 8   | $V_{OUT}$        | Voltage Output. Fixed output voltage range of approximately 0V to 4.095V (1mV/LSB). The internal reference maintains this output range over time, temperature, and power supply variations (within the values defined in the specifications section). |



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|   |                          |
|---|--------------------------|
| $V_{DD}$ to GND .....                   | -0.3V to 6V              |
| Digital Inputs to GND .....             | -0.3V to $V_{DD} + 0.3V$ |
| $V_{OUT}$ to GND .....                  | -0.3V to $V_{DD} + 0.3V$ |
| Power Dissipation .....                 | 325mW                    |
| Thermal Resistance, $\theta_{JA}$ ..... | 150°C/W                  |
| Maximum Junction Temperature .....      | +150°C                   |
| Operating Temperature Range .....       | -40°C to +85°C           |
| Storage Temperature Range .....         | -65°C to +150°C          |
| Lead Temperature (soldering, 10s) ..... | +300°C                   |

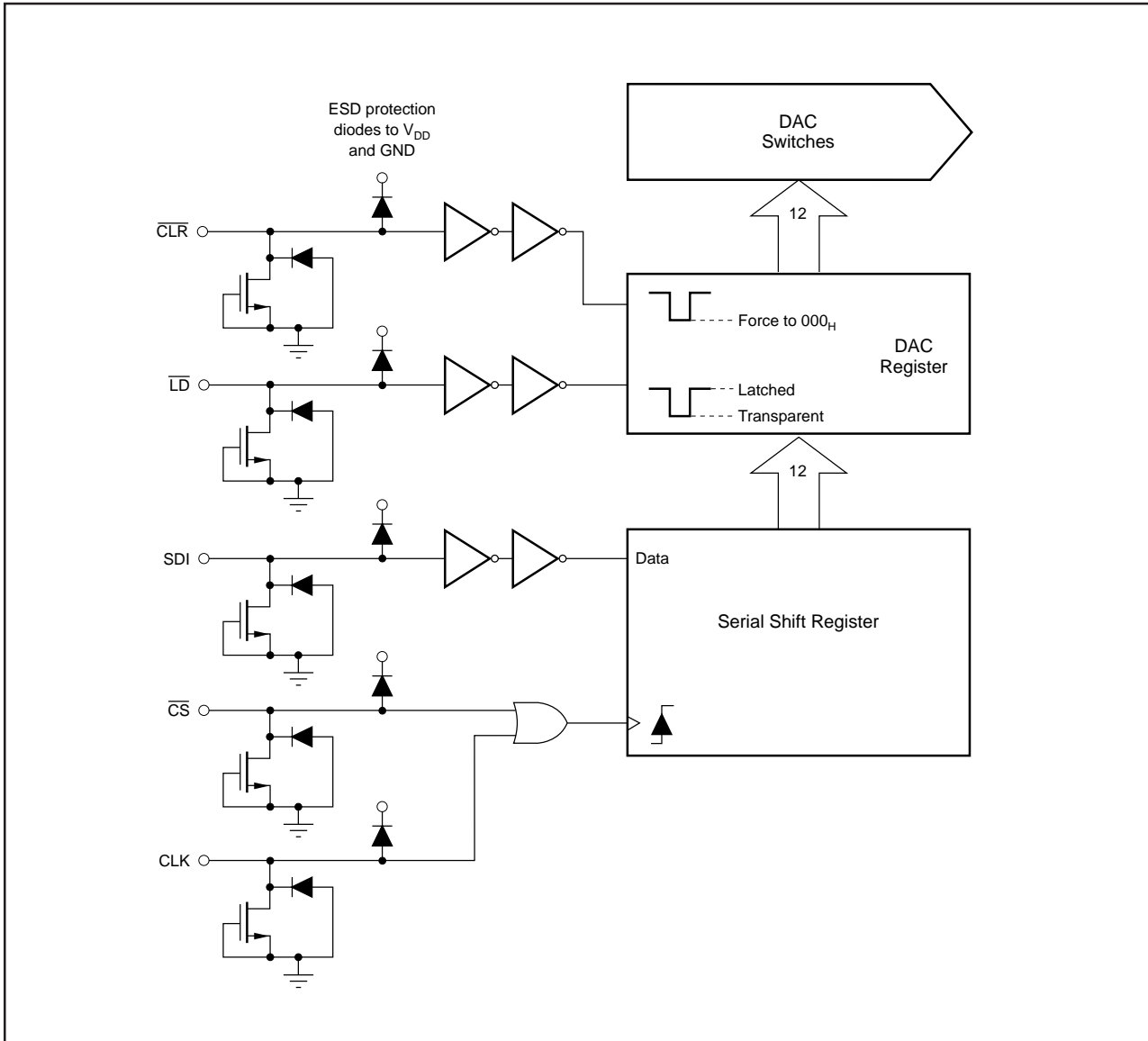
NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PACKAGE/ORDERING INFORMATION

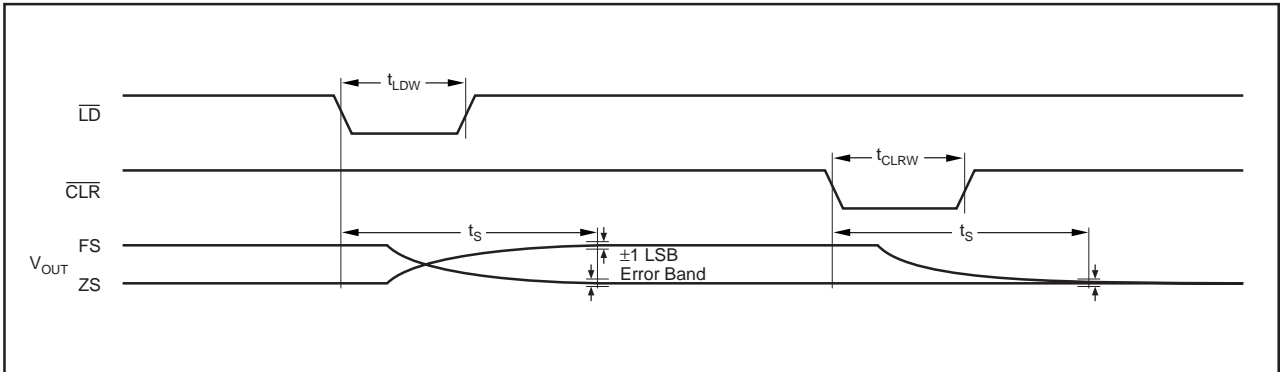
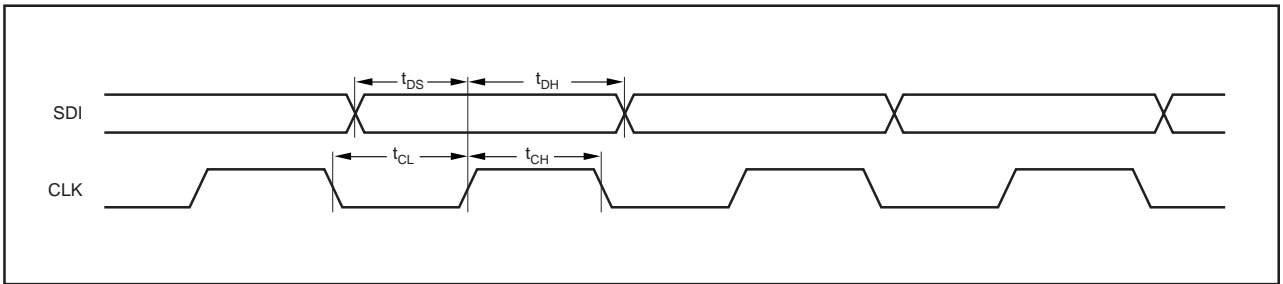
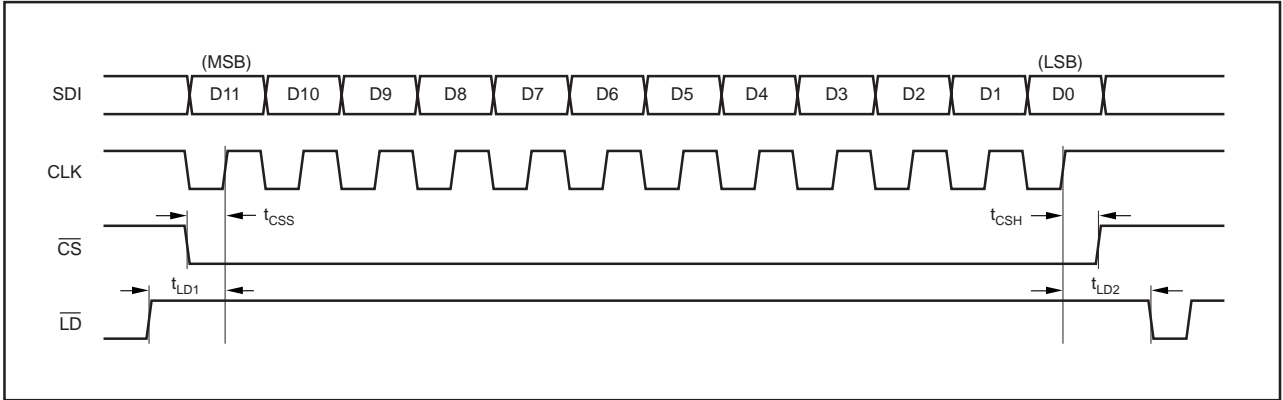
| PRODUCT   | MINIMUM RELATIVE ACCURACY (LSB) | DIFFERENTIAL NONLINEARITY (LSB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE     | PACKAGE DRAWING NUMBER <sup>(1)</sup> | ORDERING NUMBER <sup>(2)</sup> | TRANSPORT MEDIA |
|-----------|---------------------------------|---------------------------------|---------------------------------|-------------|---------------------------------------|--------------------------------|-----------------|
| DAC7611P  | ±2                              | ±1                              | -40°C to +85°C                  | 8-Pin DIP   | 006                                   | DAC7611P                       | Rails           |
| DAC7611U  | ±2                              | ±1                              | -40°C to +85°C                  | 8-Lead SOIC | 182                                   | DAC7611U                       | Rails           |
| "         | "                               | "                               | "                               | "           | "                                     | DAC7611U/2K5                   | Tape and Reel   |
| DAC7611PB | ±1                              | ±1                              | -40°C to +85°C                  | 8-Pin DIP   | 006                                   | DAC7611PB                      | Rails           |
| DAC7611UB | ±1                              | ±1                              | -40°C to +85°C                  | 8-Lead SOIC | 182                                   | DAC7611UB                      | Rails           |
| "         | "                               | "                               | "                               | "           | "                                     | DAC7611UB/2K5                  | Tape and Reel   |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "DAC7611/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

# EQUIVALENT INPUT LOGIC



## TIMING DIAGRAMS



## LOGIC TRUTH TABLE

| $\overline{\text{CS}}^{(1)}$ | $\text{CLK}^{(1)}$ | $\overline{\text{CLR}}$ | $\overline{\text{LD}}$ | SERIAL SHIFT REGISTER | DAC REGISTER                              |
|------------------------------|--------------------|-------------------------|------------------------|-----------------------|---|
| H                            | X                  | H                       | H                      | No Change             | No Change                                 |
| L                            | L                  | H                       | H                      | No Change             | No Change                                 |
| L                            | H                  | H                       | H                      | No Change             | No Change                                 |
| L                            | ↑                  | H                       | H                      | Advanced One Bit      | No Change                                 |
| ↑                            | L                  | H                       | H                      | Advanced One Bit      | No Change                                 |
| H <sup>(2)</sup>             | X                  | H                       | ↓                      | No Change             | Changes to Value of Serial Shift Register |
| H <sup>(2)</sup>             | X                  | H                       | L <sup>(3)</sup>       | No Change             | Transparent                               |
| H                            | X                  | L                       | X                      | No Change             | Loaded with 000 <sub>H</sub>              |
| H                            | X                  | ↑                       | H                      | No Change             | Latched with 000 <sub>H</sub>             |

↑ Positive Logic Transition; ↓ Negative Logic Transition; X = Don't Care.

NOTES: (1)  $\overline{\text{CS}}$  and  $\text{CLK}$  are interchangeable. (2) A HIGH value is suggested in order to avoid to "false clock" from advancing the shift register and changing the DAC voltage. (3) If data is clocked into the serial register while  $\overline{\text{LD}}$  is LOW, the DAC output voltage will change, reflecting the current value of the serial shift register.

## TIMING SPECIFICATIONS

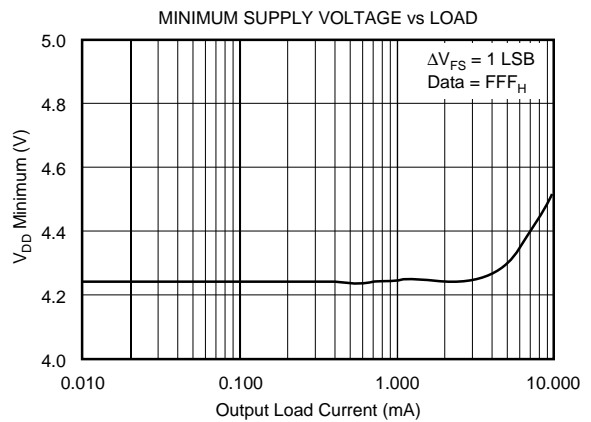
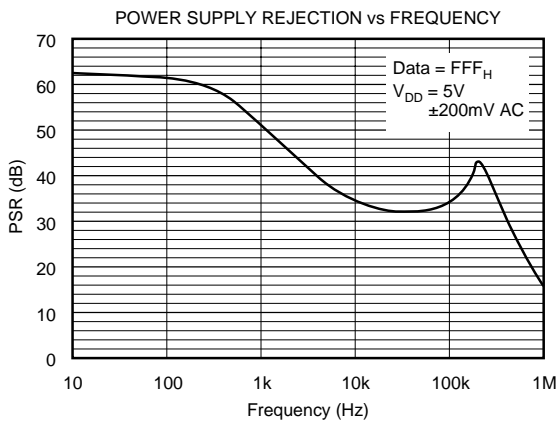
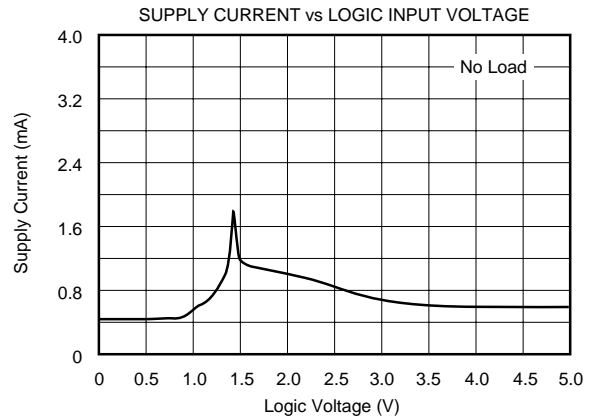
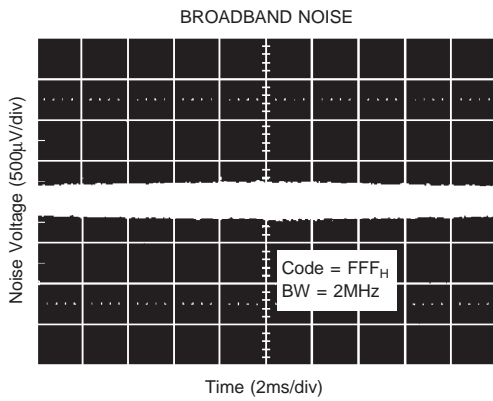
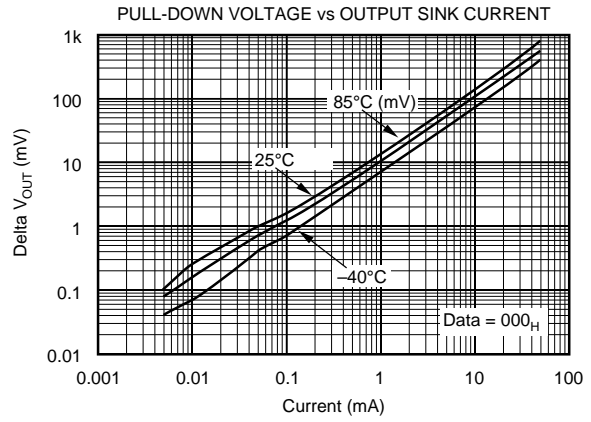
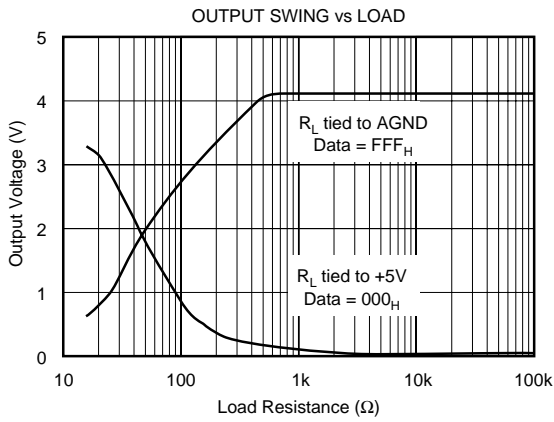
$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  and  $V_{DD} = +5\text{V}$ .

| SYMBOL             | DESCRIPTION       | MIN | TYP | MAX | UNITS |
|--------------------|-------------------|-----|-----|-----|-------|
| $t_{\text{CH}}$    | Clock Width HIGH  | 30  |     |     | ns    |
| $t_{\text{CL}}$    | Clock Width LOW   | 30  |     |     | ns    |
| $t_{\text{LDW}}$   | Load Pulse Width  | 20  |     |     | ns    |
| $t_{\text{DS}}$    | Data Setup        | 15  |     |     | ns    |
| $t_{\text{DH}}$    | Data Hold         | 15  |     |     | ns    |
| $t_{\text{CLR W}}$ | Clear Pulse Width | 30  |     |     | ns    |
| $t_{\text{LD1}}$   | Load Setup        | 15  |     |     | ns    |
| $t_{\text{LD2}}$   | Load Hold         | 10  |     |     | ns    |
| $t_{\text{CSS}}$   | Select            | 30  |     |     | ns    |
| $t_{\text{CSH}}$   | Deselect          | 20  |     |     | ns    |

NOTE: All input control signals are specified with  $t_R = t_F = 5\text{ns}$  (10% to 90% of +5V) and timed from a voltage level of 1.6V. These parameters are guaranteed by design and are not subject to production testing.

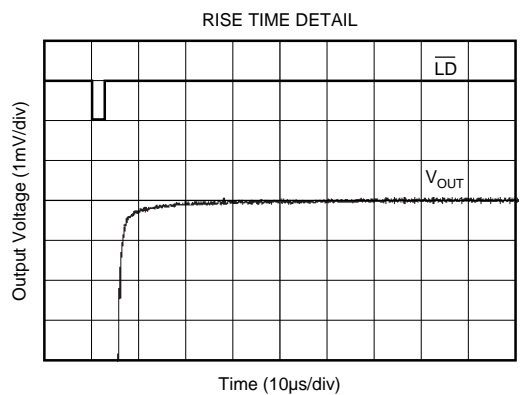
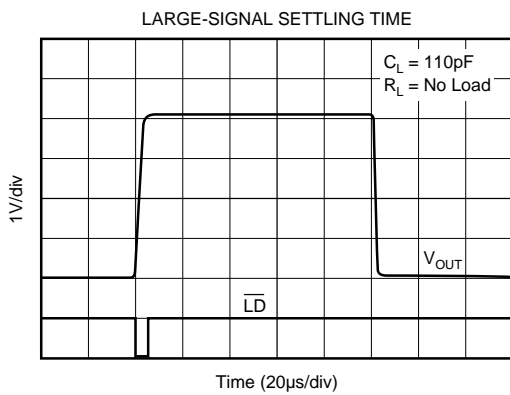
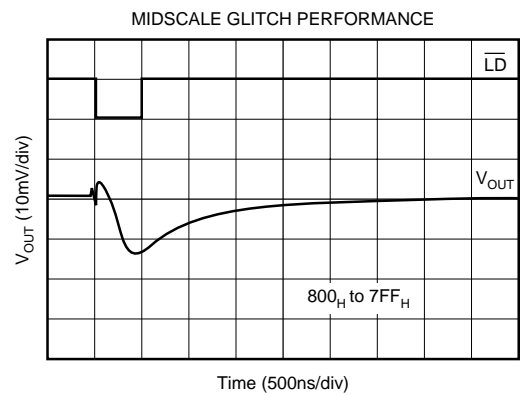
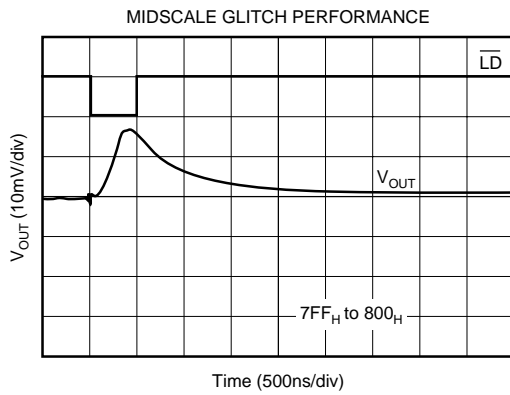
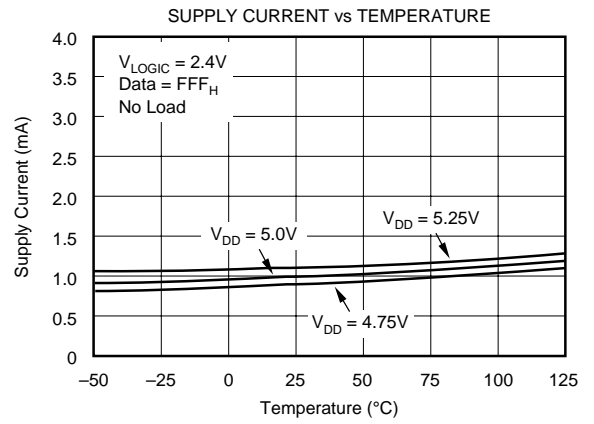
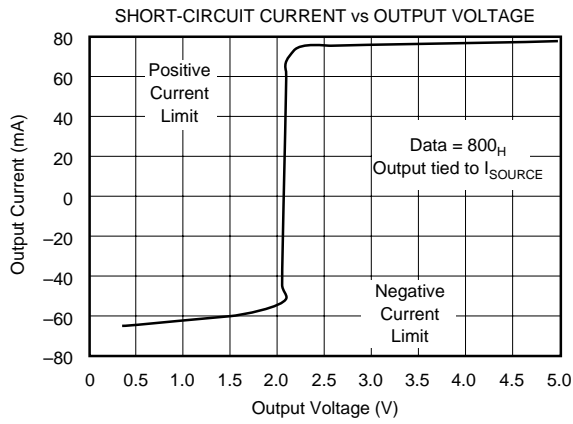
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ$ , and  $V_{DD} = 5V$ , unless otherwise specified.



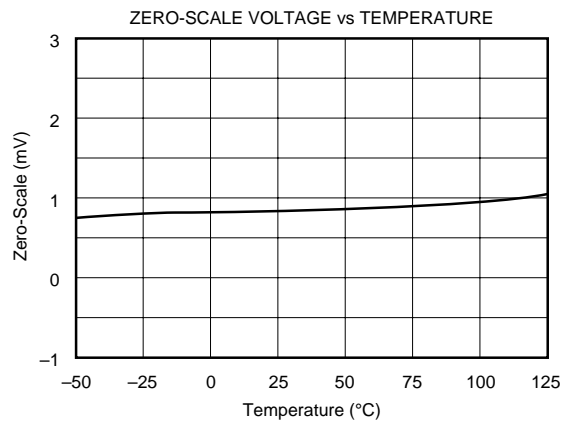
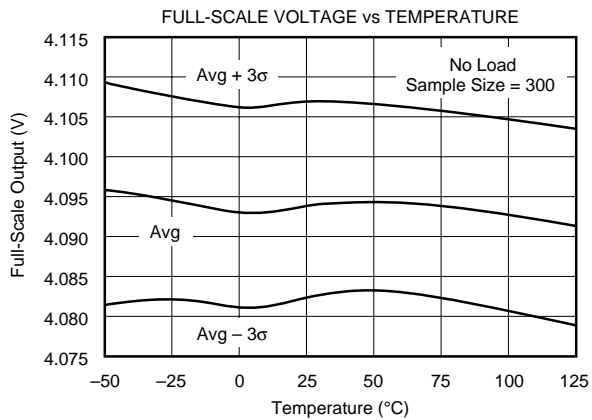
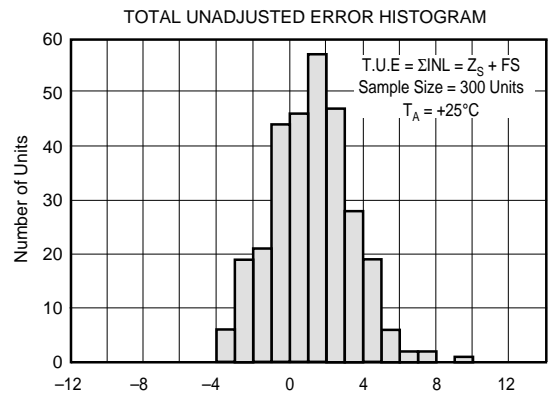
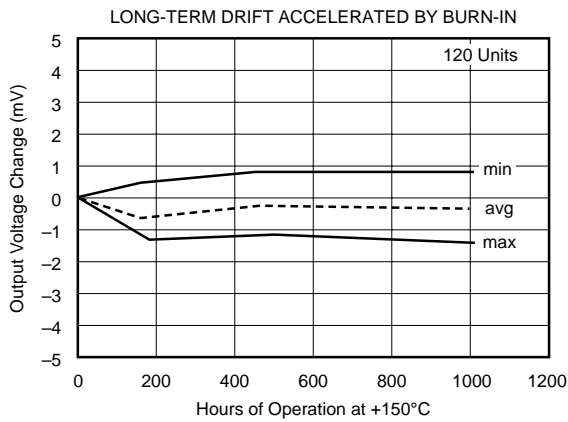
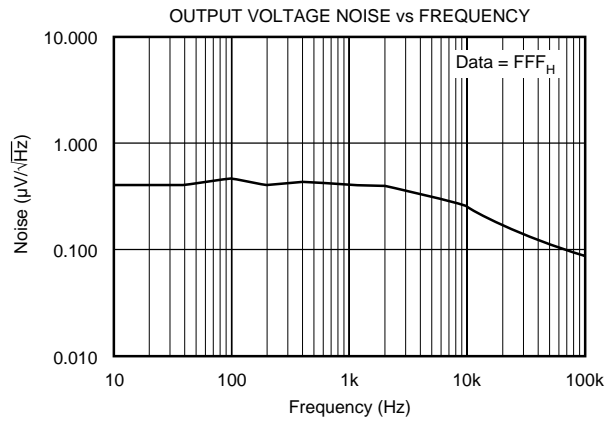
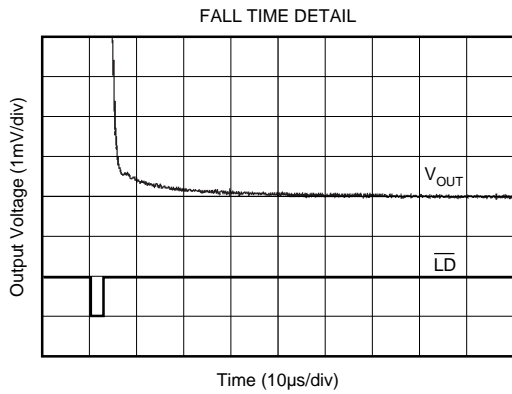
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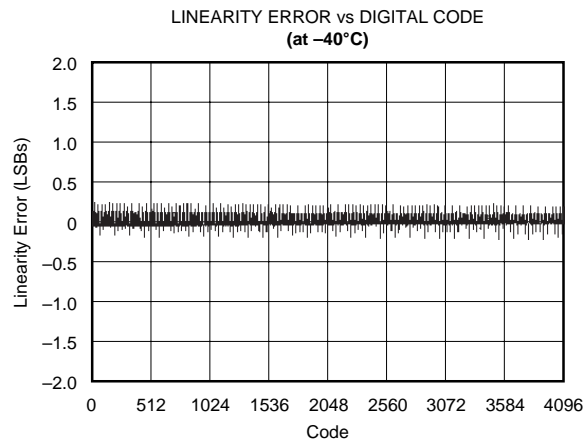
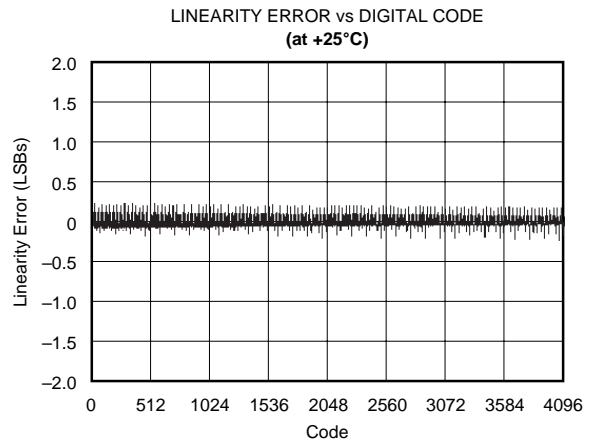
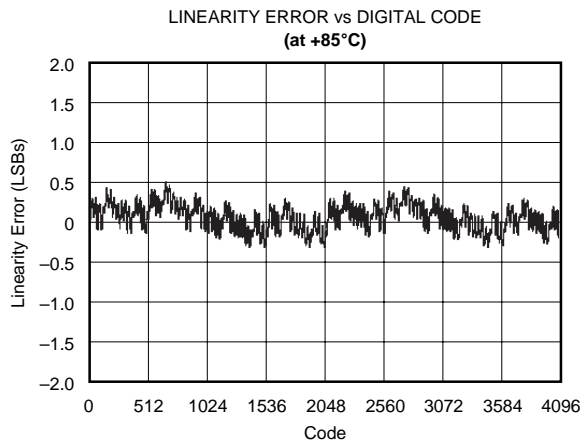
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ$ , and  $V_{DD} = 5V$ , unless otherwise specified.



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ$ , and  $V_{DD} = 5V$ , unless otherwise specified.



# OPERATION

The DAC7611 is a 12-bit digital-to-analog converter (DAC) complete with a serial-to-parallel shift register, DAC register, laser-trimmed 12-bit DAC, on-board reference, and a rail-to-rail output amplifier. Figure 1 shows the basic operation of the DAC7611.

## INTERFACE

Figure 1 shows the basic connection between a microcontroller and the DAC7611. The interface consists of a serial clock (CLK), serial data (SDI), and a load strobe signal ( $\overline{LD}$ ). In addition, a chip select ( $\overline{CS}$ ) input is available to enable serial communication when there are multiple serial devices. The data format is Straight Binary and is loaded MSB-first into the shift registers. An asynchronous

clear input ( $\overline{CLR}$ ) is provided to simplify start-up or periodic resets. Table I shows the relationship between input code and output voltage.

The digital data into the DAC7611 is double-buffered. This means that new data can be entered into the DAC without disturbing the old data and the analog output of the converter. At some point after the data has been entered into the serial shift register, this data can be transferred into the DAC register. This transfer is accomplished with a HIGH to LOW transition of the  $\overline{LD}$  pin. However, the  $\overline{LD}$  pin makes the DAC register transparent. If new data is shifted into the shift register while  $\overline{LD}$  is LOW, the DAC output voltage will change as each new bit is entered. To prevent this,  $\overline{LD}$  must be returned HIGH prior to shifting in new serial data.

At any time, the contents of the DAC register can be set to  $000_H$  (analog output equals 0V) by taking the  $\overline{CLR}$  input LOW. The DAC register will remain at this value until  $\overline{CLR}$  is returned HIGH and  $\overline{LD}$  is taken LOW to allow the contents of the shift register to be transferred to the DAC register. If  $\overline{LD}$  is LOW when  $\overline{CLR}$  is taken LOW, the DAC register will be set to  $000_H$  and the analog output driven to 0V. When  $\overline{CLR}$  is returned HIGH, the DAC register will be set to the current value in the serial shift register and the analog output will respond accordingly.

| DAC7611 Full-Scale Range = 4.095V<br>Least Significant Bit = 1mV |                      |                  |
|--|----------------------|------------------|
| DIGITAL INPUT CODE<br>STRAIGHT BINARY                            | ANALOG OUTPUT<br>(V) | DESCRIPTION      |
| FFF <sub>H</sub>   | +4.095               | Full Scale       |
| 801 <sub>H</sub>   | +2.049               | Midscale + 1 LSB |
| 800 <sub>H</sub>   | +2.048               | Midscale         |
| 7FF <sub>H</sub>   | +2.047               | Midscale - 1 LSB |
| 000 <sub>H</sub>   | 0                    | Zero Scale       |

TABLE I. Digital Input Code and Corresponding Ideal Analog Output.

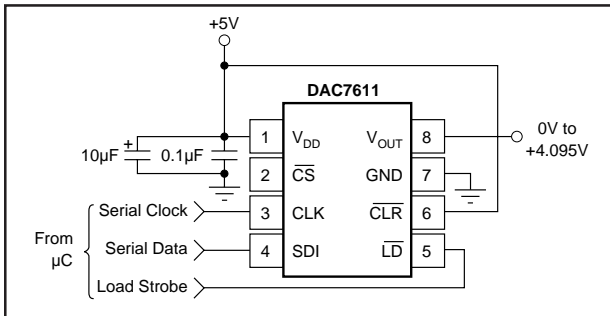


FIGURE 1. Basic Operation of the DAC7611.

## DIGITAL-TO-ANALOG CONVERTER

The internal DAC section is a 12-bit voltage output device that swings between ground and the internal reference voltage. The DAC is realized by a laser-trimmed R-2R ladder network which is switched by N-channel MOSFETs. The DAC output is internally connected to the rail-to-rail output operational amplifier.

## OUTPUT AMPLIFIER

A precision, low-power amplifier buffers the output of the DAC section and provides additional gain to achieve a 0 to 4.095V range. The amplifier has low offset voltage, low noise, and a set gain of 1.682V/V ( $4.095/2.435$ ). See Figure 2 for an equivalent circuit schematic of the analog portion of the DAC7611.

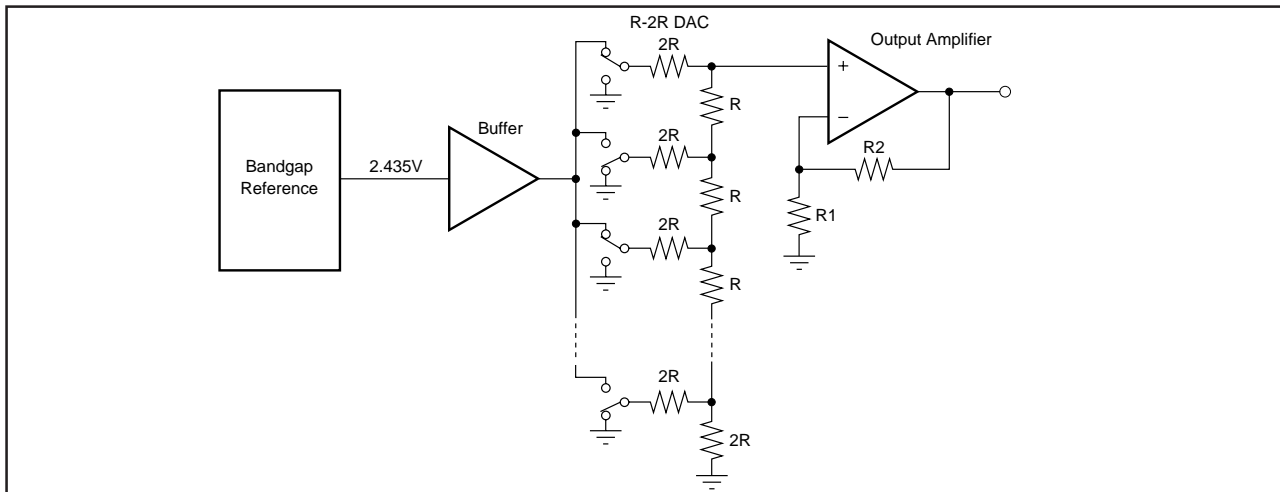


FIGURE 2. Simplified Schematic of Analog Portion.

The output amplifier has a  $7\mu\text{s}$  typical settling time to  $\pm 1$  LSB of the final value. Note that there are differences in the settling time for negative-going signals versus positive-going signals.

The rail-to-rail output stage of the amplifier provides the full-scale range of 0V to 4.095V while operating on a supply voltage as low as 4.75V. In addition to its ability to drive resistive loads, the amplifier will remain stable while driving capacitive loads of up to 500pF. See Figure 3 for an equivalent circuit schematic of the amplifier's output driver and the Typical Performance Curves section for more information regarding settling time, load driving capability, and output noise.

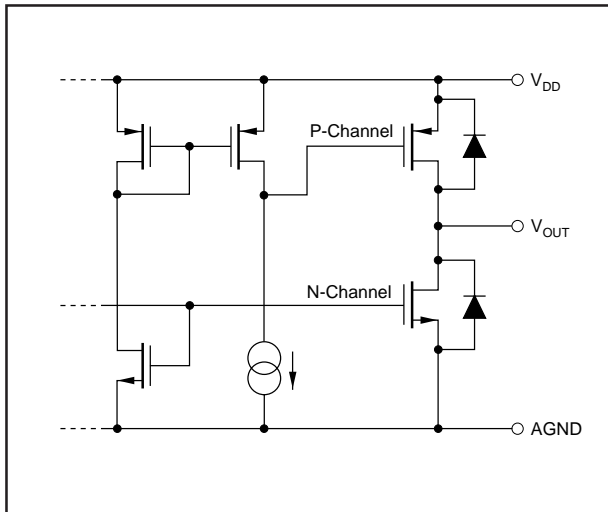


FIGURE 3. Simplified Driver Section of Output Amplifier.

## POWER SUPPLY

A BiCMOS process and careful design of the bipolar and CMOS sections of the DAC7611 result in a very low power device. Bipolar transistors are used where tight matching and low noise are needed to achieve analog accuracy, and CMOS transistors are used for logic, switching functions and for other low power stages.

If power consumption is critical, it is important to keep the logic levels on the digital inputs ( $\overline{\text{SDI}}$ ,  $\overline{\text{CLK}}$ ,  $\overline{\text{CS}}$ ,  $\overline{\text{LD}}$ ,  $\overline{\text{CLR}}$ ) as close as possible to either  $V_{\text{DD}}$  or ground. This will keep the CMOS inputs (see “Supply Current vs Logic Input Voltages” in the Typical Performance Curves) from shunting current between  $V_{\text{DD}}$  and ground. Thus, CMOS logic levels rather than TTL logic levels, are strongly recommended for driving the DAC7611.

The DAC7611 power supply should be bypassed as shown in Figure 1. The bypass capacitors should be placed as close to the device as possible, with the 0.1 $\mu\text{F}$  capacitor taking priority in this regard. The Power Supply Rejection vs Frequency graph in the Typical Performance Curves section shows the PSRR performance of the DAC7611. This should be taken into account when using switching power supplies or DC/DC converters.

In addition to offering guaranteed performance with  $V_{\text{DD}}$  in the 4.75V to 5.25V range, the DAC7611 will operate with reduced performance down to 4.5V. Operation between 4.5V and 4.75V will result in longer settling time, reduced performance, and current sourcing capability. Consult the  $V_{\text{DD}}$  vs Load Current graph in the Typical Performance Curves section for more information.

## APPLICATIONS

### POWER AND GROUNDING

The DAC7611 can be used in a wide variety of situations—from low power, battery operated systems to large-scale industrial process control systems. In addition, some applications require better performance than others, or are particularly sensitive to one or two specific parameters. This diversity makes it difficult to define definite rules to follow concerning the power supply, bypassing, and grounding. The following discussion must be considered in relation to the desired performance and needs of the particular system.

A precision analog component requires careful layout, adequate bypassing, and a clean, well-regulated power supply. As the DAC7611 is a single-supply, +5V component, it will often be used in conjunction with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance.

Because the DAC7611 has a single ground pin, all return currents, including digital and analog return currents, must flow through this pin. The GND pin is also the ground reference point for the internal bandgap reference. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they are connected at the power entry point of the system (see Figure 4).

The power applied to  $V_{\text{DD}}$  should be well regulated and low-noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between  $V_{\text{DD}}$  and  $V_{\text{OUT}}$ .

As with the GND connection,  $V_{DD}$  should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 10 $\mu$ F and 0.1 $\mu$ F capacitors shown in Figure 4 are strongly recommended and should be installed as close to  $V_{DD}$  and ground as possible. In some situations, additional bypassing may be required such as a 100 $\mu$ F electrolytic capacitor or even a “Pi” filter made up of inductors and capacitors—all designed to essentially lowpass filter the +5V supply, removing the high frequency noise (see Figure 4).

### OFFSET ERROR MEASUREMENT

As with most DACs, the DAC7611 can have an offset error (or zero scale error) which is either negative or positive. If the error is positive, the output voltage for an input code of 000<sub>H</sub> will be greater than 0V. If the error is negative, the output voltage is below 0V. However, since the DAC7611 is a single-supply device and cannot swing below ground, the output voltage will be 0V, giving the impression that the offset error is zero.

Since measuring the offset error on a DAC is such a common task, a method is needed to reliably measure the offset error of the DAC7611. This can easily be done as shown in Figure 5. The resistor between  $V_{OUT}$  and a negative voltage provides the output amplifier some ability to swing below ground.

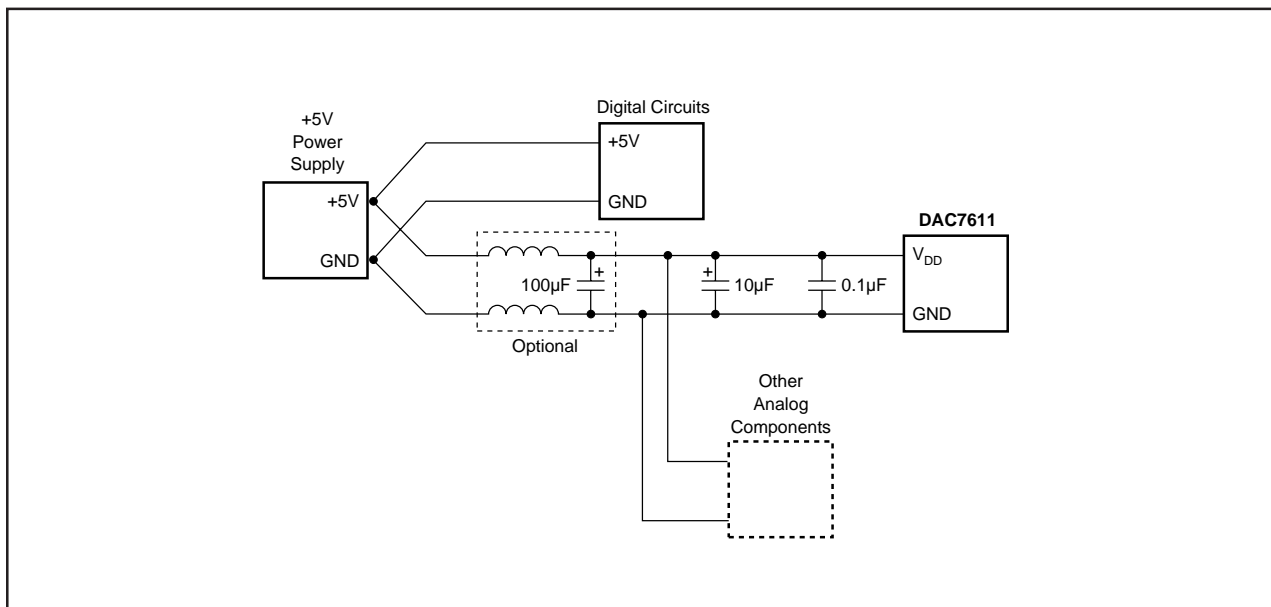


FIGURE 4. Suggested Power and Ground Connections for a DAC7611 Sharing a +5V Supply with a Digital System.

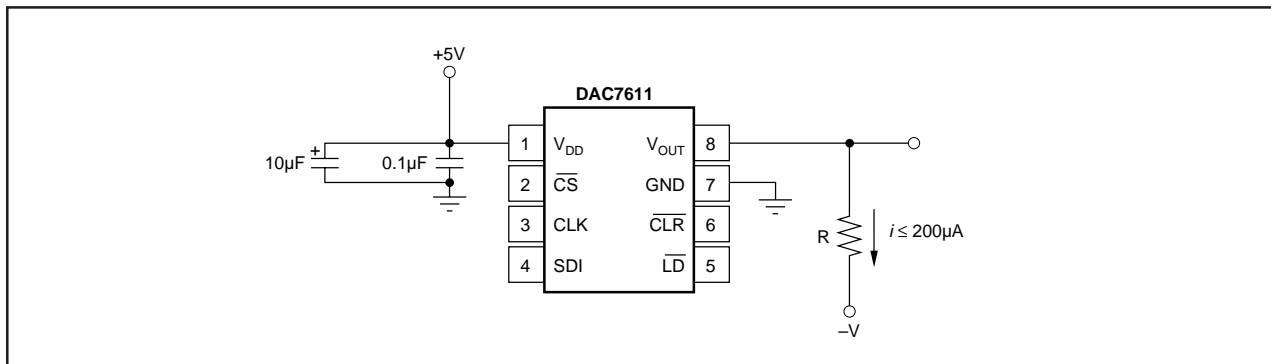


FIGURE 5. Offset Error Measurement Circuit.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| DAC7611P         | NRND                  | PDIP         | P               | 8    | 50          | TBD                     | Call TI          | Level-NA-NA-NA               |
| DAC7611PB        | NRND                  | PDIP         | P               | 8    | 50          | TBD                     | Call TI          | Level-NA-NA-NA               |
| DAC7611U         | ACTIVE                | SOIC         | D               | 8    | 100         | TBD                     | CU NIPDAU        | Level-3-220C-168 HR          |
| DAC7611U/2K5     | ACTIVE                | SOIC         | D               | 8    | 2500        | TBD                     | CU NIPDAU        | Level-3-220C-168 HR          |
| DAC7611UB        | ACTIVE                | SOIC         | D               | 8    | 100         | TBD                     | CU NIPDAU        | Level-3-220C-168 HR          |
| DAC7611UB/2K5    | ACTIVE                | SOIC         | D               | 8    | 2500        | TBD                     | CU NIPDAU        | Level-3-220C-168 HR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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