+2.7 V to +5.5 V, I²C INTERFACE, VOLTAGE OUTPUT, 10-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Micropower Operation: 125 µA @ 3 V**
- **Fast Update Rate: 188 kSPS**
- **Power-On Reset to Zero**
- **+2.7 V to +5.5 V Power Supply**
- **Specified Monotonic by Design**
- **I²C™ Interface up to 3.4 Mbps**
- **On-Chip Output Buffer Amplifier, Rail-to-Rail Operation**
- **Double-Buffered Input Register**
- **Address Support for up to Two DAC6571s**
- **Small 6 Lead SOT 23 Package**
- **Operation From -40°C to 105°C**

APPLICATIONS

- **Process Control**
- **Data Acquistion Systems**
- **Closed-Loop Servo Control**
- **PC Peripherals**
- **Portable Instrumentation**

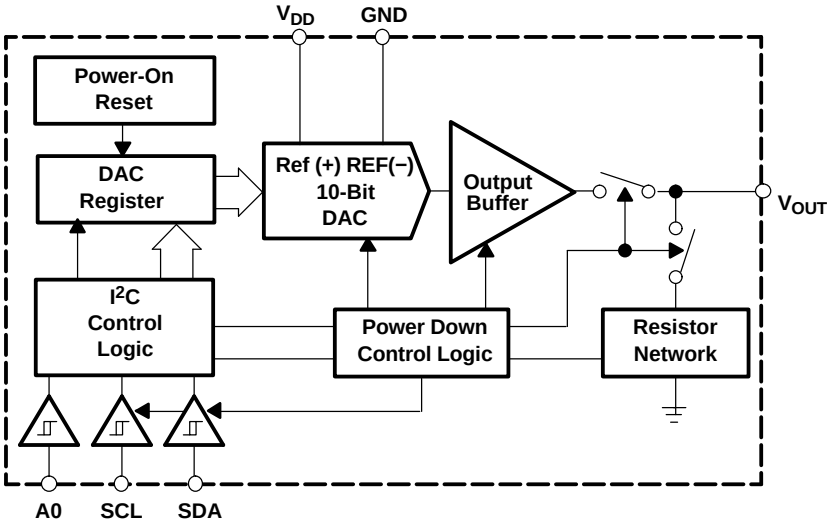
DESCRIPTION

The DAC6571 is a low-power, single channel, 10-Bit buffered voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC6571 utilizes an I²C compatible two wire serial interface that operates at clock rates up to 3.4 Mbps with address support of up to two DAC6571s on the same data bus.

The output voltage range of the DAC is 0 V to V_{DD}. The DAC6571 incorporates a power-on-reset circuit that ensures that the DAC output powers up at zero volts and remains there until a valid write to the device takes place. The DAC6571 contains a power-down feature, accessed via the internal control register, that reduces the current consumption of the device to 50 nA at 5 V.

The low power consumption of this part in normal operation makes it ideally suited for portable battery operated equipment. The power consumption is less than 0.7 mW at V_{DD} = 5 V reducing to 1 µW in power-down mode.

DAC7571/6571/5571 are 12/10/8 bit single channel I²C DACs from the same family. DAC7574/6574/5574 and DAC7573/6573/5573 are 12/10/8 bit quad channel I²C DACs. Also see DAC8571/8574 for single/quad channel 16-bit I²C DACs.



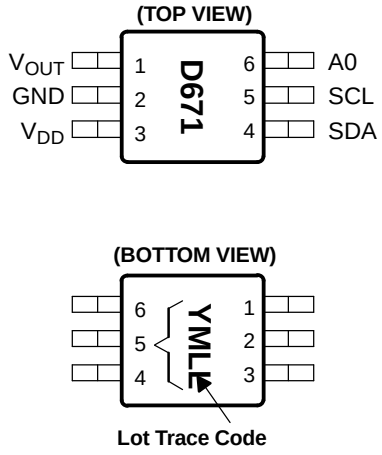
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC6571	SOT23-6	DBV	-40°C to +105°C	D671	DAC6571IDBVT	250 Piece Small Tape and Reel
					DAC6571IDBVR	3000 Piece Tape and Reel

PIN CONFIGURATIONS



PIN DESCRIPTION (SOT23-6)

PIN	NAME	DESCRIPTION
1	V_{OUT}	Analog output voltage from DAC
2	GND	Ground reference point for all circuitry on the part
3	V_{DD}	Analog Voltage Supply Input
4	SDA	Serial Data Input
5	SCL	Serial Clock Input
6	A0	Device Address Select
LOT TRACE CODE:	**Y**ear (3 = 2003); **M** onth (1–9 = JAN–SEP; A=OCT, B=NOV, C=DEC); **LL**– Random code generated when assembly is requested	

ABSOLUTE MAXIMUM RATINGS(1)

		UNITS
V_{DD} to GND		-0.3V to +6V
Digital Input voltage to GND		-0.3 V to +V_{DD} + 0.3 V
V_{OUT} to GND		-0.3 V to +V_{DD} + 0.3 V
Operating temperature range		-40°C to + 105°C
Storage temperature range		-65°C to + 150°C
Junction temperature range (T_J max)		+ 150°C
Power dissipation		($T_J$max - T_A)$R_{\Theta JA}$
Thermal impedance, $R_{\Theta JA}$		240°C/W
Lead temperature, soldering	Vapor phase (60s)	215°C
	Infrared (15s)	220°C

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications -40°C to +105°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC6571			UNITS
		MIN	TYP	MAX	
STATIC PERFORMANCE(1)					
Resolution		10			Bits
Relative accuracy				±2	LSB
Differential nonlinearity	Assured monotonic by design			±0.5	LSB
Zero code error	All zeroes loaded to DAC register		5	20	mV
Full-scale error	All ones loaded to DAC register		-0.15	-1.25	% of FSR
Gain error				±1.25	% of FSR
Zero code error drift			±7		µV/°C
Gain temperature coefficient			±3		ppm of FSR/°C
OUTPUT CHARACTERISTICS(2)					
Output voltage range		0		V_{DD}	V
Output voltage settling time	1/4 Scale to 3/4 scale change (400_H to $C00_H$) ; R_L = ∞		7	9	µ s
Slew rate			1		V/µs
Capacitive load stability	R_L = ∞		470		pF
	R_L = 2kΩ		1000		pF
Code change glitch impulse	1 LSB Change around major carry		20		nV-s
Digital feedthrough			0.5		nV-s
DC output impedance			1		Ω
Short-circuit current	V_{DD} = +5V		50		mA
	V_{DD} = +3V		20		mA
Power-up time	Coming out of power-down mode, V_{DD} = +5V		2.5		µ s
	Coming out of power-down mode, V_{DD} = +3V		5		µ s
LOGIC INPUTS(2)					
Input current				± 1	µ A
$V_{IN}L$, Input low voltage	V_{DD} = +3V			$0.3\times V_{DD}$	V
$V_{IN}H$, Input high voltage	V_{DD} = +5V	$0.7\times V_D$ D			V
Pin capacitance				3	pF
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
I_{DD} (normal operation)	DAC active and excluding load current				
V_{DD} = +3.6V to +5.5V	$V_{IH} = V_{DD}$ and V_{IL} = GND		155	200	µ A
V_{DD} = +2.7V to +3.6V	$V_{IH} = V_{DD}$ and V_{IL} = GND		125	160	µ A
I_{DD} (all power-down modes)					
V_{DD} = +3.6 V to +5.5V	$V_{IH} = V_{DD}$ and V_{IL} = GND		0.2	1	µ A
V_{DD} = +2.7V to +3.6V	$V_{IH} = V_{DD}$ and V_{IL} = GND		0.05	1	µ A
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2mA, V_{DD} = +5V		93		%

(1) Linearity calculated using a reduced code range of 12 to 1012; output unloaded.
(2) Specified by design and characterization, not production tested.

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		High-speed mode, C_B - 100pF max			3.4	MHz
		High-Speed mode, C_B - 400pF max			1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HD}; t_{STA}	Hold Time (Repeated) START Condition	Standard mode	4.0			µs
		Fast mode	600			ns
		High-speed mode	160			ns
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
		High-speed mode, C_B - 100pF max	160			ns
		High-speed mode, C_B - 400pF max	320			ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4.0			µs
		Fast mode	600			ns
		High-speed mode, C_B - 100pF max	60			ns
		High-speed mode, C_B - 400pF max	120			ns
t_{SU}; t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7			µs
		Fast mode	600			ns
		High-speed mode	160			ns
t_{SU}; t_{DAT}	Data Setup Time	Standard mode	250			ns
		Fast mode	100			ns
		High-speed mode	10			ns
t_{HD}; t_{DAT}	Data Hold Time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
		High-speed mode, C_B - 100pF max	0		70	ns
		High-speed mode, C_B - 400pF max	0		150	ns
t_{RCL}	Rise Time of SCL Signal	Standard mode	$20 \times 0.1C_B$		1000	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		40	ns
		High-speed mode, C_B - 400pF max	20		80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	$20 \times 0.1C_B$		1000	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		80	ns
		High-speed mode, C_B - 400pF max	20		160	ns
t_{FCL}	Fall Time of SCL Signal	Standard mode	$20 \times 0.1C_B$		300	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		40	ns
		High-speed mode, C_B - 400pF max	20		80	ns
t_{RDA}	Rise Time of SDA Signal	Standard mode	$20 \times 0.1C_B$		1000	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		80	ns
		High-speed mode, C_B - 400pF max	20		160	ns
t_{FDA}	Fall Time of SDA Signal	Standard mode	$20 \times 0.1C_B$		300	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		80	ns
		High-speed mode, C_B - 400pF max	20		160	ns

TIMING CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{SU}; t_{STO}	Setup Time for STOP Condition	Standard mode	4.0			µs
		Fast mode	600			ns
		High-speed mode	160			ns
C_B	Capacitive Load for SDA and SCL				400	pF
t_{SP}	Pulse Width of Spike Suppressed	Fast mode			50	ns
		High-speed mode			10	ns
V_{NH}	Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	Standard mode	$0.2V_{DD}$			V
		Fast mode				
		High-speed mode				
V_{NL}	Noise Margin at the LOW Level for Each Connected Device (Including Hysteresis)	Standard mode	$0.1V_{DD}$			V
		Fast mode				
		High-speed mode				

TYPICAL CHARACTERISTICS: V_{DD} = +5 V

At T_A = +25°C, +V_{DD} = +5 V, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (-40°C)

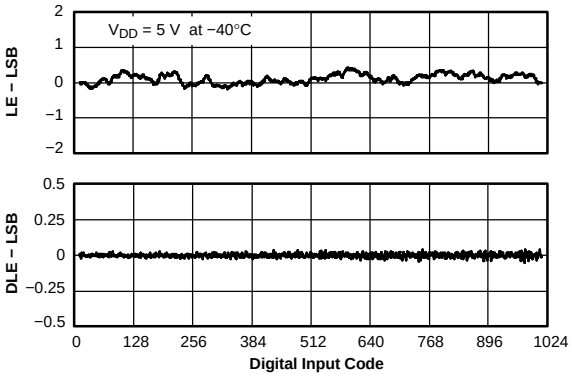


Figure 1.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (+25 ° C)

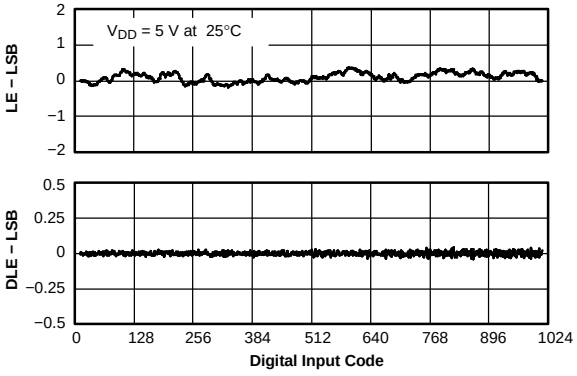


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (+105° C)

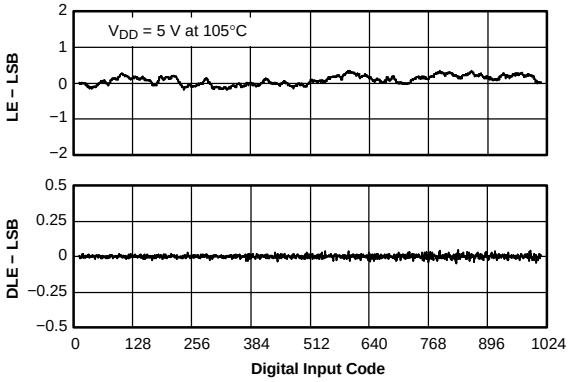


Figure 3.

TYPICAL TOTAL UNADJUSTED ERROR

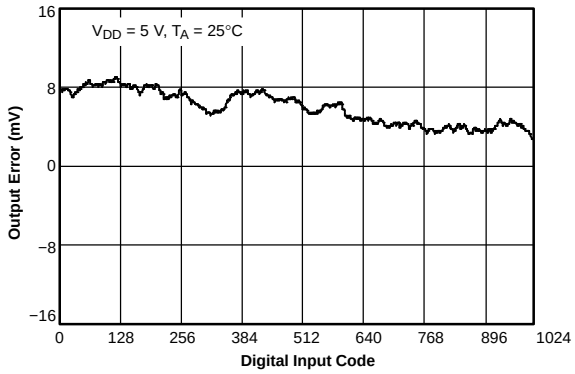


Figure 4.

ZERO-SCALE ERROR VS TEMPERATURE

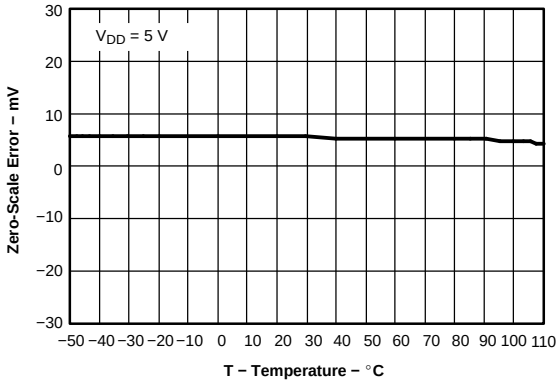


Figure 5.

FULL-SCALE ERROR VS TEMPERATURE

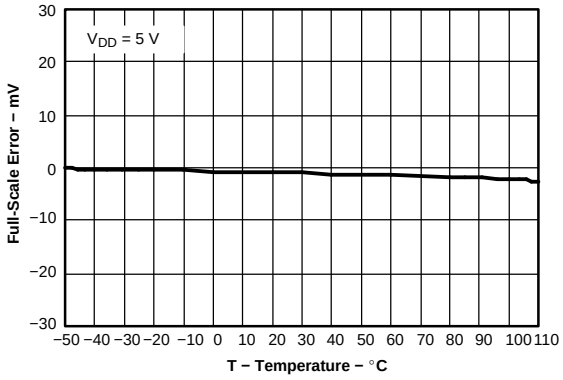


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

I_{DD} HISTOGRAM

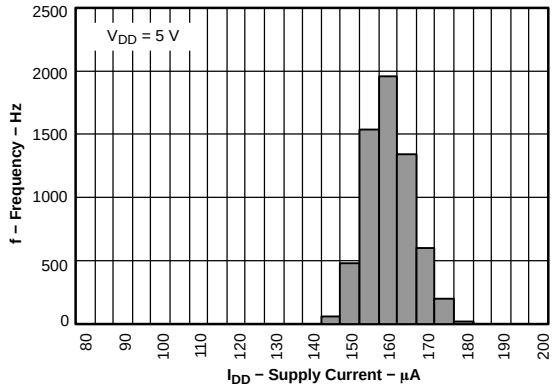


Figure 7.

SOURCE AND SINK CURRENT CAPABILITY

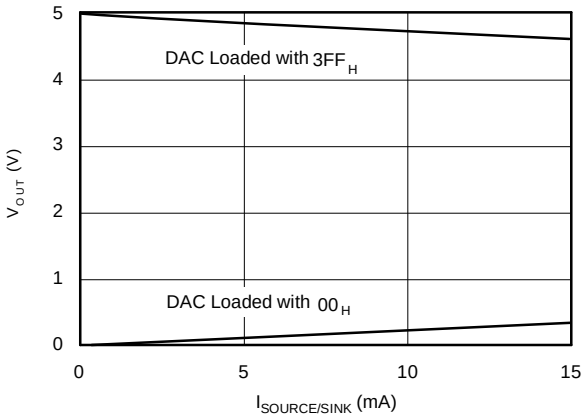


Figure 8.

SUPPLY CURRENT vs CODE

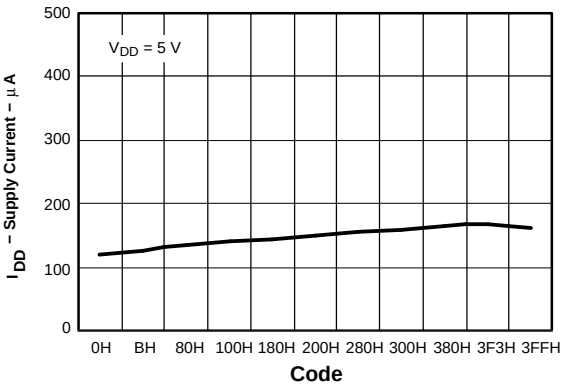


Figure 9.

SUPPLY CURRENT vs TEMPERATURE

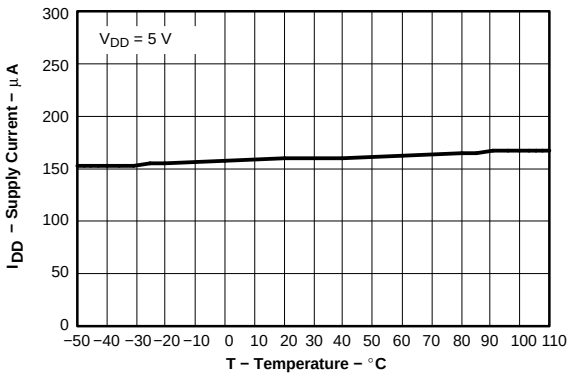


Figure 10.

SUPPLY CURRENT vs SUPPLY VOLTAGE

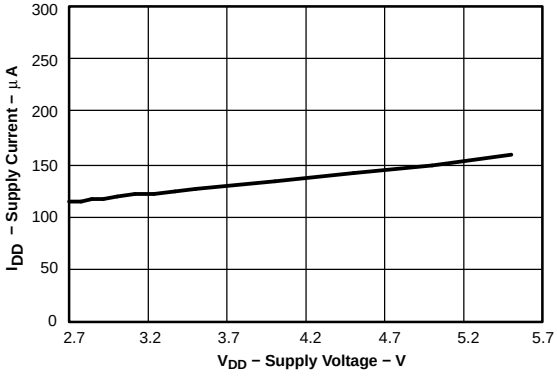


Figure 11.

POWER-DOWN CURRENT vs SUPPLY VOLTAGE

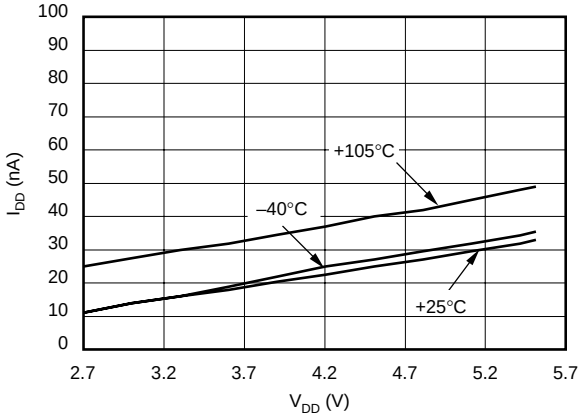


Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

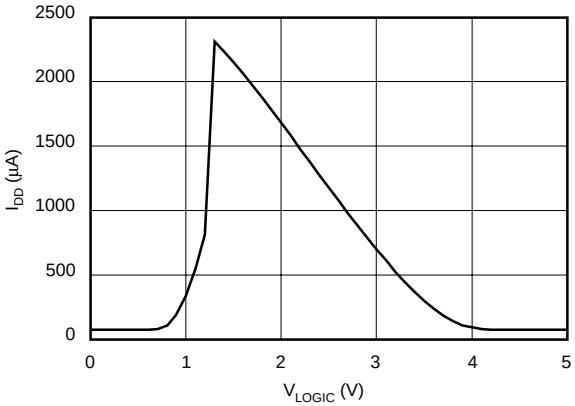


Figure 13.

FULL-SCALE SETTLING TIME

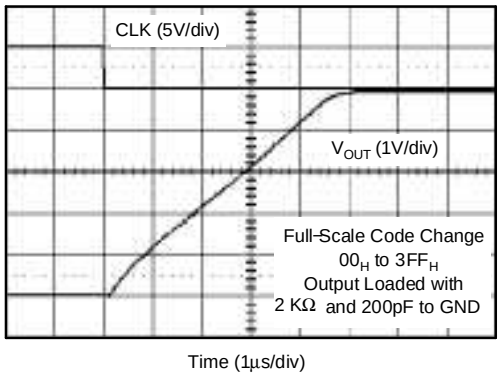


Figure 14.

FULL-SCALE SETTLING TIME

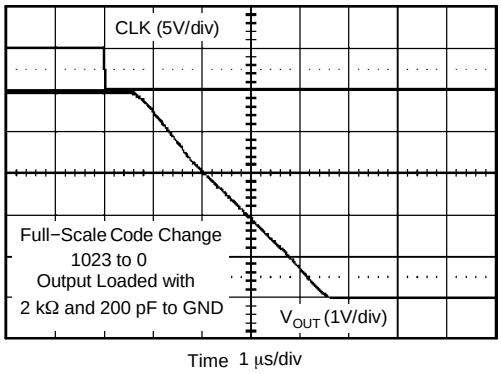


Figure 15.

HALF-SCALE SETTLING TIME

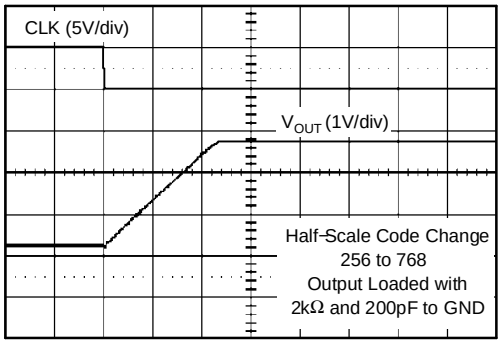


Figure 16.

HALF-SCALE SETTLING TIME

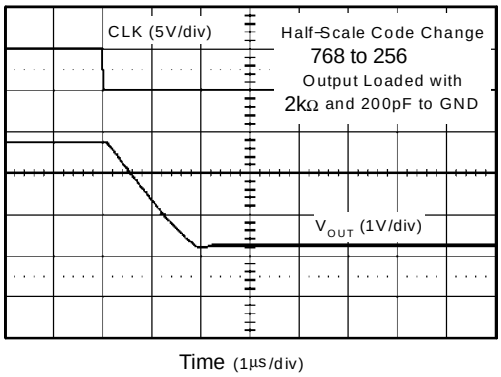


Figure 17.

POWER-ON RESET TO 0V

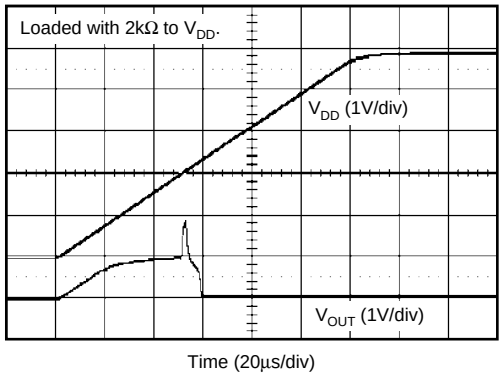


Figure 18.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

EXITING POWER-DOWN (512 Loaded)

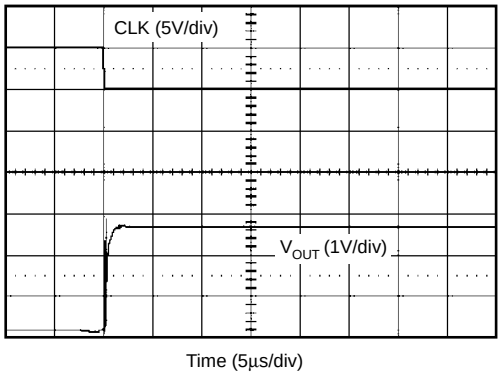


Figure 19.

CODE CHANGE GLITCH

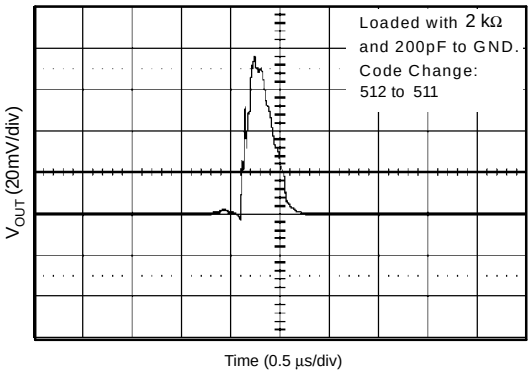


Figure 20.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (-40 °C)

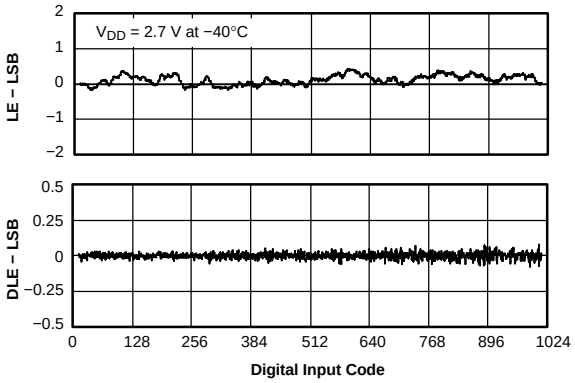


Figure 21.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (+25 °C)

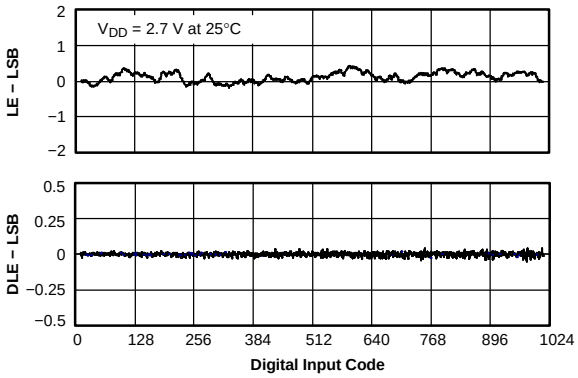


Figure 22.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (+105 °C)

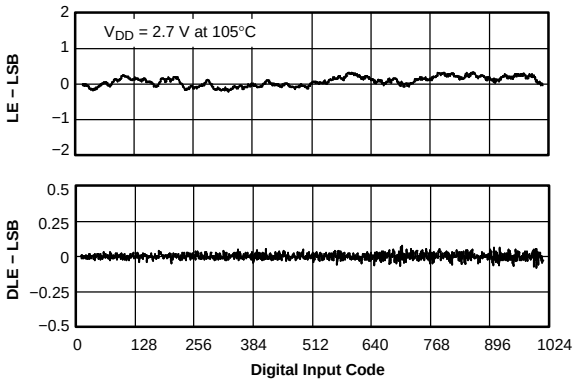


Figure 23.

OUTPUT ERROR VS CODE (+25 °C)

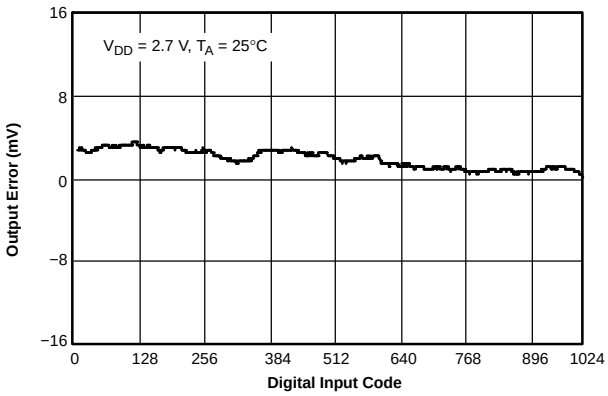


Figure 24.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

ZERO-SCALE ERROR vs TEMPERATURE

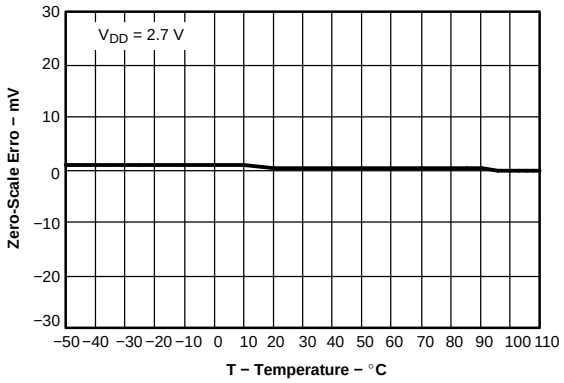


Figure 25.

FULL-SCALE ERROR vs TEMPERATURE

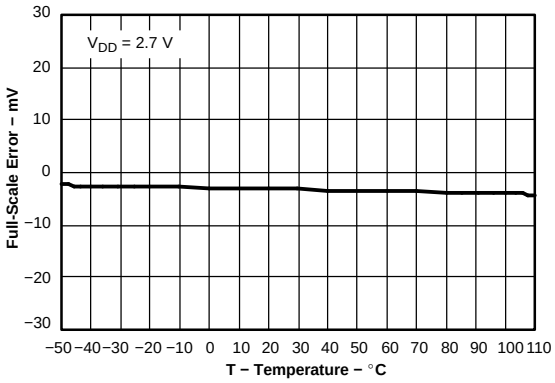


Figure 26.

I_{DD} HISTOGRAM

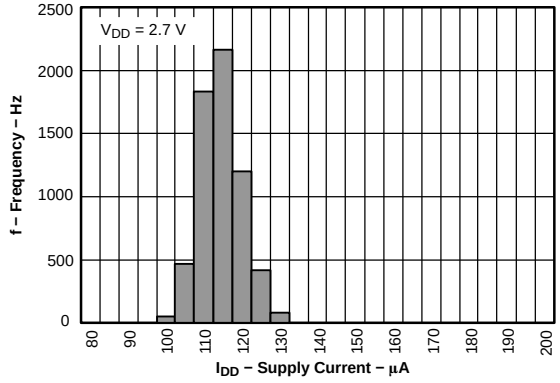


Figure 27.

SOURCE AND SINK CURRENT CAPABILITY

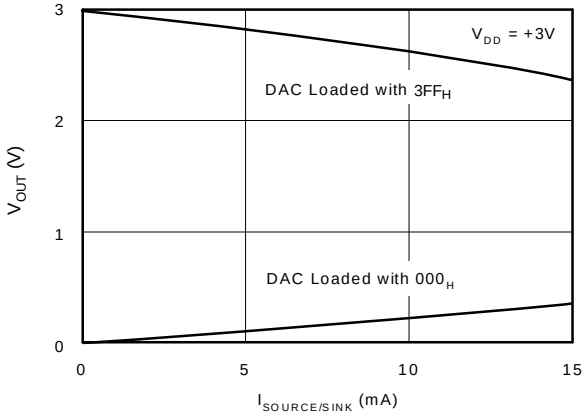


Figure 28.

SUPPLY CURRENT vs CODE

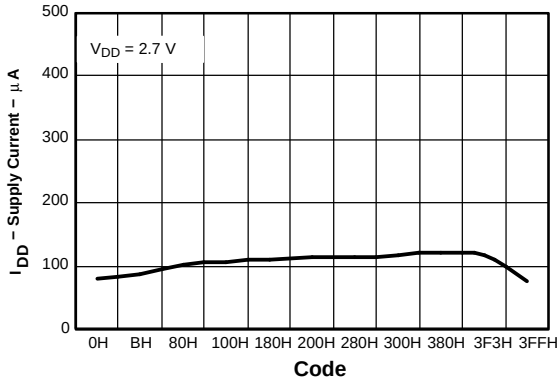


Figure 29.

SUPPLY CURRENT vs 9 TEMPERATURE

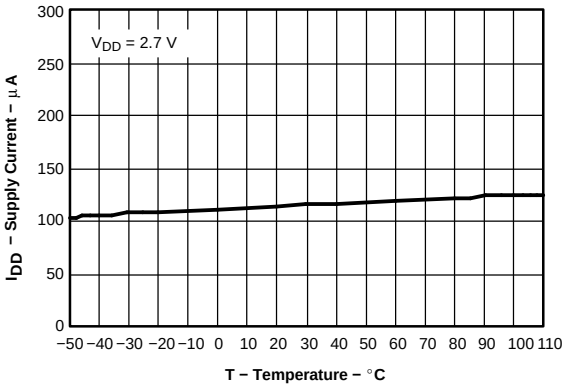


Figure 30.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

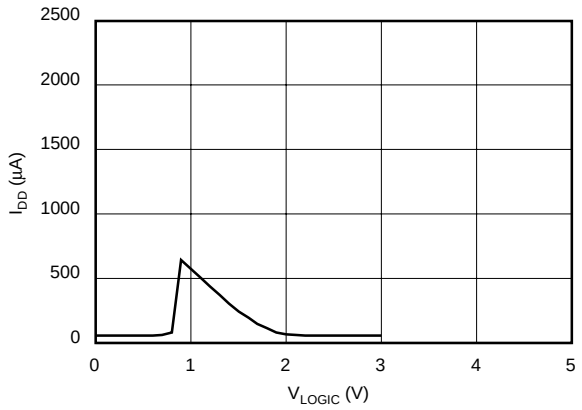


Figure 31.

FULL SCALE SETTLING TIME

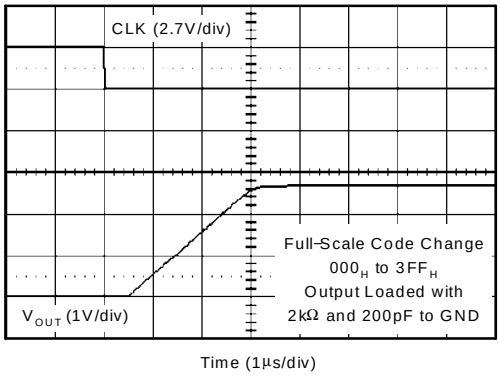


Figure 32.

FULL SCALE SETTLING TIME

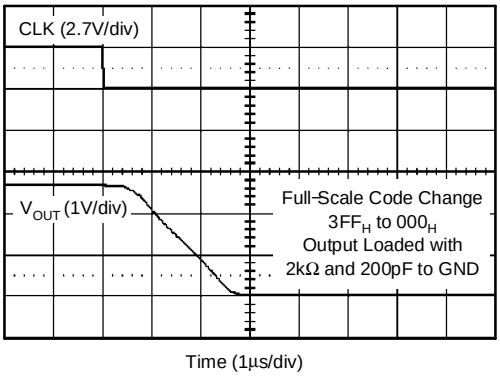


Figure 33.

HALF SCALE SETTLING TIME

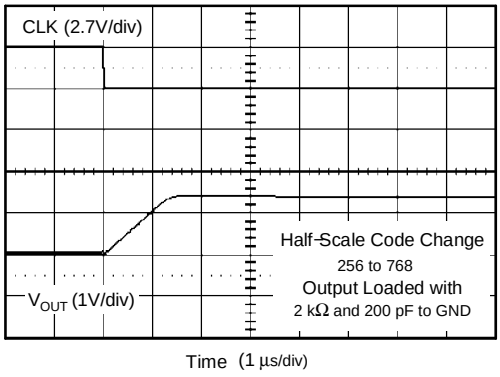


Figure 34.

HALF SCALE SETTLING TIME

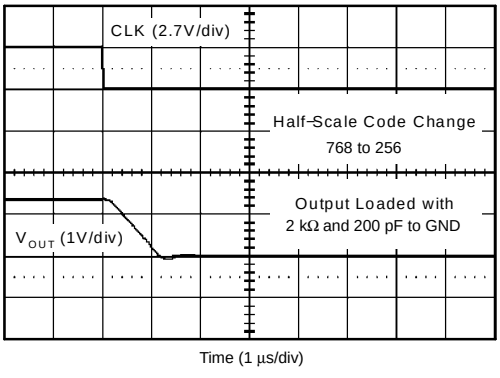


Figure 35.

POWER ON RESET 0 V

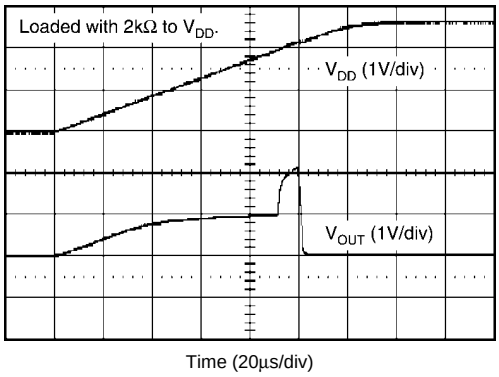


Figure 36.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

EXITING-POWER DOWN (512 Loaded)

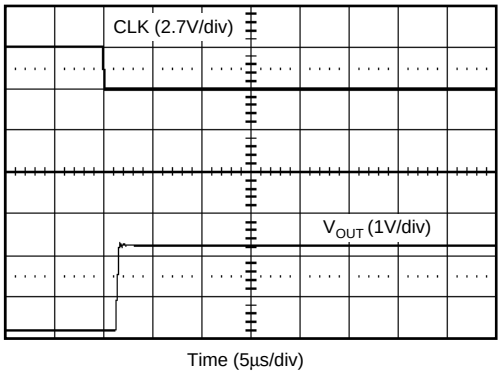


Figure 37.

CODE CHANGE GLITCH

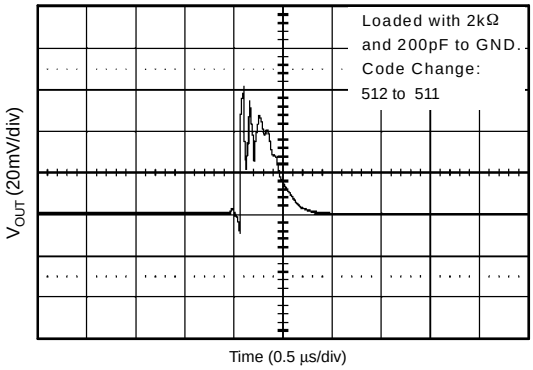


Figure 38.

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC6571 consists of a string DAC followed by an output buffer amplifier.Figure 39 shows a generalized block diagram of the DAC architecture.

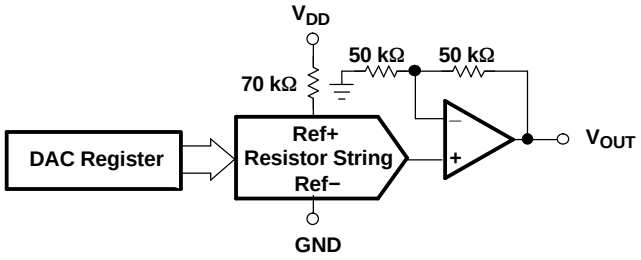


Figure 39. R-String DAC Architecture

The input coding to the DAC6571 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = V_{DD} \times \frac{D}{1024}$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 1023.

RESISTOR STRING

The resistor string section is shown in Figure 40. It is basically a divide-by-2 resistor, followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the ouptput amplifier by closing one of the switches connecting the string to the amplifier. Because the acrhitecture consists of a string of resistors, it is specified monotonic.

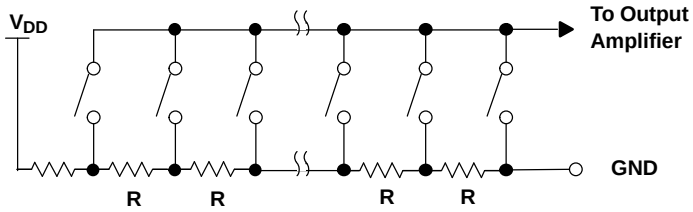


Figure 40. Typical Resistor String

Output Amplifier

The output buffer amplifier is a gain-of-2 amplifier, capable of generating rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics curves. The slew rate is 1 V/µs with a half-scale settling time of 7 µs with the output unloaded.

I²C Interface

I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.

THEORY OF OPERATION (continued)

The DAC6571 works as a slave and supports the following data transfer *modes*, as defined in the I^2C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as HS-mode. The DAC6571 supports 7-bit addressing; 10-bit addressing and general call address are *not* supported.

F/S-Mode Protocol

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 41. All I^2C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses, and transmits the 7-bit address and the *read/write direction bit* R/$\overline{W}$ on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 42). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 43) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/$\overline{W}$ bit 1) or *receive* data from the slave (R/$\overline{W}$ bit 0). In either case, the *receiver* needs to acknowledge the data sent by the *transmitter*. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 41). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

HS-Mode Protocol

- When the bus is idle, both SDA and SCL lines are pulled high by the pullup devices.
- The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.
- The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode.

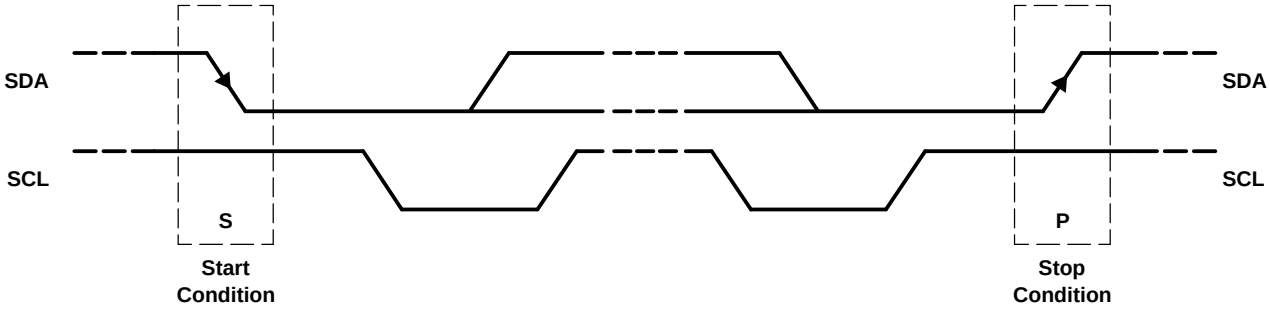


Figure 41. START and STOP Conditions

THEORY OF OPERATION (continued)

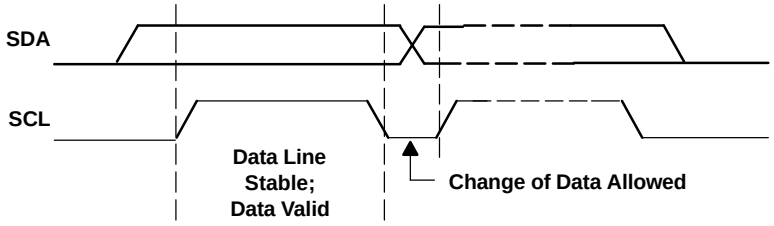


Figure 42. Bit Transfer on the I^2C Bus

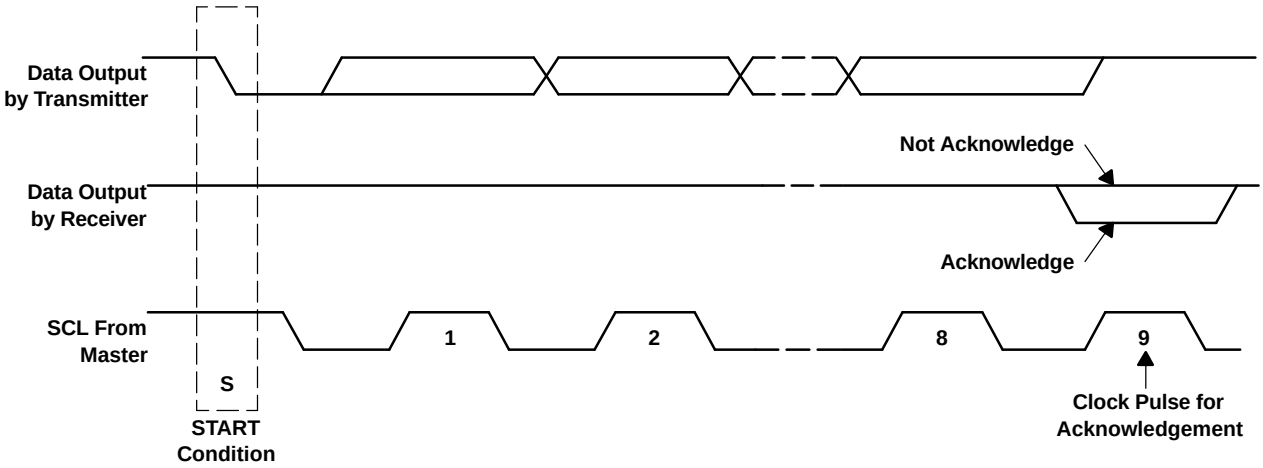


Figure 43. Acknowledge on the I^2C Bus

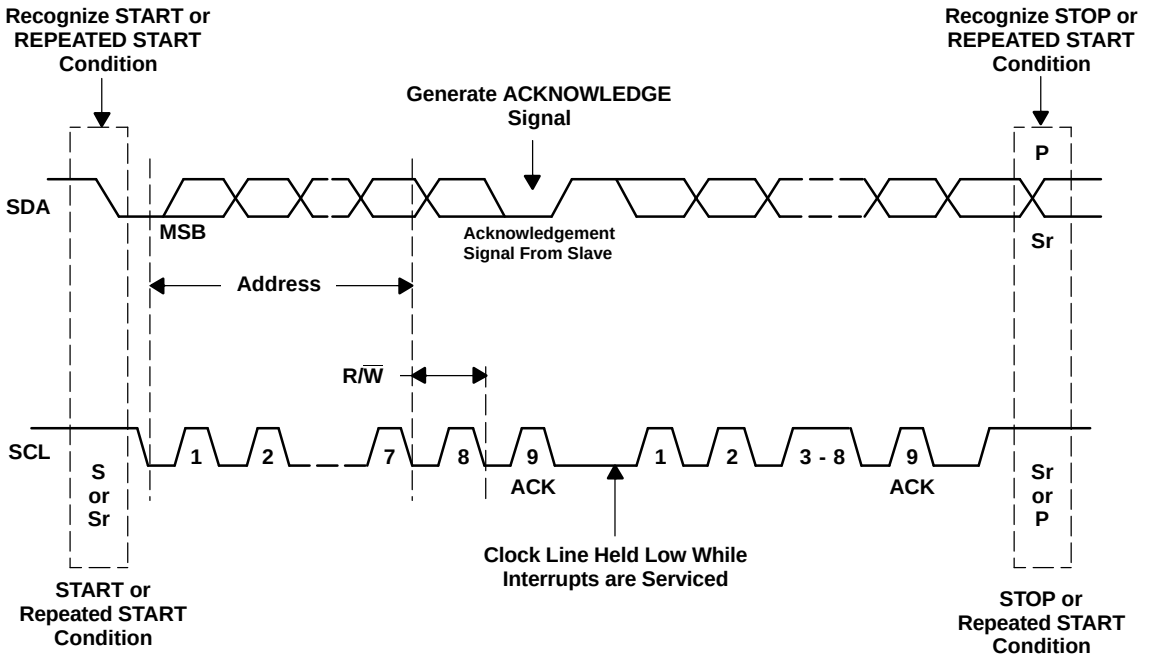


Figure 44. Bus Protocol

THEORY OF OPERATION (continued)

DAC6571 I²C Update Sequence

The DAC6571 requires a start condition, a valid I²C address, a control-MSB byte, and an LSB byte for a single update. After the receipt of each byte, DAC6571 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the DAC6571. The CTRL/MSB byte sets the operational mode of the DAC6571, and the 4 most significant bits. The DAC6571 then receives the LSB byte containing 6 least significant data bits. DAC6571 performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

For the first update, DAC6571 requires a start condition, a valid I²C address, a CTRL/MSB byte, an LSB byte. For all consecutive updates, DAC6571 needs a CTRL/MSB byte, and an LSB byte.

Using the I²C high-speed mode (f_{scl}= 3.4 MHz), the clock running at 3.4 MHz, each 10-bit DAC update other than the first update can be done within 18 clock cycles (CTRL/MSB byte, acknowledge signal, LSB byte, acknowledge signal), at 188.88 KSPS. Using the fast mode (f_{scl}= 400 kHz), clock running at 400 kHz, maximum DAC update rate is limited to 22.22 KSPS. Once a stop condition is received, DAC6571 releases the I²C bus and awaits a new start condition.

Address Byte

MSB							LSB
1	0	0	1	1	0	A0	0

The address byte is the first byte received following the START condition from the master device. The first six bits (MSBs) of the address are factory preset to 100110. The next bit of the address is the device select bit A0. The A0 address input can be connected to V_{DD} or digital GND, or can be actively driven by TTL/CMOS logic levels. The device address is set by the state of this pin during the power-up sequence of the DAC6571. Up to 2 devices (DAC6571) can be connected to the same I²C-Bus without requiring additional glue logic.

Broadcast Address Byte

MSB							LSB
1	0	0	1	0	0	0	0

Broadcast addressing is also supported by DAC6571. Broadcast addressing can be used for synchronously updating or powering down multiple DAC6571 devices. Using the broadcast address, DAC6571 responds regardless of the state of the address pin A0.

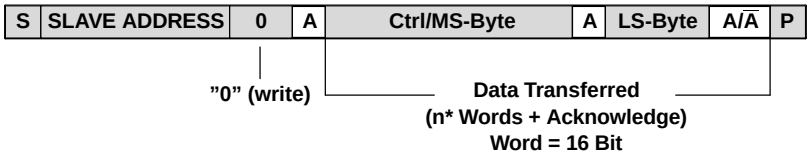
Control - Most Significant Byte

Most Significant Byte CTRL/MSB[7:0] consists of two zeros, two power-down bits, and four most significant bits of 10-bit unsigned binary D/A conversion data.

Least Significant Byte

Least Significant Byte LSB[7:0] consists of the 6 least significant bits of the 10-bit unsigned binary D/A conversion data, followed by 2 don't care bits. DAC6571 updates at the falling edge of the acknowledge signal that follows the LSB[0] bit.

Standard-and Fast-Mode:

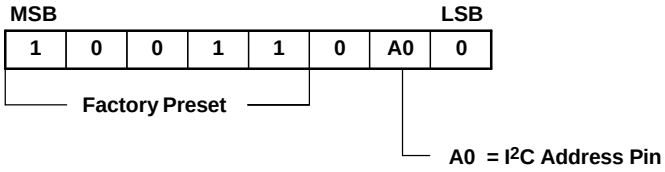


From Master to DAC6571

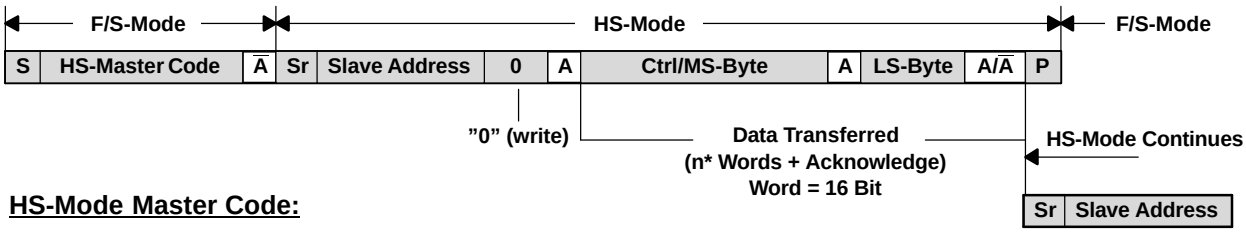
From DAC6571 to Master

A = Acknowledge (SDA LOW)
Ā = Not Acknowledge (SDA HIGH)
S = START Condition
Sr = Repeated START Condition
P = STOP Condition

DAC6571 I²C-SLAVE ADDRESS:



High-Speed-Mode (HS-Mode):



HS-Mode Master Code:

MSB							LSB
0	0	0	0	1	X	X	0

Ctrl/MS-Byte:

MSB							LSB
0	0	PD1	PD2	D9	D8	D7	D6

LS-Byte:

MSB							LSB
D5	D4	D3	D2	D1	D0	X	X

D9 − D0 = Data Bits

Figure 45. Master Transmitter Addressing DAC6571 as a Slave Receiver With a 7-Bit Address

POWER-ON RESET

The DAC6571 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0 V. It remains at a zero-code output until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the DAC output while it is in the process of powering up.

POWER-DOWN MODES

The DAC6571 contains four separate modes of operation. These modes are programmable via two bits (PD1 and PD0). Table 1 shows how the state of these bits correspond to the mode of operation.

Table 1. Modes of Operation for the DAC6571

PD1	PD0	OPERATING MODE
0	0	Normal Operation
0	1	1kΩ to AGND, PWD
1	0	100kΩ to AGND, PWD
1	1	High Impedance, PWD

When both bits are set to 0, the device works normally with normal power consumption of 150 µA at 5V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while in power-down mode. There are three different options: The output is connected internally to AGND through a 1 kΩ resistor, a 100 kΩ resistor, or it is left open-circuited (high impedance). The output stage is illustrated in Figure 46.

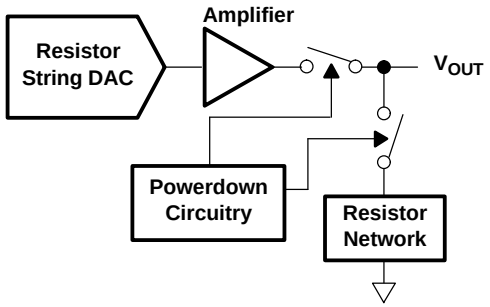


Figure 46. Output Stage During Power-Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time required to exit power down is typically 2.5 µs for AV_{DD} = 5 V and 5 µs for AV_{DD} = 3V. See the Typical Characteristics for more information.

CURRENT CONSUMPTION

The DAC6571 typically consumes 150 µA at V_{DD} = 5 V and 120 µA at V_{DD} = 3 V. Additional current consumption can occur due to the digital inputs if V_{IH} << V_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC. In power-down mode, typical current consumption is 200 nA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC6571 output stage is capable of driving loads of up to 1000 pF while remaining stable. Within the offset and gain error margins, the DAC6571 can operate rail-to-rail when driving a capacitive load. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This may occur within approximately the top 20 mV of the DAC's digital input-to-voltage output transfer characteristic.

OUTPUT VOLTAGE STABILITY

The DAC6571 exhibits excellent temperature stability of 5 ppm/°C typical output voltage drift over the specified temperature range of the device. This enables the output voltage to stay within a ±25 µV window for a ±1°C ambient temperature change. Combined with good dc noise performance and true 10-bit differential linearity, the DAC6571 becomes a perfect choice for closed-loop control applications.

APPLICATIONS

USING REF02 AS A POWER SUPPLY FOR THE DAC6571

Due to the extremely low supply current required by the DAC6571, a possible configuration is to use a REF02 +5 V precision voltage reference to supply the required voltage to the DAC6571's supply input as well as the reference input, as shown in Figure 47. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 will output a steady supply voltage for the DAC6571. If the REF02 is used, the current it needs to supply to the DAC6571 is 140 µA typical. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5 mW load on a given DAC output) is: 140 µA + (5 mW/5 V) = 1.14 mA.

The load regulation of the REF02 is typically (0.005%×V_{DD})/mA, which results in an error of 0.285 mV for the 1.14 mA current drawn from it. This corresponds to a 0.05 LSB error for a 0 V to 5 V output range.

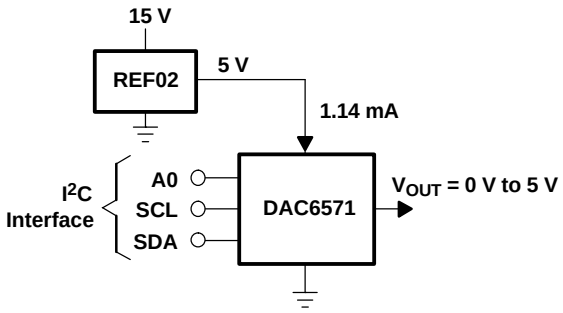


Figure 47. REF02 as Power Supply to DAC6571

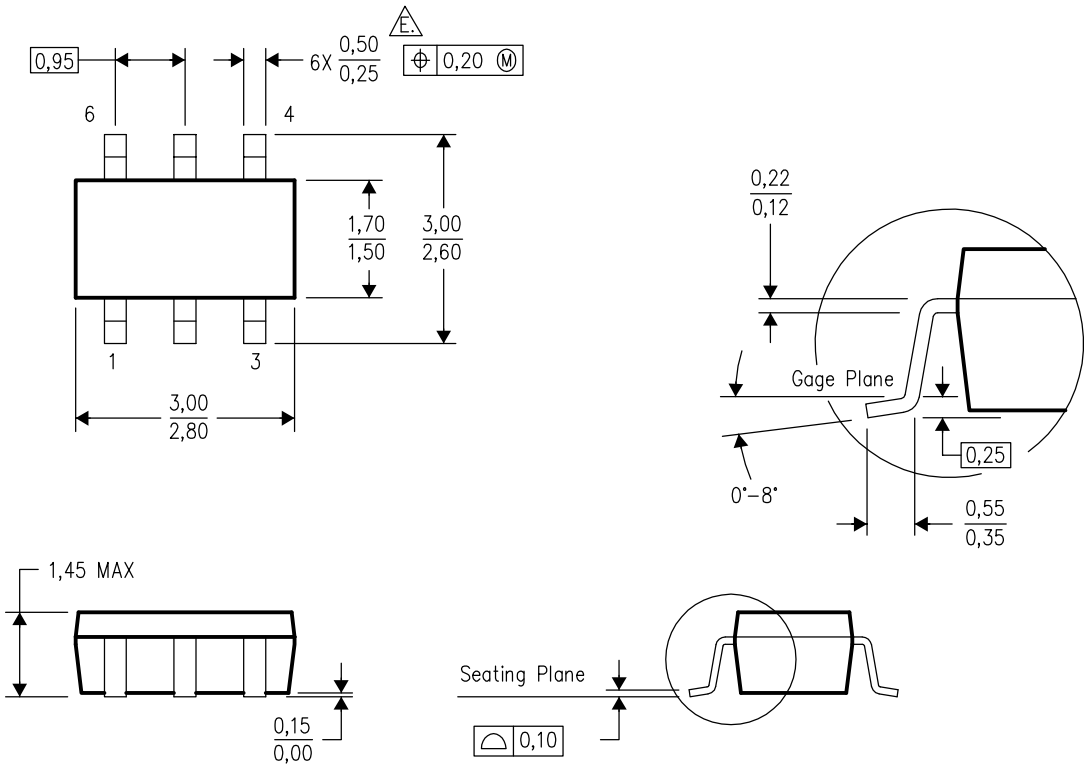
LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1 µF to 10 µF and 0.1 µF bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the +5V supply, removing the high-frequency noise.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/H 10/2003

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

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