Data Sheet | April 19, 2005 | FN1547.6

CMOS Serial Real-Time Clock With RAM and Power Sense/Control

The CDP68HC68T1 Real-Time Clock provides a time/calendar function, a 32 byte static RAM, and a 3 wire Serial Peripheral Interface (SPI Bus). The primary function of the clock is to divide down a frequency input that can be supplied by the on-board oscillator in conjunction with an external crystal or by an external clock source. The internal oscillator can operate with a 32kHz, 1MHz, 2MHz, or 4MHz crystal. An external clock source with a 32kHz, 1MHz, 2MHz, 4MHz, 50Hz or 60Hz frequency can be used to drive the CDP68HC68T1. The time registers hold seconds, minutes, and hours, while the calendar registers hold day-of-week, date, month, and year information. The data is stored in BCD format. In addition, 12 or 24 hour operation can be selected. In 12 hour mode, an AM/PM indicator is provided. The T1 has a programmable output which can provide one of seven outputs for use elsewhere in the system.

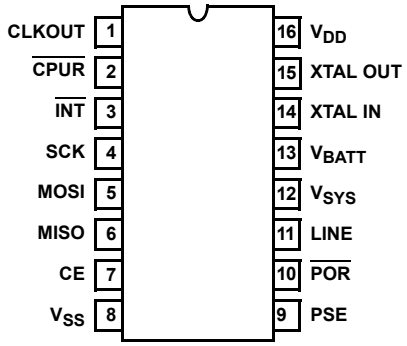
Computer handshaking is controlled with a “wired-OR” interrupt output. The interrupt can be programmed to provide a signal as the result of: 1) an alarm programmed to occur at a predetermined combination of seconds, minutes, and hours; 2) one of 15 periodic interrupts ranging from sub-second to once per day frequency; 3) a power fail detect. The PSE output and the V_{SYS} input are used for external power control. The $\overline{CPUR}$ output is available to reset the processor under power-down conditions. $\overline{CPUR}$ is enabled under software control and can also be activated via the CDP68HC68T1’s watchdog. If enabled, the watchdog requires a periodic toggle of the CE pin without a serial transfer.

Features

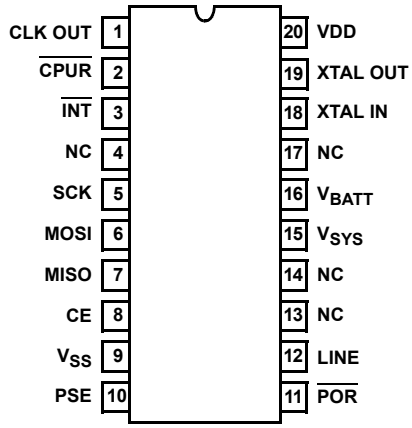
- SPI (Serial Peripheral Interface)
- Full Clock Features
  - Seconds, Minutes, Hours (12/24, AM/PM), Day of Week, Date, Month, Year (0-99), Automatic Leap Year
- 32 Word x 8-Bit RAM
- Seconds, Minutes, Hours Alarm
- Automatic Power Loss Detection
- Low Minimum Standby (Timekeeping) Voltage 2.2V
- Selectable Crystal or 50/60Hz Line Input
- Buffered Clock Output
- Battery Input Pin that Powers Oscillator and also Connects to V_{DD} Pin When Power Fails
- Three Independent Interrupt Modes
  - Alarm
  - Periodic
  - Power-Down Sense
- Pb-Free Available (RoHS Compliant)

Pinouts

CDP68HC68T1 (PDIP, SOIC)
TOP VIEW



CDP68HC68T1 (SOIC)
TOP VIEW



Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG DWG. #
CDP68HC68T1E	-40 to 85	16 Ld PDIP	E16.3
CDP68HC68T1EZ (Note)	-40 to 85	16 Ld PDIP** (Pb-free)	E16.3
CDP68HC68T1M*	-40 to 85	20 Ld SOIC	M20.3
CDP68HC68T1M2*	-40 to 85	16 Ld SOIC	M16.3
CDP68HC68T1M2Z* (Note)	-40 to 85	16 Ld SOIC (Pb-free)	M16.3

*Add “96” suffix for taoe and reel.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing. applications.
Pin number references throughout this specification refer to the 16 lead PDIP/SOIC. See pinouts for cross reference.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . -0.5V to +7V
Input Voltage, V_{IN} . . . . . V_{SS} -0.3V to V_{DD} +0.3V
Current Drain Per Input Pin Excluding V_{DD} and V_{SS}, I 10mA
Current Drain Per Output Pin, I 40mA

Operating Conditions

Voltage Range . . . . . +3.0V to +6.0V
Standby (Timekeeping) Voltage . . . . . +2.2V to +6.0V
Temperature Range
CDP68HC68T1E (PDIP Package) . . . . . -40°C to 85°C
CDP68HC68T1M/M2 (SOIC Packages) . . . . . -40°C to 85°C
Input High Voltage . . . . . ($0.7 \times V_{DD}$) to V_{DD}
Input Low Voltage . . . . . 0V to ($0.3 \times V_{DD}$)
Serial Clock Frequency (f_{SCK}) . . . . . +3.0V to +6.0V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
16 Ld PDIP*	90
16 Ld SOIC	100
20 Ld SOIC	95

Maximum Junction Temperature (Plastic) . . . . . 150°C
Maximum Storage Temperature Range (T_{STG}) . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC, Lead Tips Only)
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing. applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Static Electrical Specifications

At T_A = -40°C to +85°C, $V_{DD} = V_{BATT}$ = 5V ±5%, except as noted.

PARAMETER	CONDITIONS	CDP68HC68T1 MIN	CDP68HC68T1 (NOTE 2) TYP	CDP68HC68T1 MAX	UNITS
Quiescent Device Current I_{DD}		-	1	10	µA
Output Voltage High Level V_{OH}	I_{OH} = -1.6mA, V_{DD} = 4.5V	3.7	-	-	V
Output Voltage Low Level V_{OL}	I_{OL} = 1.6mA, V_{DD} = 4.5V	-	-	0.4	
Output Voltage High Level V_{OH}	$I_{OH} \leq 10\mu A$, V_{DD} = 4.5V	4.4	-	-	
Output Voltage Low Level V_{OL}	$I_{OL} \leq 10\mu A$, V_{DD} = 4.5V	-	-	0.1	
Input Leakage Current I_{IN}		-	-	±1	µA
Three-State Output Leakage Current I_{OUT}		-	-	±10	
Operating Current (Note 3) ($I_D + I_B$) $V_{DD} = V_B$ = 5V Crystal Operation	32kHz	-	0.08	0.01	mA
	1MHz	-	0.5	0.6	
	2MHz	-	0.7	0.84	
	4MHz	-	1	1.2	
Pin 14 External Clock (Squarewave) (Note 3) ($I_D + I_B$) $V_{DD} = V_S$ = 5V	32kHz	-	0.02	0.024	
	1MHz	-	0.1	0.12	
	2MHz	-	0.2	0.24	
	4MHz	-	0.4	0.5	
Standby Current (Note 3) I_B V_S = 3V Crystal Operation	32kHz	-	20	25	µA
	1MHz	-	200	250	
	2MHz	-	300	360	
	4MHz	-	500	600	

Operating Current (Note 3) V_{DD} = 5V, V_B = 3V Crystal Operation			I_D	I_B	I_D	I_S	mA
	32kHz	-	25	15	30	20	
	1MHz	-	0.08	0.15	0.1	0.18	
	2MHz	-	0.15	0.25	0.18	0.3	
	4MHz	-	0.3	0.4	0.36	0.5	

Static Electrical Specifications At T_A = -40°C to +85°C, V_{DD} = V_{BATT} = 5V ±5%, except as noted. **(Continued)**

PARAMETER	CONDITIONS	CDP68HC68T1			UNITS
		MIN	(NOTE 2) TYP	MAX	
Standby Current (Note 3) I_B V_B = 2.2V Crystal Operation	32kHz	-	10	12	µA
Input Capacitance C_{IN}	V_{IN} = 0, T_A = 25°C	-	-	2	pF
Maximum Rise and Fall Times t_r, t_f (Except XTAL Input and $\overline{POR}$ Pin 10)		-	-	2	µs
Input Voltage (Line Input Pin Only, Power Sense Mode)		0	10	12	V
$V_{SYS} > V_B V_T$ (For V_B Not Internally Connected to V_{DD})		-	1.0	-	V
Power-On Reset ($\overline{POR}$) Pulse Width		100	75	-	ns

NOTES:

2. Typical values are for T_A = 25°C and nominal V_{DD}.
3. Clock out (Pin 1) disabled, outputs open circuited. No serial access cycles.

Functional Block Diagram

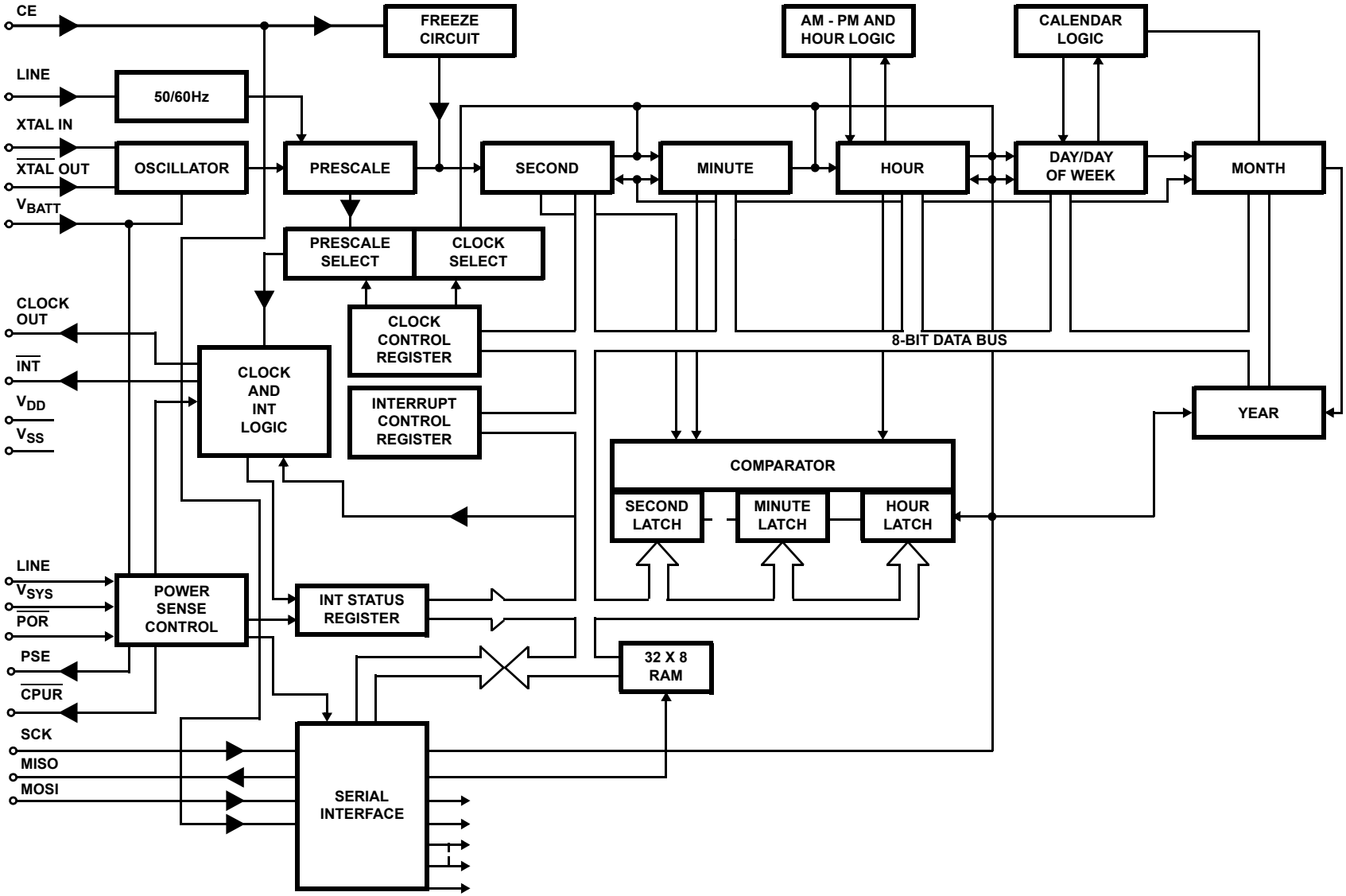


FIGURE 1. REAL TIME CLOCK FUNCTIONAL DIAGRAM

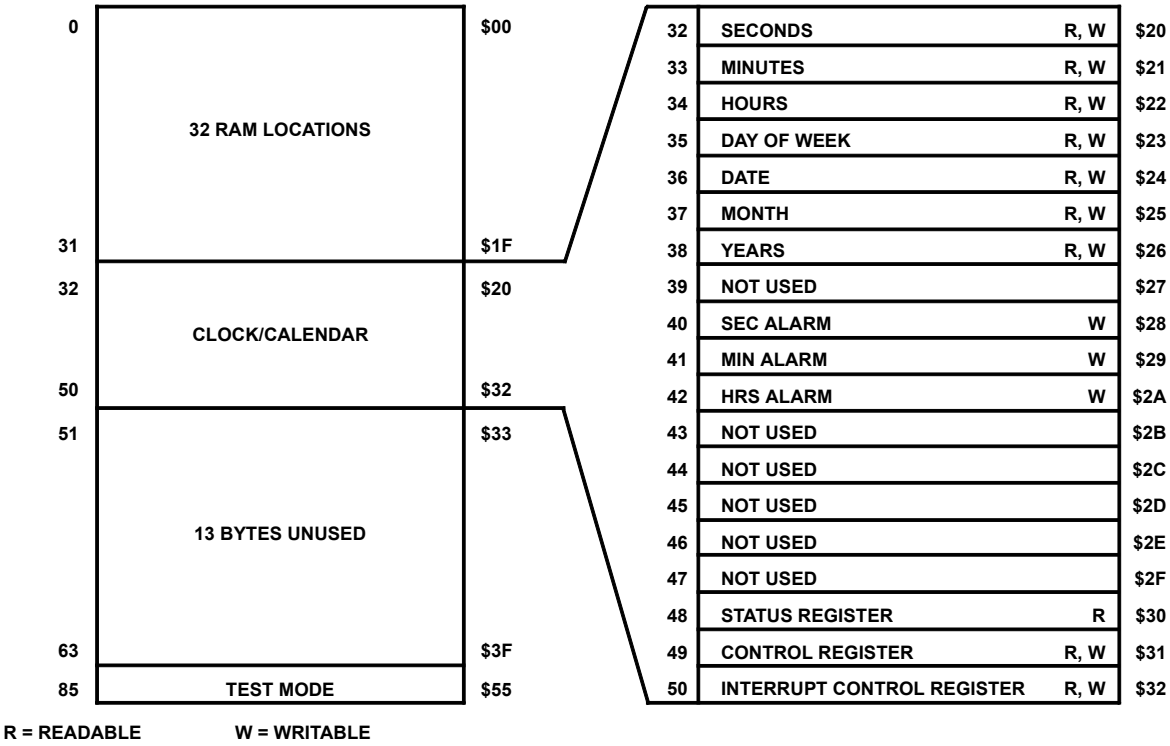


FIGURE 2. ADDRESS MAP

TABLE 1. CLOCK/CALENDAR AND ALARM DATA MODES

ADDRESS LOCATION (H)	FUNCTION	DECIMAL RANGE	BCD DATA RANGE	(NOTE 4) BCD DATE EXAMPLE
20	Seconds	0-59	00-59	18
21	Minutes	0-59	00-59	49
22	Hours 12 Hour Mode (Note 5)	1-12	81-92 (AM) A1-B2 (PM)	A3
	Hours 24 Hour Mode	0-23	00-23	15
23	Day of the Week (Sunday = 1)	1-7	01-07	03
24	Day of the Month (Date)	1-31	01-31	29
25	Month Jan = 1, Dec = 12	1-12	01-12	10
26	Years	0-99	00-99	85
28	Alarm Seconds	0-59	00-59	18
29	Alarm Minutes	0-59	00-59	49
2A	Alarm Hours (Note 6) 12 Hour Mode	1-12	01-12 (AM) 21-32 (PM)	23
	Alarm Hours 24 Hour Mode	0-23	00-23	15

NOTES:

4. Example: 3:49:18, Tuesday. Oct. 29,1985.
5. Most significant Bit, D7, is “0” for 24 hours, and “1” for 12 hour mode. Data Bit D5 is “1” for P.M. and ‘0” for A.M. in 12 hour mode.
6. Alarm hours. Data Bit D5 is “1” for P.M. and “0” for A.M. in 12 hour mode. Data Bits D7 and D6 are DON’T CARE.

Alarm

The output of the alarm comparator is enabled when this bit is set high. When a comparison occurs between the seconds, minutes and hours time and alarm counters, the interrupt output is activated. When loading the time counters, this bit should be set low to avoid a false interrupt. This is not required when loading the alarm counters. See Pin Functions, $\overline{INT}$ for explanation of alarm delay.

Periodic Select

The value in these 4 bits will select the frequency of the periodic output. (See Table 2).

CLOCK CONTROL REGISTER (Write/Read) - Address 31H

D7	D6	D5	D4	D3	D2	D1	D0
START	LINE	XTAL SEL	XTAL SEL	50Hz	CLK OUT	CLK OUT	CLK OUT
$\overline{STOP}$	$\overline{XTAL}$	1	0	$\overline{60}$Hz	2	1	0

INTERRUPT CONTROL REGISTER (Write/Read) - Address 32H

D7	D6	D5	D4	D3	D2	D1	D0
WATCHDOG	POWER DOWN	POWER SENSE	ALARM	PERIODIC SELECT			

NOTE: All bits are reset by power-on reset.

TABLE 2. PERIODIC INTERRUPT OUTPUT

D0 - D3 VALUE	PERIODIC INTERRUPT OUTPUT FREQUENCY	FREQUENCY TIME BASE	
		XTAL	LINE
0	Disable		
1	2048Hz	X	
2	1024Hz	X	
3	512Hz	X	
4	256Hz	X	
5	128Hz	X	
6	64Hz	X	
	50 or 60Hz		X
7	32Hz	X	
8	16Hz	X	
9	8Hz	X	
10	4Hz	X	
11	2Hz	X	X
12	1Hz	X	X
13	Minute	X	X
14	Hour	X	X
15	Day	X	X

STATUS REGISTER (Read Only) - Address 30H

D7	D6	D5	D4	D3	D2	D1	D0
0	WATCHDOG	TEST MODE	FIRST TIME UP	INTERRUPT TRUE	POWER SENSE INTERRUPT	ALARM INTERRUPT	CLOCK INTERRUPT

TRUTH TABLE

MODE	SIGNAL			
	CE	**SCK** (Note 9)	**MOSI**	**MISO**
DISABLE RESET	L	INPUT DISABLED	INPUT DISABLED	HIGH Z
WRITE	H	CPOL = 1  CPOL = 0	DATA BIT LATCH	HIGH Z
READ	H	CPOL = 1  CPOL = 0	X	NEXT DATA BIT SHIFTED OUT (Note 10)

NOTES:

9. When interfacing to CDP68HC05 microcontrollers, serial clock phase bit, CPHA, must be set = 1 in the microcomputer's Control Register.
10. MISO remains at a high Z until 8-bits of data are ready to be shifted out during a READ. It remains at a high Z during the entire WRITE cycle.

WATCHDOG

If this bit is set high, the watchdog circuit has detected a CPU failure.

TEST MODE

When this bit is set high, the device is in the TEST MODE.

FIRST-TIME UP

Power-on reset sets this bit high. This signifies that data in the RAM and Clock is not valid and should be initialized.

INTERRUPT TRUE

A high in this bit signifies that one of the three interrupts (Power Sense, Alarm, and Clock) is valid.

POWER-SENSE INTERRUPT

This bit set high signifies that the power-sense circuit has generated an interrupt.

ALARM INTERRUPT

When the seconds, minutes and hours time and alarm counter are equal, this bit will be set high. Status Register must be read before loading Interrupt Control Register for valid alarm indication after alarm activates.

CLOCK INTERRUPT

A periodic interrupt will set this bit high.

All bits are reset by a power-on reset except the "FIRST-TIME UP" which is set. All bits except the power-sense bit are reset after a read of this register.

Pin Signal Description

SCK (Serial Clock Input, Note 11)

This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

MOSI (Master Out/Slave In, Note 11)

Data bytes are shifted in at this pin, most significant bit (MSB) first.

MISO (Master In/Slave Out)

Data bytes are shifted out at this pin, most significant bit (MSB) first.

CE (Chip Enable, Note 12)

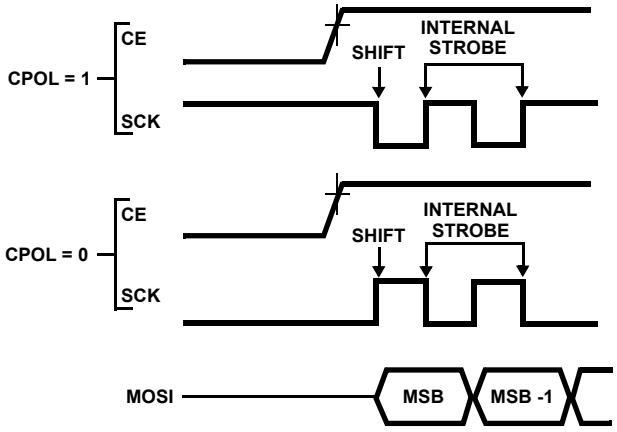
A positive chip-enable input. A low level at this input holds the serial interface logic in a reset state, and disables the output driver at the MISO pin.

NOTES:

11. These inputs will retain their previous state if the line driving them goes into a High-Z state.
12. The CE input has as internal pull down device, if the input is in a low state before going to High Z, the input can be left in a High Z.

Functional Description

The Serial Peripheral Interface (SPI) utilized by the CDP68HC68T1 is a serial synchronous bus for address and data transfers. The clock, which is generated by the microcomputer is active only during address and data transfers. In systems using the CDP68HC05C4 or CDP68HC05D2, the inactive clock polarity is determined by the CPOL bit in the microcomputer's Control Register. A unique feature of the CDP68HC68T1 is that it automatically determines the level of the inactive clock by sampling SCK when CE becomes active (see Figure 8). Input data (MOSI) is latched internally on the internal strobe edge and output data (MISO) is shifted out on the shift edge, as defined by Figure 8. There is one clock for each data bit transferred (address, as well as data bits are transferred in groups of 8).



NOTE: "CPOL" is a bit that is set in the microcomputer's Control Register.

FIGURE 8. SERIAL RAM CLOCK (SCK) AS A FUNCTION OF MCU CLOCK POLARITY (CPOL)

Address And Data Format

There are three types of serial transfer:

1. Address Control - Figure 9.
2. READ or WRITE Data - Figure 10.
3. Watchdog Reset (actually a non-transfer) Figure 11.

The Address/Control and Data bytes are shifted MSB first, Into the serial data input (MOSI) and out of the serial data output (MISO).

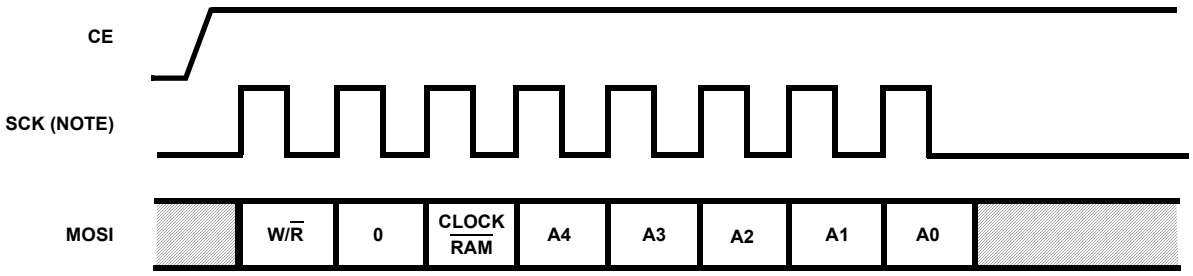
Any transfer of data requires an Address/Control byte to specify a Write or Read operation and to select a Clock or RAM location, followed by one or more bytes of data.

Data is transferred out of MISO for a Read and into MOSI for a Write operation.

Address/Control Byte - Figure 9

It is always the first byte received after CE goes true. To transmit a new address, CE must first go false and then true again. Bit 5 is used to select between Clock and RAM locations.

BIT → 7		6	5	4	3	2	1	0
↓	W/$\overline{R}$	0	CLK $\overline{RAM}$	A4	A3	A2	A1	A0
04		A0-A4		Selects 5-Bit HEX Address of RAM or specifies Clock Register. Most Significant Address Bit. If equal to "1", A0 through A4 selects a Clock Register. If equal to "0", A0 through A4 selects one of 32 RAM locations. Must be set to "0" when not in Test Mode 7W/R W/R = "1" initiates one or more WRITE cycles.W/R = "0", initiates one or more READ cycles.				
5		CLK $\overline{RAM}$						
6		0						
7		W/R						

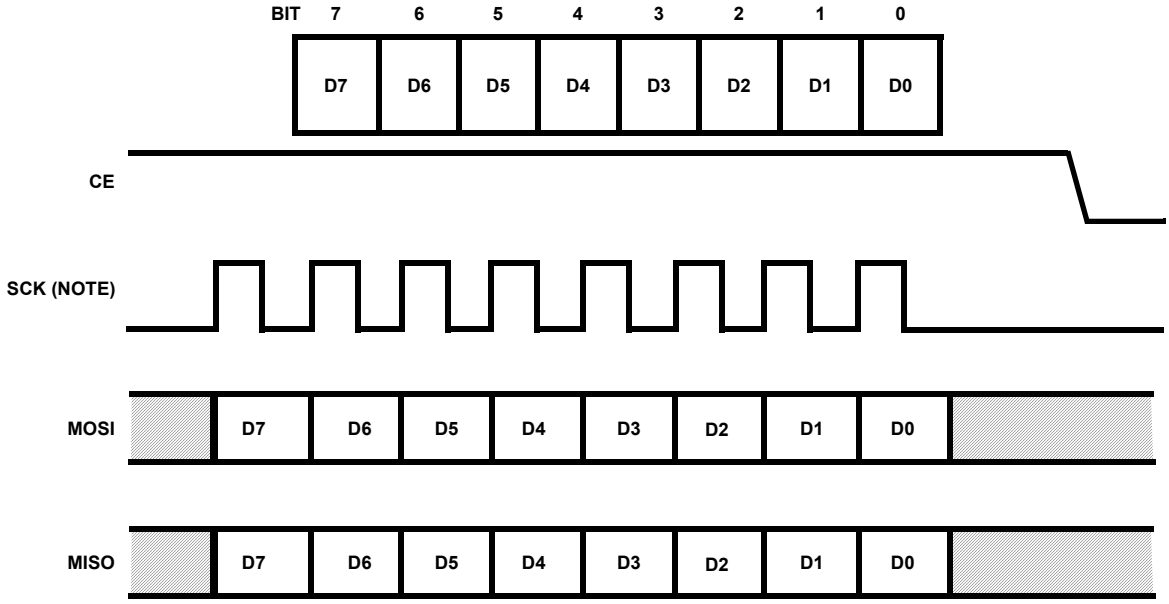


NOTE: SCK can be either polarity.

FIGURE 9. ADDRESS/CONTROL BYTE-TRANSFER WAVEFORMS

Read/Write Data (See Figure 10)

Read/Write data follows the Address/Control byte.



NOTE: SCK can be either polarity.

FIGURE 10. READ/WRITE DATA TRANSFER WAVEFORMS

Watchdog Reset (See Figure 11)

When watchdog operation is selected, CE must be toggled periodically or a CPU reset will be outputted.

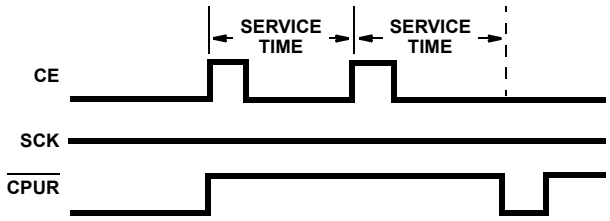


FIGURE 11. WATCHDOG OPERATION WAVEFORMS

Address And Data

Data transfers can occur one byte at a time (Figure 12) or in a multibyte burst mode (Figure 13). After the Real-Time Clock enabled, an Address/Control word is sent to set the CLOCK or RAM and select the type of operation (i.e., Read or Write). For a single-byte Read or Write, one byte is transferred to or from the Clock Register or RAM location specified in the Address/Control byte and the Real-Time Clock is then disabled. Write cycle causes the latched Clock Register or RAM address to automatically increment. Incrementing continues after each transfer until the device is disabled. After incrementing to 1FH the address will “wrap” to 00H and continue. Therefore, when the RAM is selected the address will “wrap” to 00H and when the clock is selected the address will “wrap” 20H.

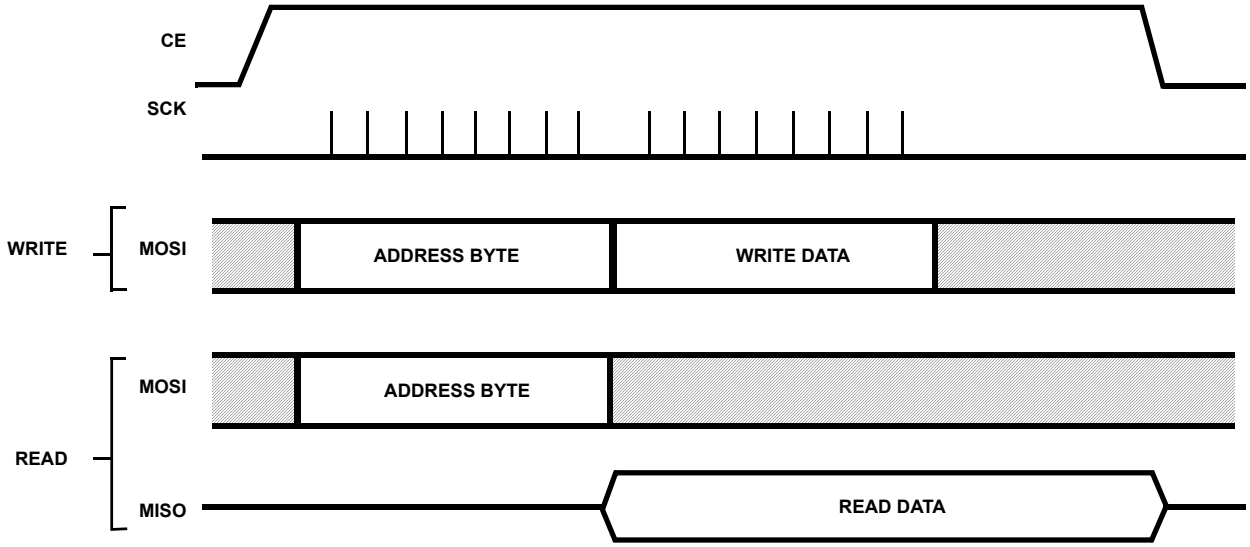


FIGURE 12. SINGLE-BYTE TRANSFER WAVEFORMS

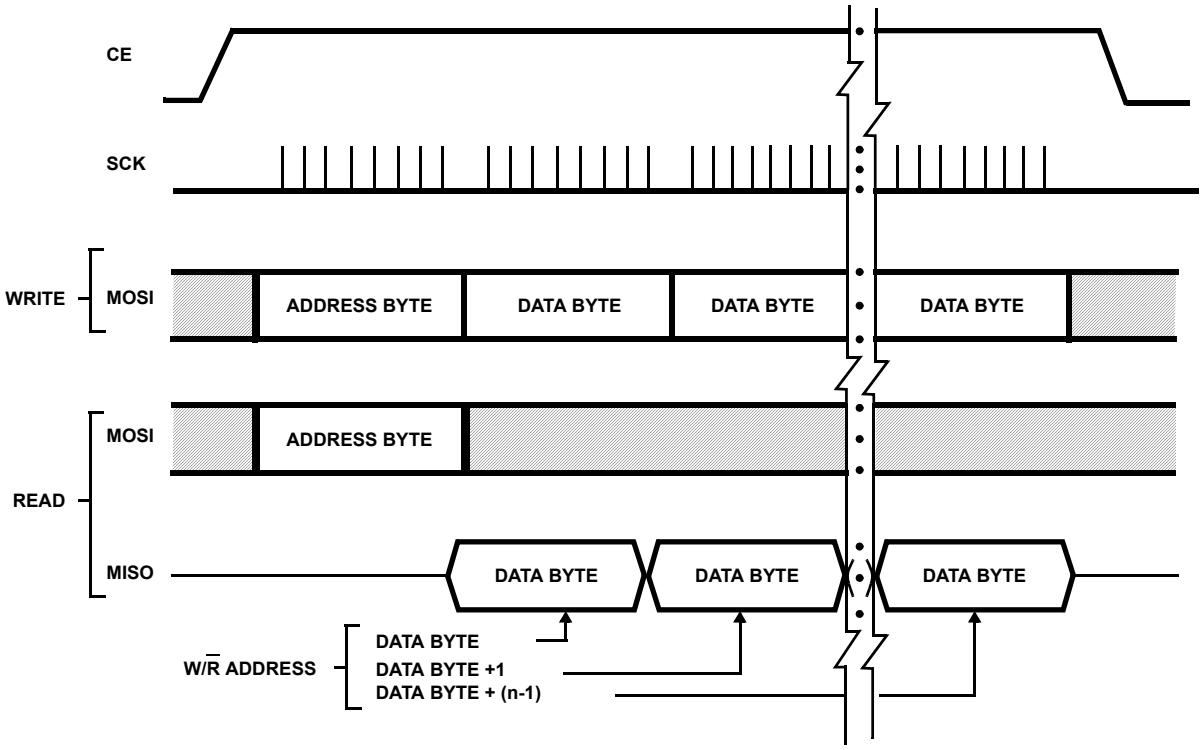


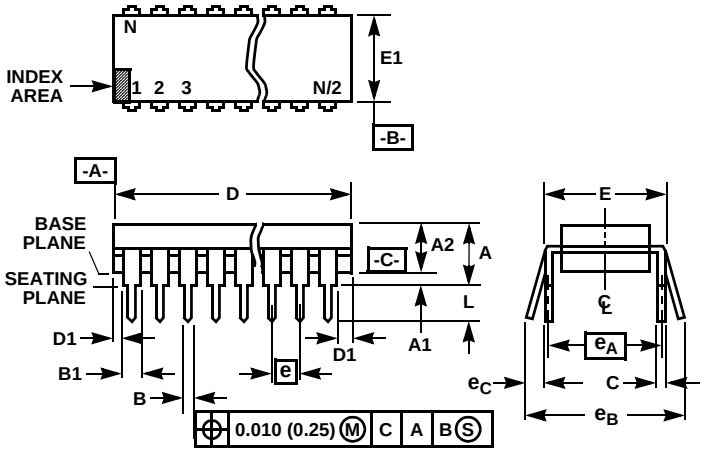
FIGURE 13. MULTIPLE-BYTE TRANSFER WAVEFORMS

Dynamic Electrical Specifications

Bus Timing V_{DD} ±10%, V_{SS} = 0V_{DC}, T_A = 40°C to 85°C

IDENT. NO	PARAMETER	LIMITS (ALL TYPES)				UNITS
		V_{DD} = 3.3V		V_{DD} = 5V		
		MIN	MAX	MIN	MAX	
1	Chip Enable Setup $Timet_{EVCV}$	200	-	100	-	ns
2	Chip Enable After Clock Hold $Timet_{CVEX}$	250	-	125	-	ns
3	Clock Width $Hight_{WH}$	400	-	200	-	ns
4	Clock Width $Lowt_{WL}$	400	-	200	-	ns
5	Data In to Clock Setup $Timet_{DVCV}$	200	-	100	-	ns
7	Clock to Data Propagation $Delayt_{CVDV}$	-	200	-	100	ns
8	Chip Disable to Output High Zt_{EXQZ}	-	200	-	100	ns
11	Output Rise $Timet_r$	-	200	-	100	ns
12	Output Fall $Timet_f$	-	200	-	100	ns
A	Data in After Clock Hold $Timet_{CVDX}$	200	-	100	-	ns
B	Clock to Data Out $Activet_{CVQX}$	-	200	-	100	ns
C	Clock Recovery $Timet_{REC}$	200	-	200	-	ns

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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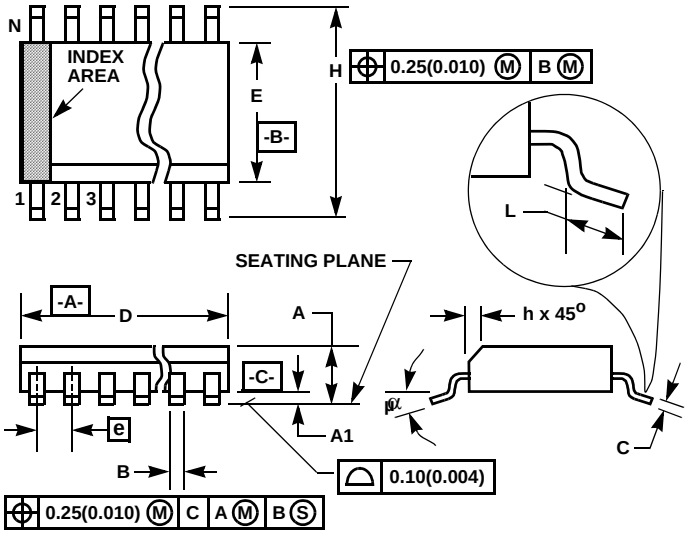
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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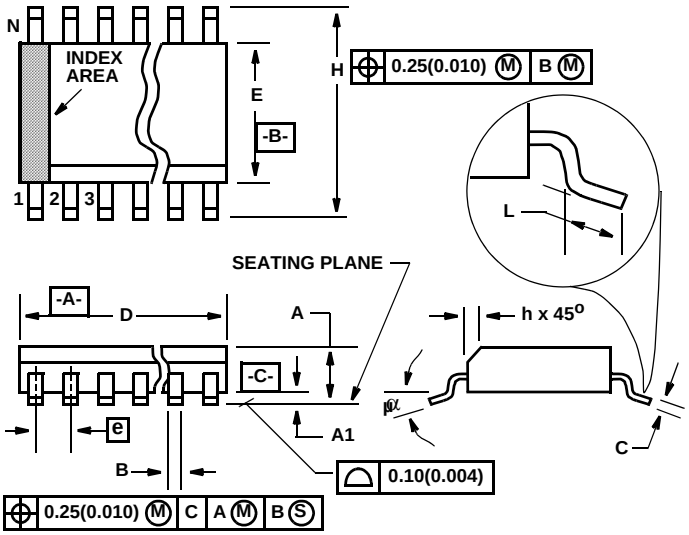
Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.