- **Recommended Applications:**
  - **DDR Memory Modules (DDR400/333/266/200)**
  - **Zero Delay Fan-Out Buffer**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 60 MHz to 220 MHz**
- **Low Jitter (Cycle-Cycle): ±35 ps**
- **Low Static Phase Offset: ±50 ps**
- **Low Jitter (Period): ±30 ps**
- **1-To-10 Differential Clock Distribution (SSTL2)**
- **Best in Class for $V_{OX} = V_{DD}/2$ ±0.1 V**
- **Operates From Dual 2.6-V or 2.5-V Supplies**
- **Available in a 40-Pin MLF Package, 48-Pin TSSOP Package, 56-Ball MicroStar Junior™ BGA Package**
- **Consumes < 100-µA Quiescent Current**
- **External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks**
- **Meets/Exceeds JEDEC Standard (JESD82−1) For DDRI-200/266/333 Specification**
- **Meets/Exceeds Proposed DDRI-400 Specification (JESD82−1A)**
- **Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low**

description

The CDCVF857 is a high-performance, low-skew, low-jitter, zero-delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to 10 differential pairs of clock outputs (Y[0:9], $\overline{\text{Y[0:9]}}$) and one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AV_{DD}). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a >20-MHz input signal, this detection circuit turns the PLL on and enables the outputs.

When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes. The CDCVF857 is also able to track spread spectrum clocking for reduced EMI.

Because the CDCVF857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCVF857 is characterized for both commercial and industrial temperature ranges.

AVAILABLE OPTIONS

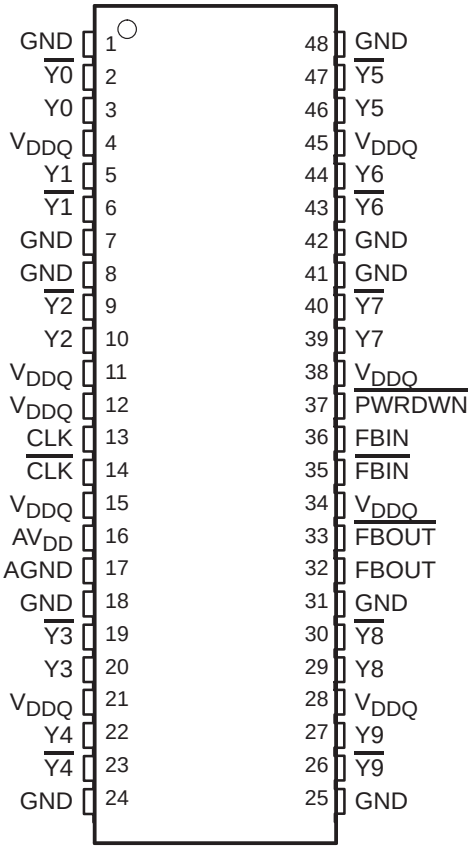
T_A	TSSOP (DGG)	40-Pin MLF	56-Ball BGA †
−40°C to 85°C	CDCVF857DGG	CDCVF857RTB	CDCVF857GQL

† Maximum load recommended is 12 pf for 200 MHz. At 12-pf load, maximum T_A allowed is 70°C.

FUNCTION TABLE
(Select Functions)

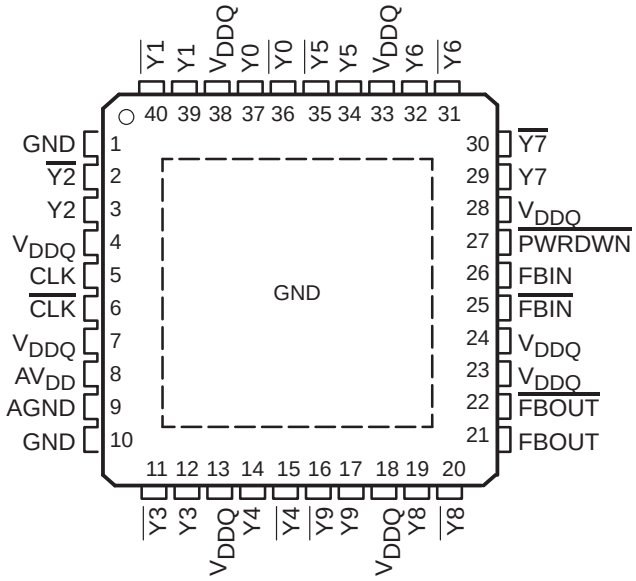
INPUTS				OUTPUTS				PLL
AV_{DD}	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y[0:9]	$\overline{Y[0:9]}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

DGG PACKAGE
(TOP VIEW)



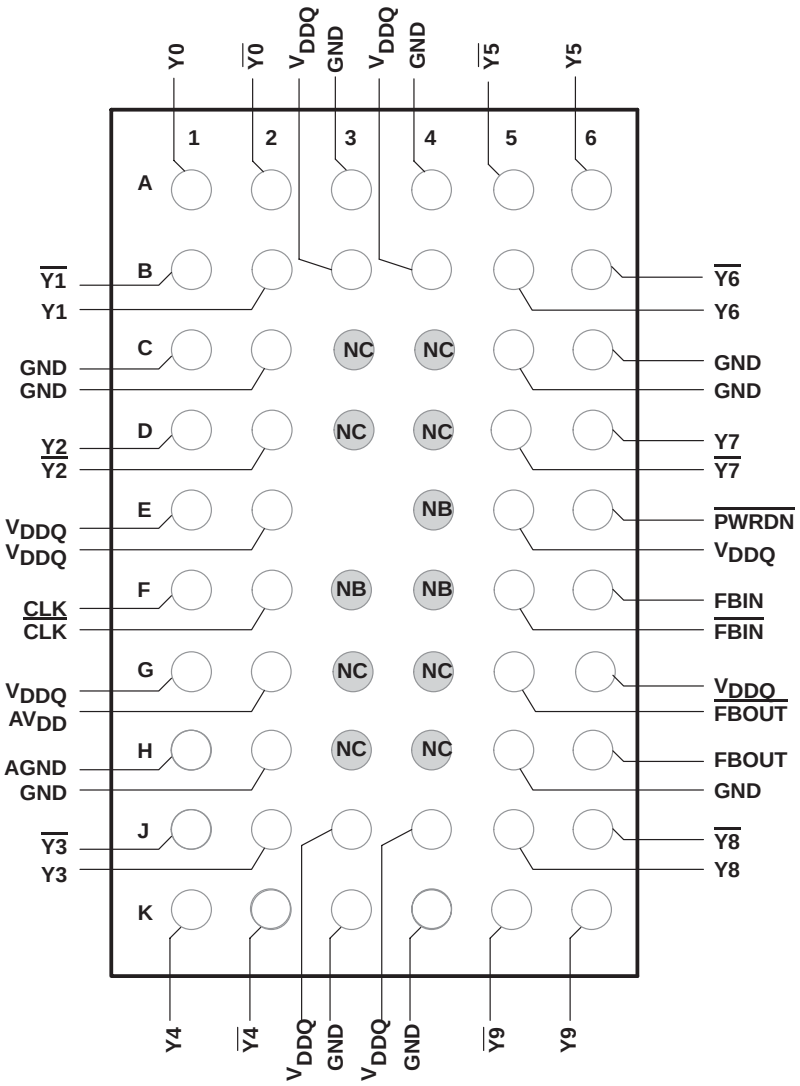
48-pin TSSOP (MO-153-ED)

RTB PACKAGE
(TOP VIEW)



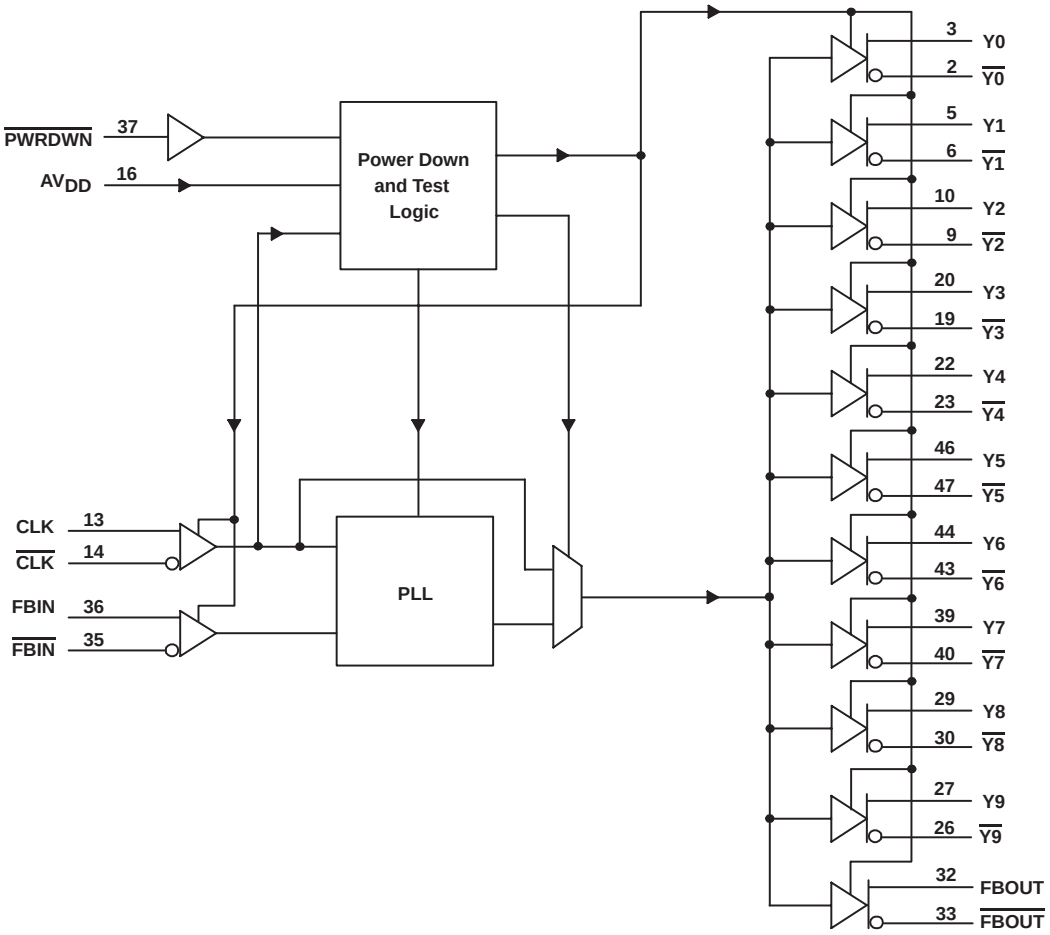
40-pin HP-VFQFP-N (6,0 x 6,0-mm Body Size,
0,5-mm Pitch, M0#220, Variation VJJD-2,
E2 = D2 = 2,9 mm ± 0,15 mm) Package Pinouts

MicroStar™ Junior (GQL) Package
(TOP VIEW)



NB = No ball
NC = No connection

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL DGG	TERMINAL RTB	TERMINAL GQL		DESCRIPTION
AGND	17	9	H1		Ground for 2.5-V analog supply
AV_{DD}	16	8	G2		2.5-V analog supply
CLK, $\overline{CLK}$	13, 14	5, 6	F1, F2	I	Differential clock input
$\overline{FBIN}$, FBIN	35, 36	25, 26	F5, F6	I	Feedback differential clock input
FBOUT, $\overline{FBOUT}$	32, 33	21, 22	H6, G5	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	1, 10	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4		Ground
$\overline{PWRDWN}$	37	27	E6	I	Output enable for Y and $\overline{Y}$
V_{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45	4, 7, 13, 18, 23, 24, 28, 33, 38	B3, B4, E1, E2, E5, G1, G6, J3, J4		2.5-V supply
Y0, $\overline{Y0}$	3, 2	37, 36	A1, A2	O	Buffered output copies of input clock, CLK, $\overline{CLK}$
Y1, $\overline{Y1}$	5, 6	39, 40	B2, B1	O	
Y2, $\overline{Y2}$	10, 9	3, 2	D1, D2	O	
Y3, $\overline{Y3}$	20, 19	12,11	J2, J1	O	
Y4, $\overline{Y4}$	22, 23	14, 15	K1, K2	O	
Y5, $\overline{Y5}$	46, 47	34, 35	A6, A5	O	
Y6, $\overline{Y6}$	44, 43	32, 31	B5, B6	O	
Y7, $\overline{Y7}$	39, 40	29, 30	D6, D5	O	
Y8, $\overline{Y8}$	29, 30	19, 20	J5, J6	O	
Y9, $\overline{Y9}$	27, 26	17, 16	K6, K5	O	

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DDQ}, AV_{DD} . . . . . 0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DDQ}) . . . . . ±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50 mA
Continuous current to GND or V_{DDQ} . . . . . ±100 mA
Storage temperature range T_{stg} . . . . . –65°C to 150°C

θ_{JA} For TSSOP (DGG) Package (see Note 3)			θ_{JA} For MLF Package		θ_{JA} For GQL Package (see Note 4)	
Airflow	**Low K**	**High K**	**Airflow**	**With 4 Thermal Vias**	**Airflow**	**High K**
0 ft/min	89.1°C/W	70°C/W	0 ft/min	44.7°C/W	0 ft/min	132.2°C/W
150 ft/min	78.5°C/W	65.3°C/W	150 ft/min		150 ft/min	126.4°C/W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.
4. Connecting the NC-balls (C3, C4, D3, D4, G3, G4, H3, H4) to a ground plane improves the θ_{JA} to 114.8°C/W (0 airflow).

recommended operating conditions (see Note 5)

			MIN	TYP	MAX	UNIT
Supply voltage	V_{DDQ}	PC1600 − PC3200	2.3		2.7	V
	AV_{DD}		V_{DDQ} − 0.12		2.7	
Low-level input voltage, V_{IL}	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$				$V_{DDQ}/2$ – 0.18	V
	$\overline{PWRDWN}$		−0.3		0.7	
High-level input voltage, V_{IH}	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$		$V_{DDQ}/2$ + 0.18			V
	$\overline{PWRDWN}$		1.7		V_{DDQ} + 0.3	
DC input signal voltage (see Note 5)			–0.3		V_{DDQ} + 0.3	V
Differential input signal voltage, V_{ID} (see Note 6)	dc	CLK, FBIN	0.36		V_{DDQ} + 0.6	V
	ac	CLK, FBIN	0.7		V_{DDQ} + 0.6	
Input differential pair cross voltage, V_{IX} (see Notes 7 and 8)			$V_{DDQ}/2$ – 0.2		$V_{DDQ}/2$ + 0.2	V
High-level output current, I_{OH}					−12	mA
Low-level output current, I_{OL}					12	mA
Input slew rate, SR			1		4	V/ns
Operating free-air temperature, T_A			−40		85	°C

NOTES: 5. The unused inputs must be held high or low to prevent them from floating.
6. The dc input signal voltage specifies the allowable dc execution of the differential input.
7. The differential input signal voltage specifies the differential voltage |VTR − VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
8. The differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must be crossing.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input voltage	All inputs	V_{DDQ} = 2.3 V, I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage		V_{DDQ} = min to max, I_{OH} = –1 mA	V_{DDQ} – 0.1			V
			V_{DDQ} = 2.3 V, I_{OH} = –12 mA	1.7			
V_{OL}	Low-level output voltage		V_{DDQ} = min to max, I_{OL} = 1 mA			0.1	V
			V_{DDQ} = 2.3 V, I_{OL} = 12 mA			0.6	
V_{OD}	Output voltage swing‡		Differential outputs are terminated with 120 Ω /C_L = 14 pF (See Figure 3)	1.1		V_{DDQ} – 0.4	V
V_{OX}	Output differential cross-voltage§			$V_{DDQ}/2$ – 0.1	$V_{DDQ}/2$	$V_{DDQ}/2$ + 0.1	
I_I	Input current		V_{DDQ} = 2.7 V, V_I = 0 V to 2.7 V			±10	µA
I_{OZ}	High-impedance state output current		V_{DDQ} = 2.7 V, V_O= V_{DDQ} or GND			±10	µA
I_{DDPD}	Power-down current on V_{DDQ} + AV_{DD}		CLK and $\overline{CLK}$ = 0 MHz; $\overline{PWRDWN}$ = Low; Σ of I_{DD} and AI_{DD}		20	100	µA
AI_{DD}	Supply current on AV_{DD}		f_O = 170 MHz		6	8	mA
			f_O = 200 MHz		8	10	
C_I	Input capacitance		V_{DDQ} = 2.5 V, V_I = V_{DDQ} or GND	2	2.5	3.5	pF

† All typical values are at a respective nominal V_{DDQ}.
‡ The differential output signal voltage specifies the differential voltage |VTR − VCP|, where VTR is the true output level and VCP is the complementary output level.
§ The differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{DD}	Dynamic current on V_{DDQ}	Without load	f_O = 170 MHz		120	140	mA
			f_O = 200 MHz		125	150	
		Differential outputs terminated with 120 Ω/C_L = 0 pF	f_O = 170 MHz		220	270	
			f_O = 200 MHz		230	280	
		Differential outputs terminated with 120 Ω/C_L = 14 pF	f_O = 170 MHz		280	330	
			f_O = 200 MHz		300	350	
ΔC	Part-to-part input capacitance variation	V_{DDQ} = 2.5 V, V_I = V_{DDQ} or GND				1	pF
$C_{I(Δ)}$	Input capacitance difference between CLK and CKB, FBIN, and FBINB	V_{DDQ} = 2.5 V, V_I = V_{DDQ} or GND				0.25	pF

† All typical values are at a respective nominal V_{DDQ}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f_{CLK}	Operating clock frequency	60	220	MHz
	Application clock frequency	90	220	
	Input clock duty cycle	40%	60%	
	Stabilization time† (PLL mode)		10	µs
	Stabilization time‡ (bypass mode)		30	ns

† The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V_{DD} must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

‡ A recovery time is required when the device goes from power-down mode into bypass mode (AVDD at GND).

switching characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}§	Low-to-high level propagation delay time	Test mode/CLK to any output			3.5		ns
t_{PHL}§	High-to-low level propagation delay time	Test mode/CLK to any output			3.5		ns
$t_{jit(per)}$¶	Jitter (period), See Figure 7	100 MHz (PC1600)		−65		65	ps
		133/167/200 MHz (PC2100/2700/3200)		−30		30	
$t_{jit(cc)}$¶	Jitter (cycle-to-cycle), See Figure 4	100 MHz (PC1600)		−50		50	ps
		133/167/200 MHz (PC2100/2700/3200)		−35		35	
$t_{jit(hper)}$¶	Half-period jitter, See Figure 8	100 MHz (PC1600)		−100		100	ps
		133/167/200 MHz (PC2100/2700/3200)		−75		75	
$t_{slr(o)}$	Output clock slew rate, See Figure 9	Load: 120 Ω/14 pF		1		2	V/ns
$t_{(Ø)}$	Static phase offset, See Figure 5	100/133/167/200 MHz		–50		50	ps
$tsk_{(o)}$	Output skew, See Figure 6	Load: 120 Ω/14 pF	100/133/167/200 MHz			40	ps

§ Refers to the transition of the noninverting output.

¶ This parameter is assured by design but can not be 100% production tested.

PARAMETER MEASUREMENT INFORMATION

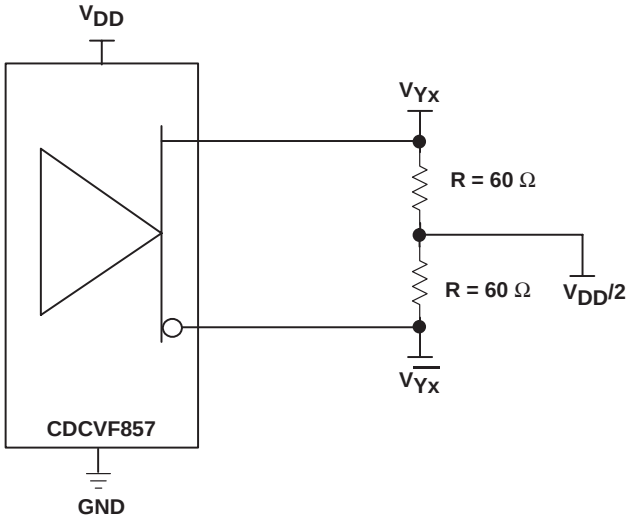


Figure 1. IBIS Model Output Load

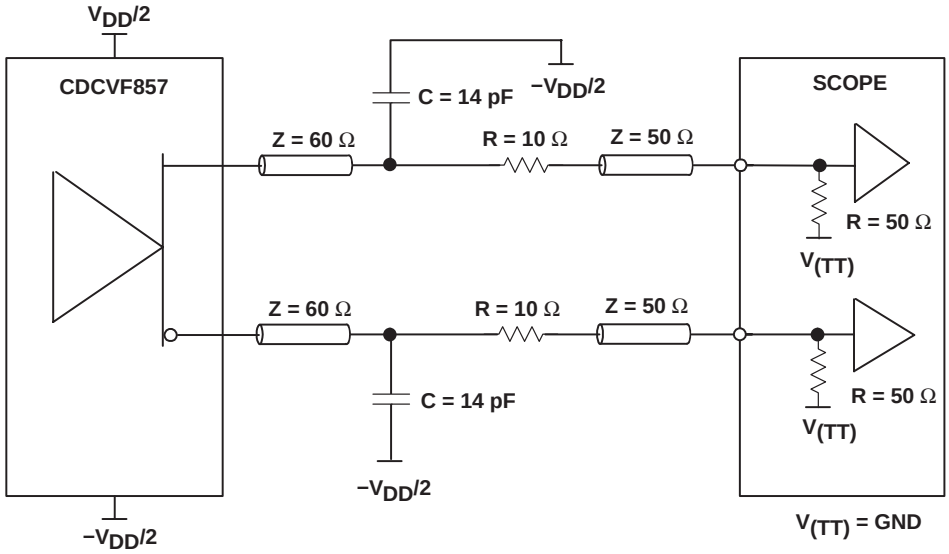


Figure 2. Output Load Test Circuit

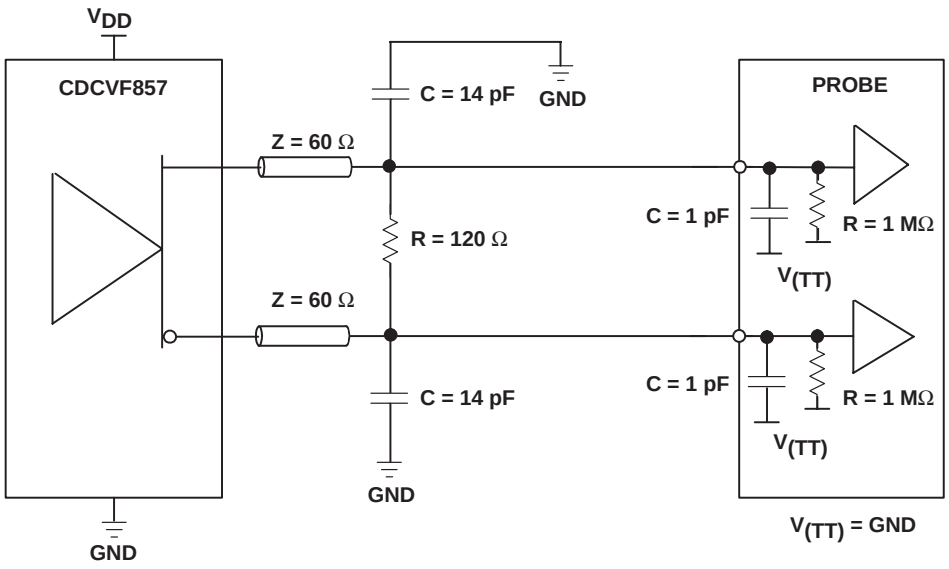
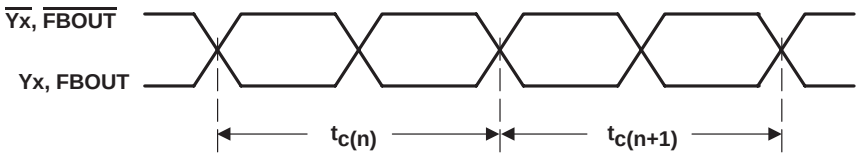


Figure 3. Output Load Test Circuit for Crossing Point



$t_{jit(cc)} = t_{c(n)} - t_{c(n+1)}$

Figure 4. Cycle-to-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION

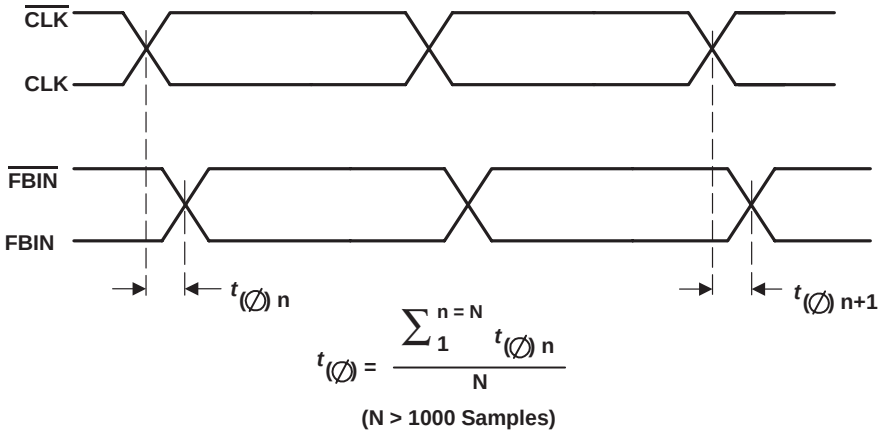


Figure 5. Phase Offset

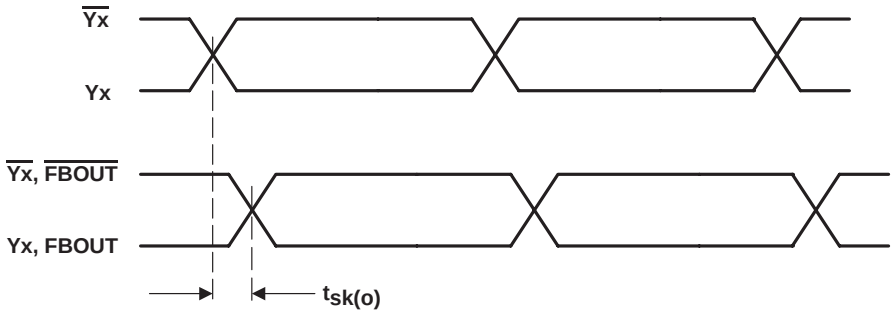
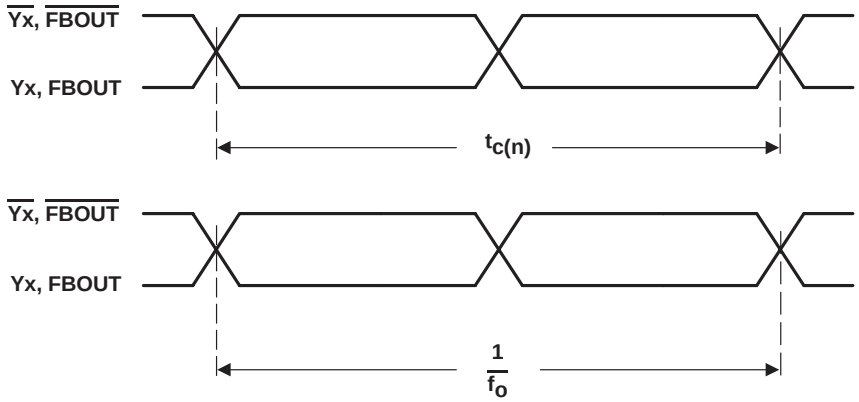


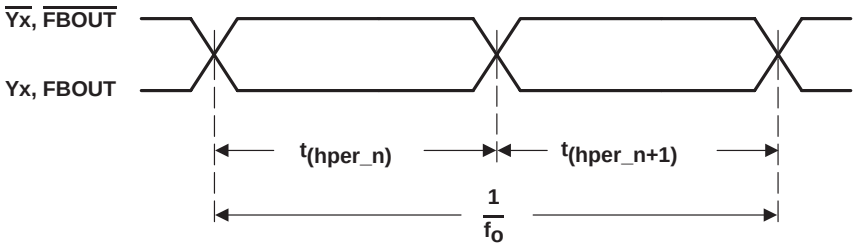
Figure 6. Output Skew

PARAMETER MEASUREMENT INFORMATION



$t_{jit(per)} = t_{cn} - \frac{1}{f_o}$ f_O = Average input frequency measured at CLK/$\overline{CLK}$

Figure 7. Period Jitter



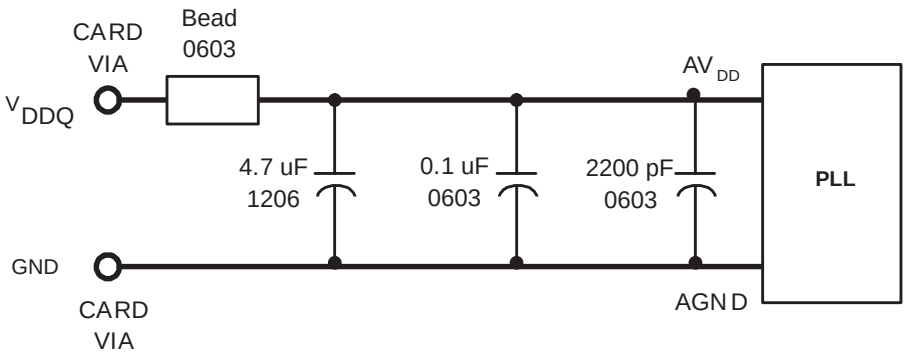
$t_{jit(hper)} = t_{(hper\_n)} - \frac{1}{2xf_o}$ n = any half cycle

f_O = Average input frequency measured at CLK/$\overline{CLK}$

Figure 8. Half-Period Jitter

$t_{slr(I/O)} = \frac{V_{80\%} - V_{20\%}}{t_{r(I/O)}}$ $t_{slf(I/O)} = \frac{V_{80\%} - V_{20\%}}{t_{f(I/O)}}$

Figure 9. Input and Output Slew Rates



See Notes 9, 10, and 11

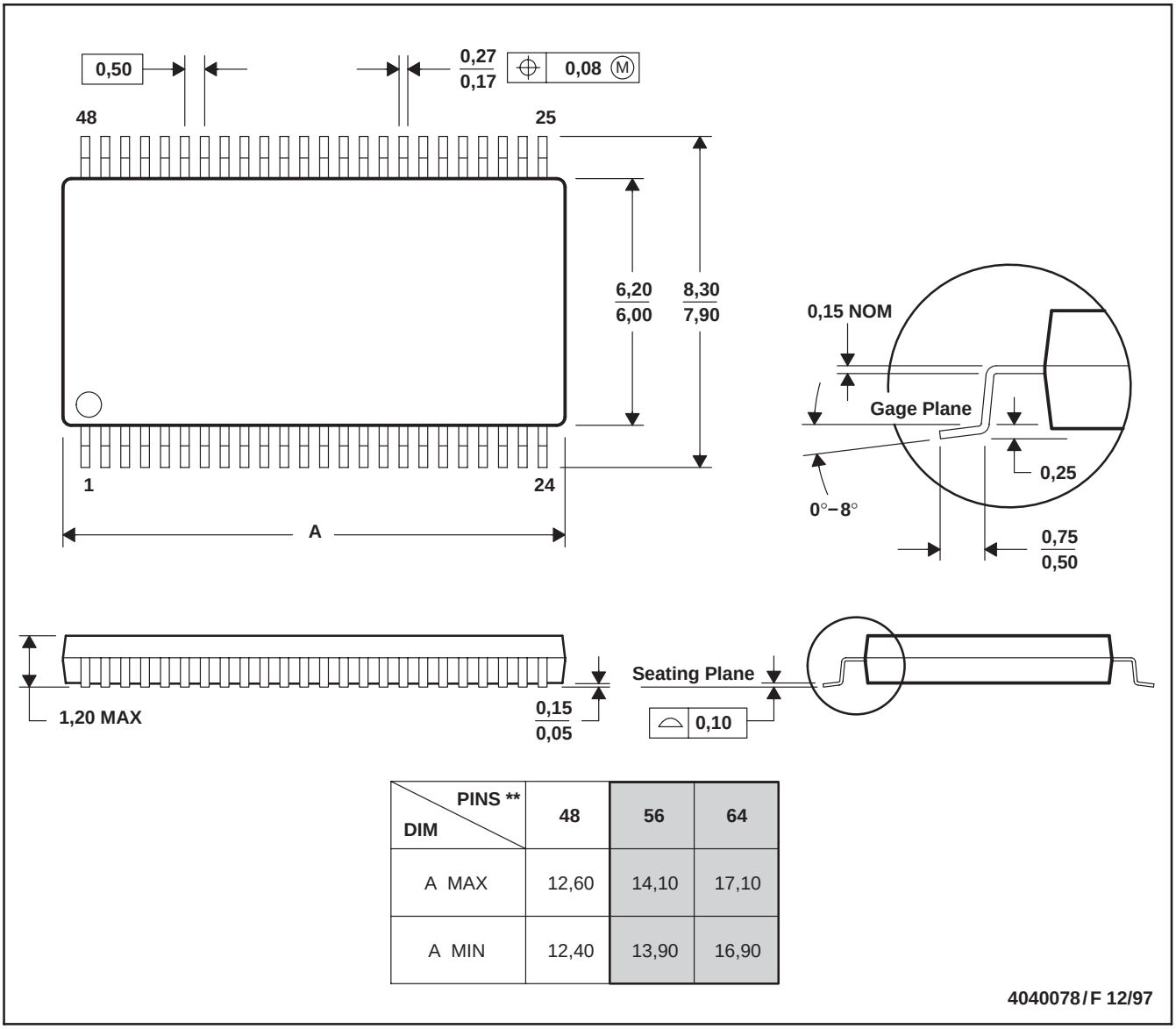
Figure 10. Recommended AV_{DD} Filtering

NOTES: 9. Place the 2200-pF capacitor close to the PLL.
10. Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).
11. Recommended bead: Fair-Rite P/N 2506036017Y0 or equilvalent (0.8 Ω dc maximum, 600 Ω at 100 MHz).

MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



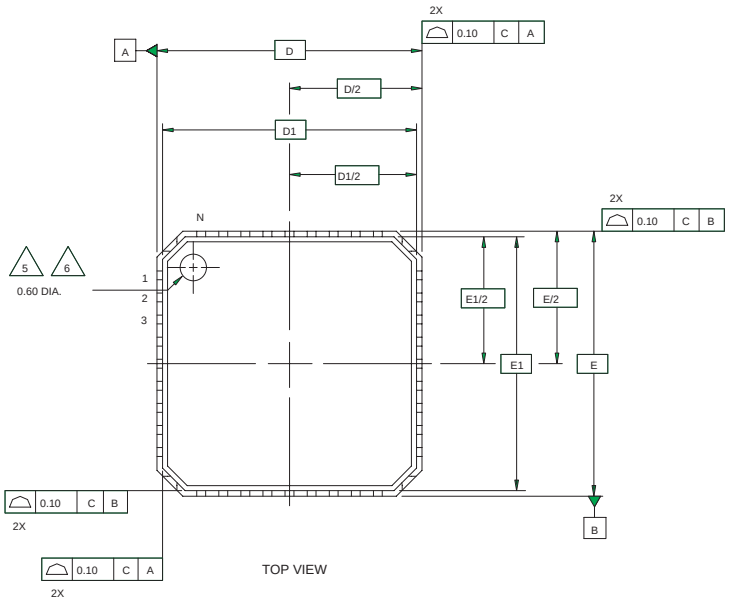
DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

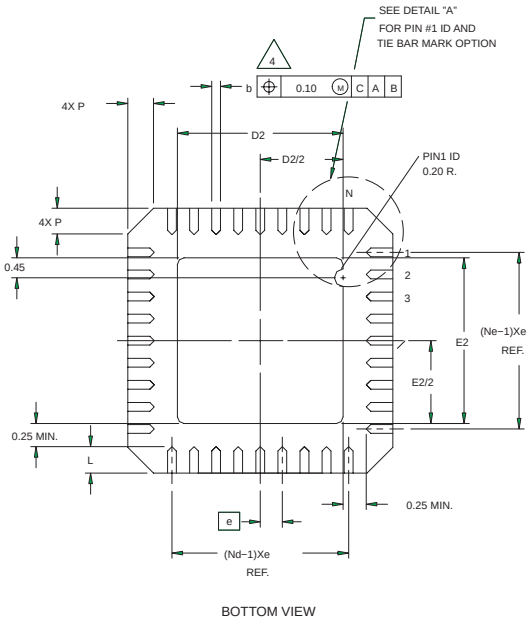
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

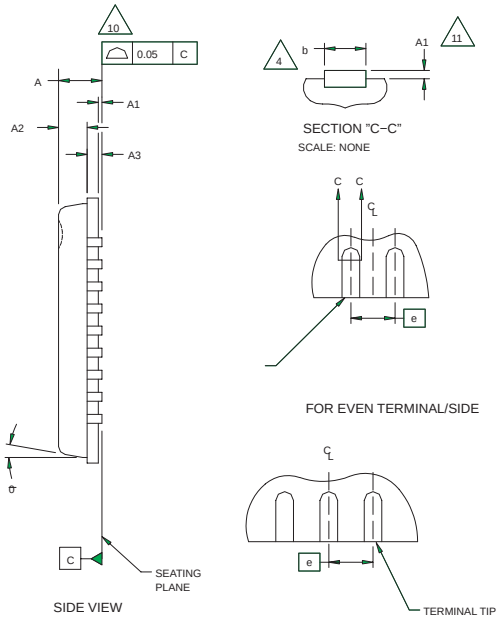
MECHANICAL DATA

RTB (MLF2-N40)

HIGH-DENSITY MATRIX LEADFRAME







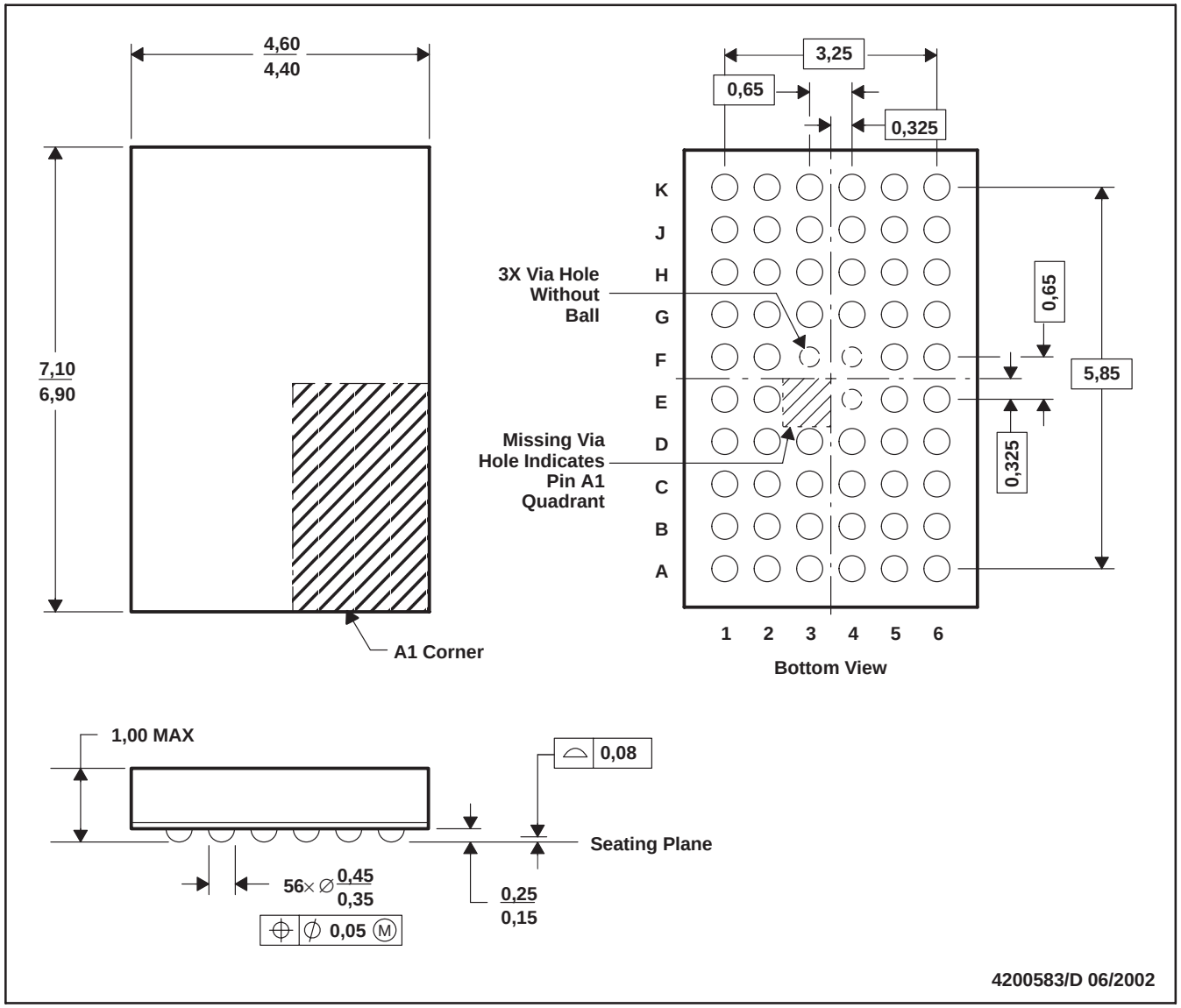
SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	0.90	
A1	0.00	0.01	0.05	D
A2	–	0.65	0.80	
A3		0.20 REF.		
D		6.00 BSC		
D1		5.75 BSC		
E		6.00 BSC		
E1		5.75 BSC		
θ			12	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	C

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		40		A
Nd		10		A
Ne		10		A
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	B
Q	0.00	0.20	0.45	C
D2	2.75	2.90	3.05	
E2	2.75	2.90	3.05	

NOTES: A. N is the number of terminals
B. Dimension b applies to the plated terminal and is measured
C. Q and R apply only for the straight tiebar shapes.
D. Applied only for terminals
E. 40-pin HP-VFQFP-N, 6.0 × 6.0 mm body size, 0.5-mm pitch, variation VJJD-2, E2 & D2 = 2.9 mm ±0.15 mm

MECHANICAL DATA

GQL (R-PBGA-N56) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO-225 variation BA.
E. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

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