

Distributed by:

**JAMECO**<sup>®</sup>  
ELECTRONICS

**www.Jameco.com ♦ 1-800-831-4242**

The content and copyrights of the attached  
material are the property of its owner.

Jameco Part Number 825213

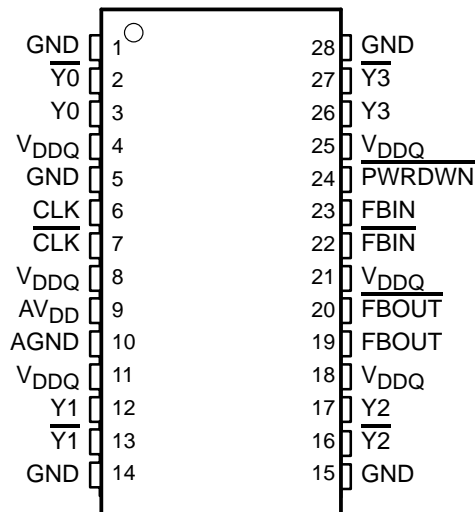
# CDCV855, CDCV855I

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

- Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 MHz to 180 MHz
- Low Jitter (cyc–cyc):  $\pm 50$  ps
- Distributes One Differential Clock Input to Four Differential Clock Outputs
- Enters Low Power Mode and Three-State Outputs When Input CLK Signal Is Less Than 20 MHz or PWRDWN Is Low
- Operates From Dual 2.5-V Supplies
- 28-Pin TSSOP Package
- Consumes < 200- $\mu$ A Quiescent Current
- External Feedback PIN (FBIN,  $\overline{\text{FBIN}}$ ) Are Used to Synchronize the Outputs to the Input Clocks

PW PACKAGE  
(TOP VIEW)



### description

The CDCV855 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to four differential pairs of clock outputs (Y[0:3],  $\overline{\text{Y}}[0:3]$ ) and one differential pair of feedback clock outputs (FBOUT,  $\overline{\text{FBOUT}}$ ). When  $\overline{\text{PWRDWN}}$  is high, the outputs switch in phase and frequency with CLK. When  $\overline{\text{PWRDWN}}$  is low, all outputs are disabled to a high-impedance state (3-state), and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low-frequency condition and after applying a >20-MHz input signal this detection circuit turns on the PLL again and enables the outputs.

When  $\text{AV}_{\text{DD}}$  is tied to GND, the PLL is turned off and bypassed for test purposes. The CDCV855 is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV855 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV855 is characterized for both commercial and industrial temperature ranges.

### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES
	TSSOP (PW)
0°C to 70°C	CDCV855PW
-40°C to 85°C	CDCV855IPW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated

# CDCV855, CDCV855I

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

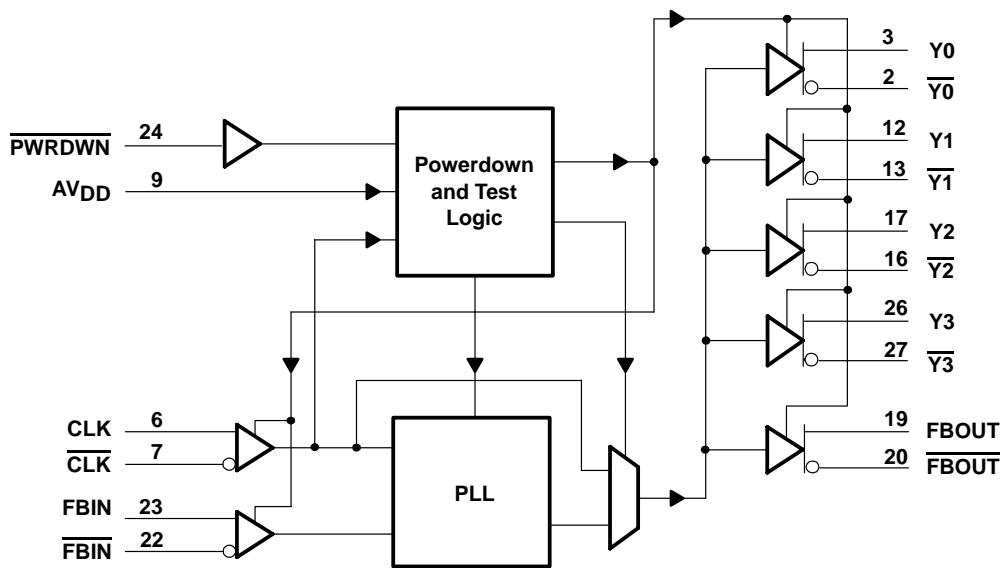
SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

**FUNCTION TABLE**  
(Select Functions)

INPUTS				OUTPUTS				PLL
AVDD	PWRDWN	CLK	CLK	Y[0:3]	Y[0:3]	FBOUT	FBOUT	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz†	<20 MHz†	Z	Z	Z	Z	Off

† Typically 10 MHz

### functional block diagram



### Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	10		Ground for 2.5-V analog supply
AVDD	9		2.5-V analog supply
CLK, CLK	6, 7	I	Differential clock input
FBIN, FBIN	23, 22	I	Feedback differential clock input
FBOUT, FBOUT	19, 20	O	Feedback differential clock output
GND	1, 5, 14, 15, 28		Ground
PWRDWN	24	I	Control input to turn device in the power-down mode
VDDQ	4, 8, 11, 18, 21, 25		2.5-V supply
Y[0:3]	3, 12, 17, 26	O	Buffered output copies of input clock, CLK
Y[0:3]	2, 13, 16, 27	O	Buffered output copies of input clock, CLK



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# CDCV855, CDCV855I

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{DDQ}$ , $AV_{DD}$	–0.5 V to 3.6 V
Input voltage range, $V_I$ (see Notes 1 and 2)	–0.5 V to $V_{DDQ} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{DDQ} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DDQ}$ )	±50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DDQ}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{DDQ}$ )	±50 mA
Continuous current to GND or $V_{DDQ}$	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): PW package	105.8°C/W
Storage temperature range $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This value is limited to 3.6 V maximum.
  3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 4)

		MIN	TYP	MAX	UNIT	
Supply voltage, $V_{DDQ}$ , $AV_{DD}$		2.3			2.7	V
Low-level input voltage, $V_{IL}$	CLK, $\overline{CLK}$ , FBIN, $\overline{FBIN}$	$V_{DDQ}/2 - 0.18$			V	
	$\overline{PWRDWN}$	–0.3				0.7
High-level input voltage, $V_{IH}$	CLK, $\overline{CLK}$ , FBIN, $\overline{FBIN}$	$V_{DDQ}/2 + 0.18$			V	
	$\overline{PWRDWN}$	1.7				$V_{DDQ} + 0.3$
DC input signal voltage (see Note 5)		–0.3			$V_{DDQ}$	V
Differential input signal voltage, $V_{ID}$ (see Note 6)	CLK, FBIN	0.36			$V_{DDQ} + 0.6$	V
Output differential cross-voltage, $V_{O(X)}$ (see Note 7)		$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.2$	V	
Input differential pair cross-voltage, $V_{I(X)}$ (see Note 7)		$V_{DDQ}/2 - 0.2$			$V_{DDQ}/2 + 0.2$	V
High-level output current, $I_{OH}$					–12	mA
Low-level output current, $I_{OL}$					12	mA
Input slew rate, SR (see Figure 7)		1			4	V/ns
Operating free-air temperature, $T_A$	Commercial	0			85	°C
	Industrial	–40			85	

- NOTES:
4. Unused inputs must be held high or low to prevent them from floating.
  5. DC input signal voltage specifies the allowable dc execution of differential input.
  6. Differential input signal voltage specifies the differential voltage  $|V_{TR} - V_{CP}|$  required for switching, where  $V_{TR}$  is the true input level and  $V_{CP}$  is the complementary input level.
  7. Differential cross-point voltage is expected to track variations of  $V_{DDQ}$  and is the voltage at which the differential signals must be crossing.



# CDCV855, CDCV855I

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Input voltage	All inputs V <sub>DDQ</sub> = 2.3 V, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>DDQ</sub> = min to max, I <sub>OH</sub> = -1 mA	V <sub>DDQ</sub> - 0.1			V
		V <sub>DDQ</sub> = 2.3 V, I <sub>OH</sub> = -12 mA	1.7			
V <sub>OL</sub>	Low-level output voltage	V <sub>DDQ</sub> = min to max, I <sub>OL</sub> = 1 mA			0.1	V
		V <sub>DDQ</sub> = 2.3 V, I <sub>OL</sub> = 12 mA			0.6	
I <sub>OH</sub>	High-level output current	V <sub>DDQ</sub> = 2.3 V, V <sub>O</sub> = 1 V	-18	-32		mA
I <sub>OL</sub>	Low-level output current	V <sub>DDQ</sub> = 2.3 V, V <sub>O</sub> = 1.2 V	26	35		mA
V <sub>OD</sub>	Output voltage swing	Differential outputs are terminated with 120 Ω	1.1		V <sub>DDQ</sub> - 0.4	V
V <sub>OX</sub>	Output differential cross-voltage‡		V <sub>DDQ</sub> /2 - 0.2	V <sub>DDQ</sub> /2	V <sub>DDQ</sub> /2 + 0.2	
I <sub>I</sub>	Input current	V <sub>DDQ</sub> = 2.7 V, V <sub>I</sub> = 0 V to 2.7 V			±10	μA
I <sub>OZ</sub>	High-impedance-state output current	V <sub>DDQ</sub> = 2.7 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND			±10	μA
I <sub>DD(PD)</sub>	Power-down current on V <sub>DDQ</sub> + AV <sub>DD</sub>	CLK and $\overline{\text{CLK}}$ = 0 MHz; PWRDWN = Low; Σ of I <sub>DD</sub> and AI <sub>DD</sub>		100	200	μA
I <sub>DD</sub>	Dynamic current on V <sub>DDQ</sub>	Differential outputs are terminated with 120 Ω / CL = 14 pF Differential outputs are terminated with 120 Ω / CL = 0 pF f <sub>O</sub> = 167 MHz		150	180	mA
				130	160	
AI <sub>DD</sub>	Supply current on AV <sub>DD</sub>	f <sub>O</sub> = 167 MHz		8	10	mA
C <sub>I</sub>	Input capacitance	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND	2	2.5	3	pF
C <sub>O</sub>	Output capacitance	V <sub>DDQ</sub> = 2.5 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND	2.5	3	3.5	pF

† All typical values are at respective nominal V<sub>DDQ</sub>.

‡ Differential cross-point voltage is expected to track variation of V<sub>DDQ</sub> and is the voltage at which the differential signals must be crossing.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		MIN	MAX	UNIT
f <sub>CLK</sub>	Operating clock frequency	60	180	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time (PLL mode)¶		10	μs
	Stabilization time (Bypass mode)§		30	ns

§ Recovery time required when the device goes from power-down mode into bypass mode (test mode with AV<sub>DD</sub> at GND).

¶ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.



**switching characteristics**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
$t_{PLH}^{\ddagger}$	Low-to-high level propagation delay time	Test mode/CLK to any output		4.5		ns	
$t_{PHL}^{\ddagger}$	High-to-low level propagation delay time	Test mode/CLK to any output		4.5		ns	
$t_{jit(per)}^{\S}$	Jitter (period), See Figure 5	66 MHz	-55		55	ps	
		100/133/167/180 MHz	-35		35	ps	
$t_{jit(cc)}^{\S}$	Jitter (cycle-to-cycle), See Figure 2	66 MHz	-60		60	ps	
		100/133/167/180 MHz	-50		50		
$t_{jit(hper)}^{\S}$	Half-period jitter, See Figure 6	66 MHz	-130		130	ps	
		100 MHz	-90		90		
		133/167/180 MHz	-75		75		
$t_{slr(o)}$	Output clock slew rate, See Figure 7	Load = 120Ω / 14 pF		1	2	V/ns	
		Load = 120Ω / 4 pF		1	3	V/ns	
$t_{d(\emptyset)}^{\S}$	Dynamic phase offset (this includes jitter), See Figure 3(b)	SSC off	66 MHz	-180		180	ps
			100/133 MHz	-130		130	
			167/180 MHz	-90		90	
		SSC on	66 MHz	-230		230	
			100/133 MHz	-170		170	
			167/180 MHz	-100		100	
$t_{(\emptyset)}$	Static phase offset, See Figure 3(a)	66 MHz	-150		150	ps	
		100/133/167/180 MHz	-100		100		
$tsk(o)^{\parallel}$	Output skew, See Figure 4				50	ps	
$t_r, t_f$	Output rise and fall times (20% – 80%)	Load: 120 Ω/14 pF		650	900	ps	

† All typical values are at a respective nominal  $V_{DDQ}$ .

‡ Refers to transition of noninverting output

§ This parameter is assured by design but can not be 100% production tested.

¶ All differential output pins are terminated with 120 Ω/14 pF.

# CDCV855, CDCV855I 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

## PARAMETER MEASUREMENT INFORMATION

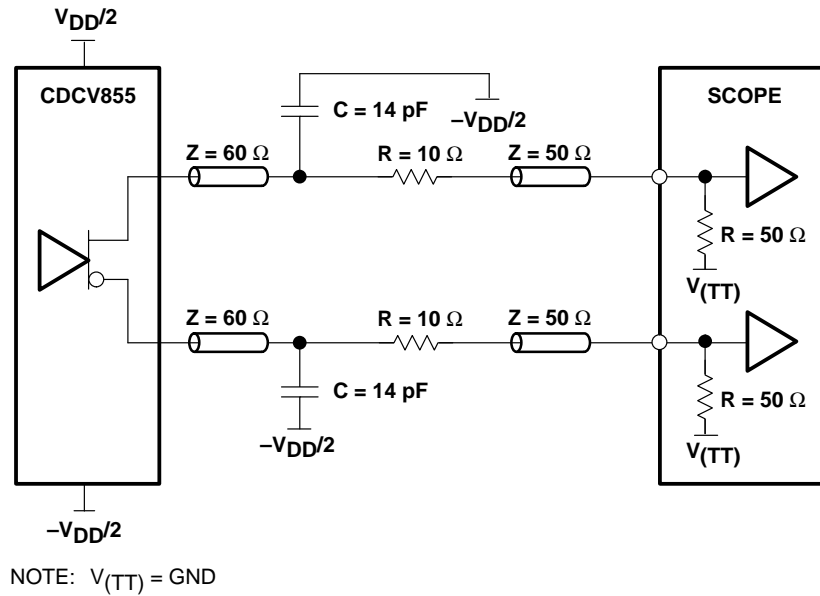


Figure 1. Output Load Test Circuit

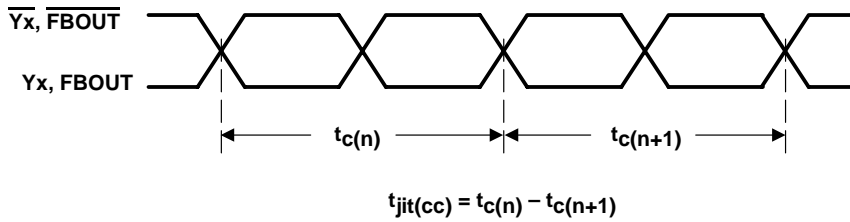


Figure 2. Cycle-to-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION

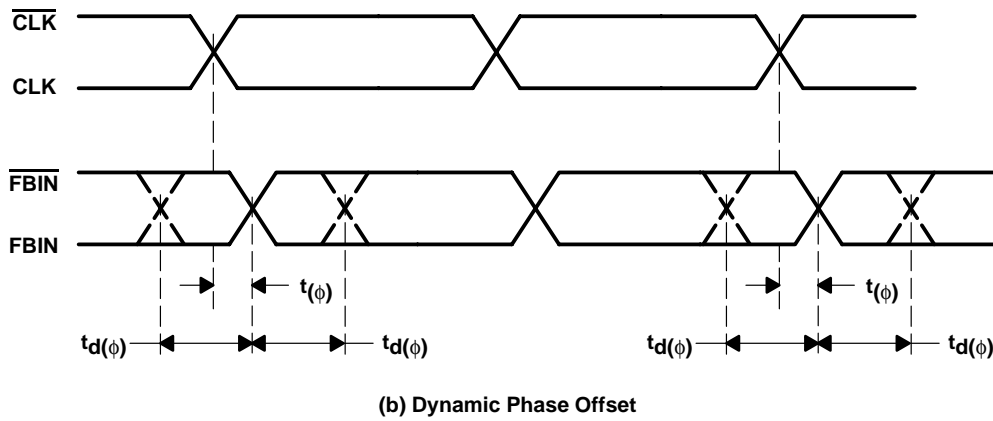
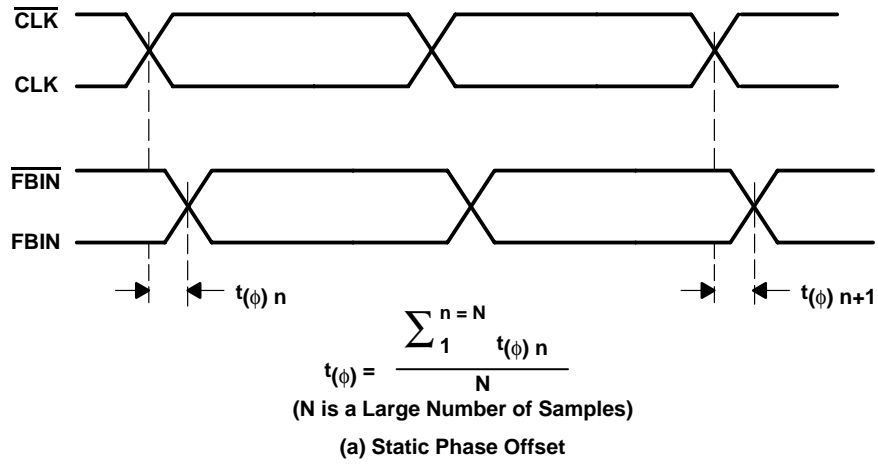


Figure 3. Phase Offset

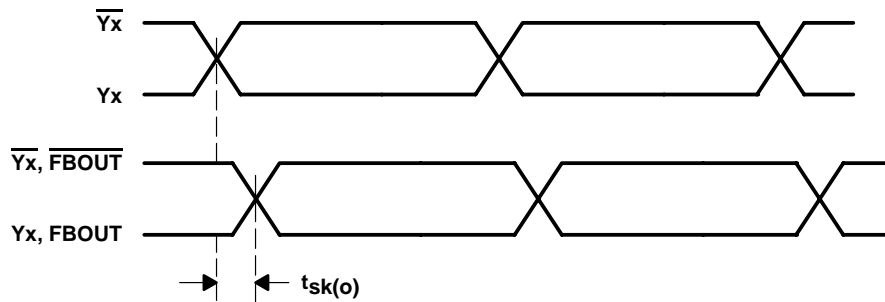


Figure 4. Output Skew

# CDCV855, CDCV855I

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

### PARAMETER MEASUREMENT INFORMATION

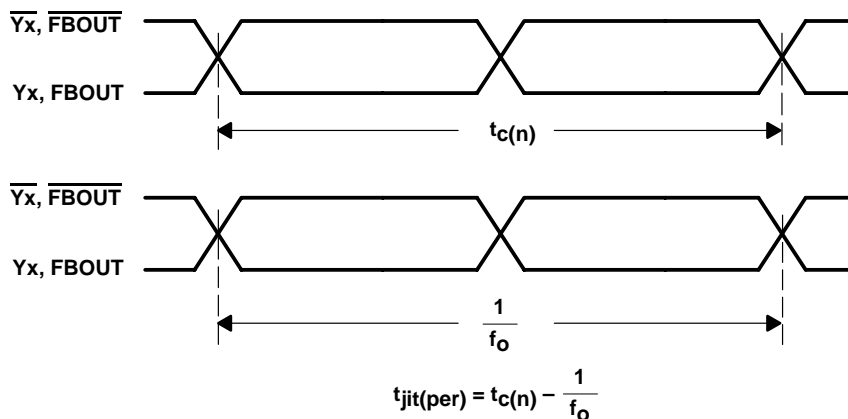


Figure 5. Period Jitter

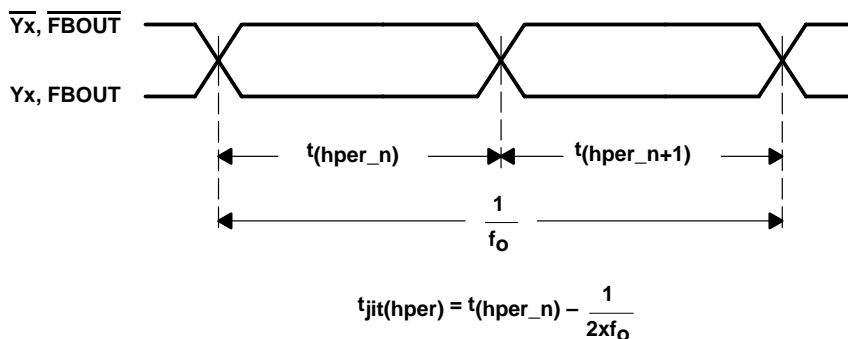


Figure 6. Half-Period Jitter

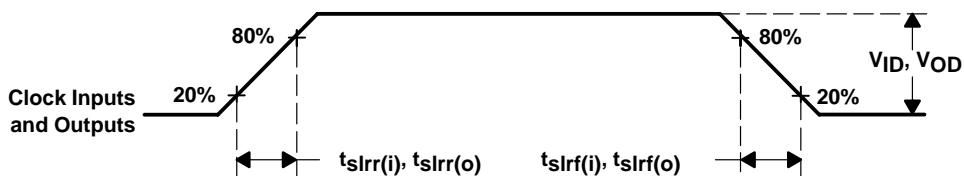


Figure 7. Input and Output Slew Rates

# CDCV855, CDCV855I 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

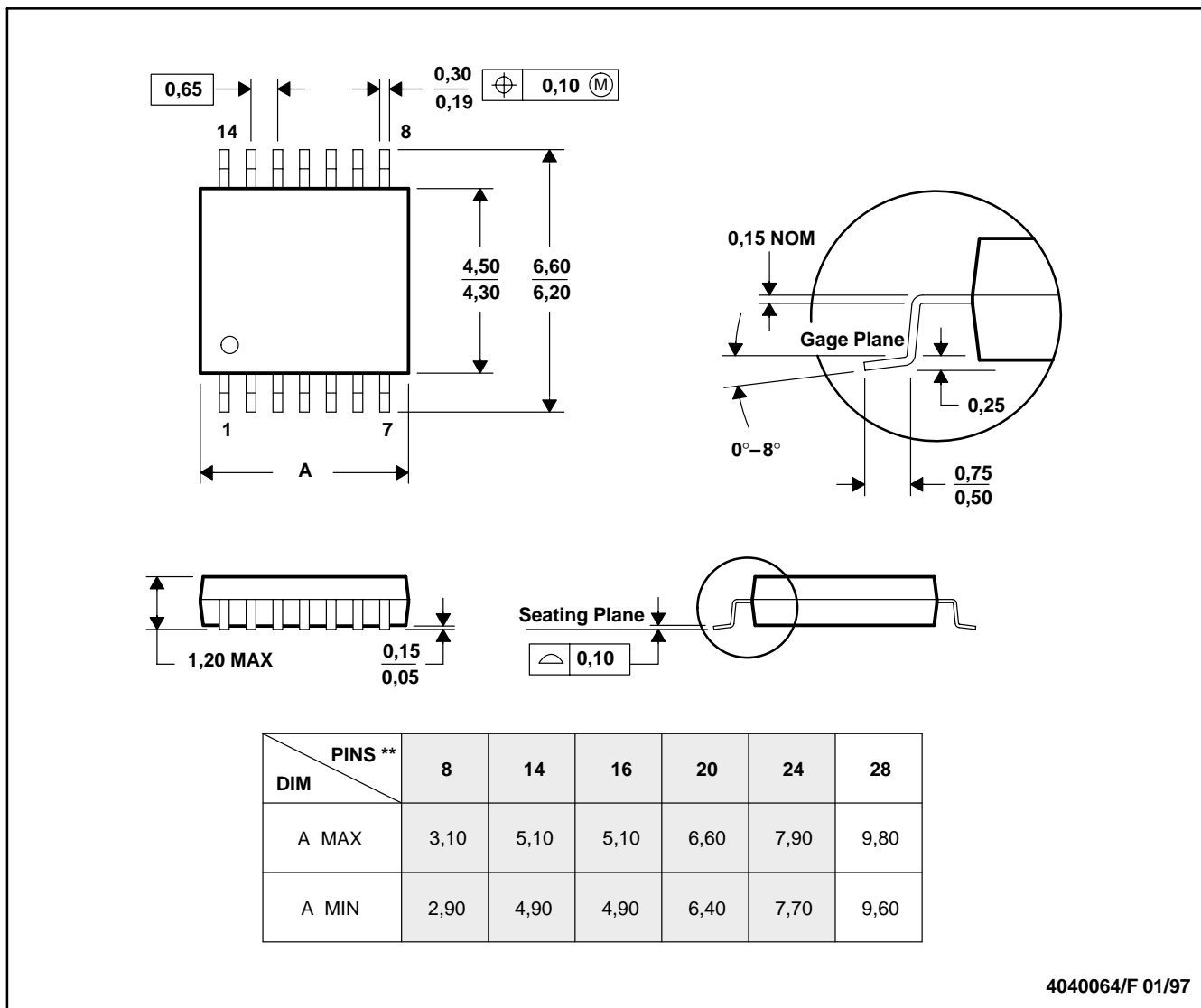
SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

## MECHANICAL DATA

**PW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDCV855IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV855IPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV855IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV855IPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV855PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV855PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV855PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV855PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated