

Design Considerations for TI's CDCV857/CDCV857A DDR PLL

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ABSTRACT

This application is a general guide for using Texas Instruments CDCV857/CDCV857A double data rate (DDR) clock driver. This report presents methods for using the device efficiently along with results of evaluation on device performance. In addition, several methods of terminating output signals and layout recommendation are provided for different applications.

Contents

1	Introduction.....	2
2	Definitions of Important Parameters	2
	2.1 Period Jitter.....	2
	2.2 Half-Period Jitter	3
	2.3 Cycle-to-Cycle Jitter	3
	2.4 Static Phase Offset	4
	2.5 Dynamic Phase Offset	4
	2.6 Output Skew	5
3	Testing CDCV857/CDCV857A	5
	3.1 Testing Equipment	5
	3.2 Testing Circuit Diagram.....	6
	3.3 Testing Procedure.....	6
	3.3.1 Measuring Jitter.....	6
4	Recommended Layout	10
	4.1 How to Choose Bypass Capacitor Values	11
	4.2 Prevent Noise Translating From Clock Driver to the Main PCB	12
5	DDR Termination	13
	5.1 Zero-Delay Tuning	15
6	References	16

Figures

Figure 1. Period Jitter	2
Figure 2. Half-Period Jitter	3
Figure 3. Cycle-to-Cycle Jitter	3
Figure 4. Static Phase Offset	4
Figure 5. Dynamic Phase Offset	4
Figure 6. Output Skew	5
Figure 7. Testing Circuit.....	6
Figure 8. M1 Window for Jitter Measurement	7
Figure 9. M1 Windows for Selecting O'Scope Channels to Measure Jitter.....	8

Figure 10.	M1 Window for Delay Measurement	9
Figure 11.	Selecting Channels to Measure Delay in M1	9
Figure 12.	CDCV857/CDCV857A Filter Circuit	10
Figure 13.	CDCV857/CDCV857A Alternate Filter Circuit	11
Figure 14.	CDCV857/CDCV857A in DDR Register DIMM	13
Figure 15.	Using CDCV857/CDCV857A for Single-Ended Outputs	14
Figure 16.	Using CDCV857/CDCV857A as a Single-Ended Input	15
Figure 17.	Normalized Delay From Y0/Y0# to CLK/CLK# as a Function of Feedback Capacitance (Cfb).....	16

1 Introduction

The CDCV857/CDCV857A is a high performance, low-skew, low-jitter phase-lock loop clock driver. It takes one pair of differential input signal and fans out to 10 pairs of differential output with low skew and low jitter. The feedback signals (FBOUT/FBOUT#) are required to externally connect to FBIN/FBIN# in order for the PLL to function. The CDCV857/CDCV857A uses the PLL to precisely align both phase and frequency of FBIN/FBIN# to input signal (CLK/CLK#). Delay from CLK/CLK# to outputs FBOUT/FBOUT# or Yn/Yn# can be adjusted to zero by changing the delay path from FBOUT/FBOUT# to FBIN/FBIN#.

2 Definitions of Important Parameters

2.1 Period Jitter

Period jitter is the maximum deviation of measured clock period with respect to ideal clock period over a large number of cycles. In DDR application, period jitter is the maximum deviation of measured clock period with respect to the average clock period measured over a large number of cycles.

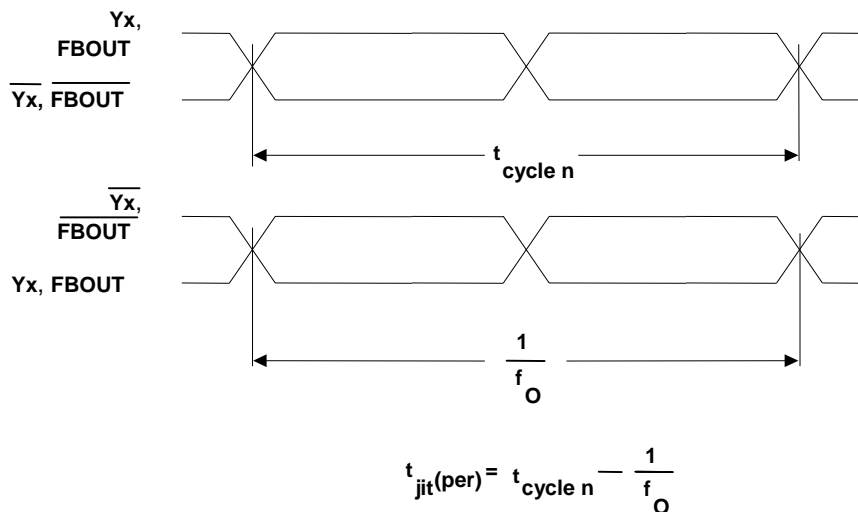


Figure 1. Period Jitter

2.2 Half-Period Jitter

Half-period jitter is the maximum deviation of every crossing point measured on clock waveforms with respect to half of ideal clock period over a large number of cycles. In the DDR application, half period jitter is the maximum deviation of every crossing points measured on clock waveforms with respect to the average of crossing points measured on clocked waveforms over a large number of cycles.

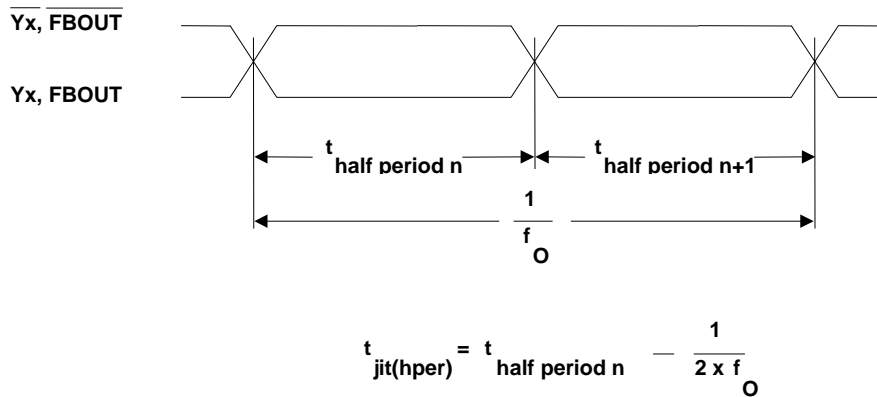


Figure 2. Half-Period Jitter

2.3 Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the difference in the period of successive cycles of a continuous clock pulse.

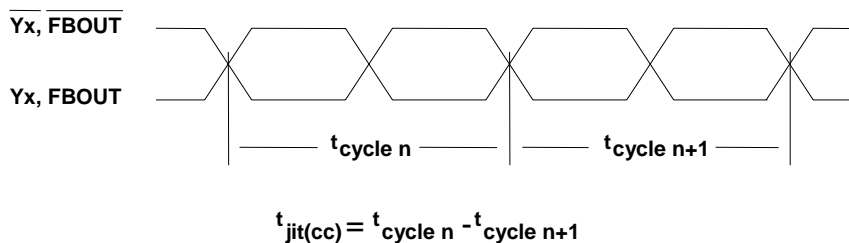
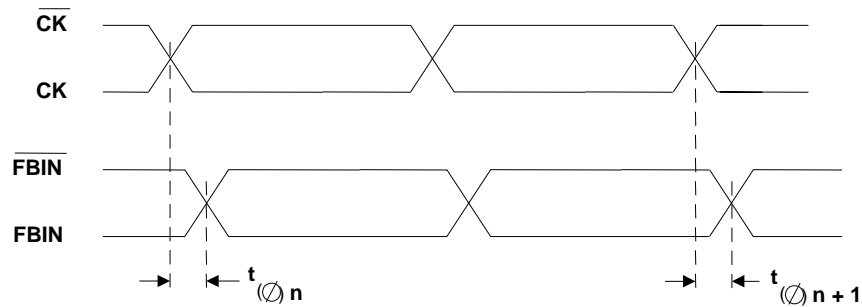


Figure 3. Cycle-to-Cycle Jitter

2.4 Static Phase Offset

Static phase offset is the difference between the averaged phase of the input clock and the averaged phase of the FBIN signal.



$$t_{\phi} = \frac{\sum_{N=1}^{N=N} 1 \cdot t_{\phi n}}{N}$$

(N is a large number of samples)

Figure 4. Static Phase Offset

2.5 Dynamic Phase Offset

Dynamic phase offset is the maximum phase deviation of the FBIN signals from the static phase offset.

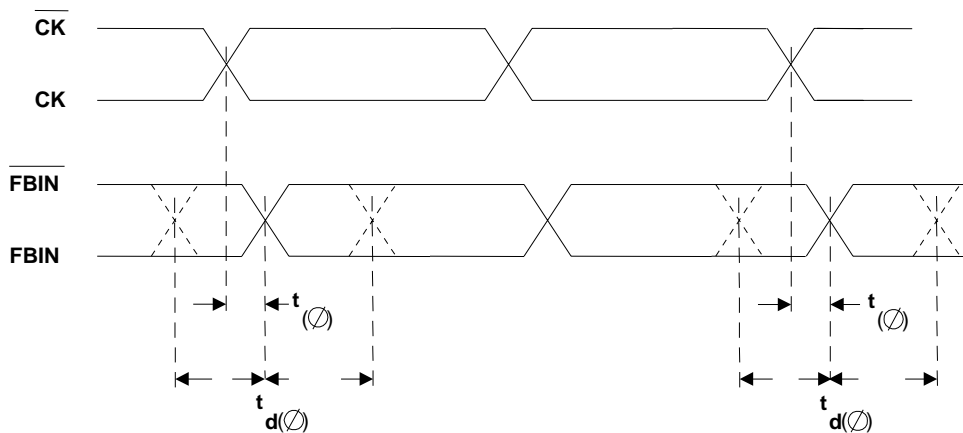


Figure 5. Dynamic Phase Offset

2.6 Output Skew

Output skew is the skew between any outputs on a single device when the outputs have identical loads and are switching in the same direction.

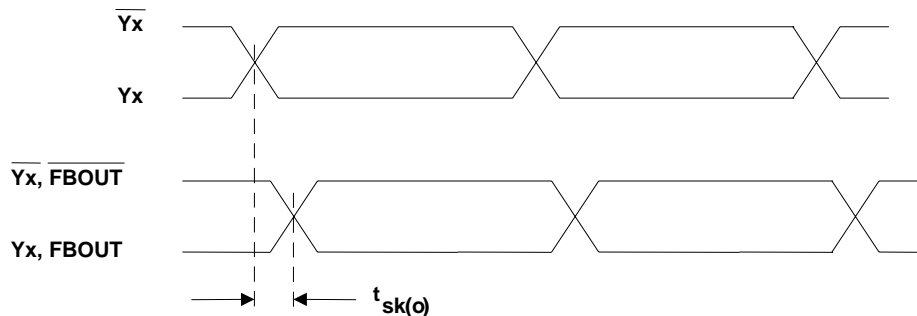


Figure 6. Output Skew

3 Testing CDCV857/CDCV857A

TI's test board and testing methodology have been chosen as a standard tool to evaluate DDR clock for the industry. With TI's testing methodology, users can easily evaluate CDCV857/CDCV857A accurately before putting the device in the system. Following is the required equipment, testing block diagram and testing procedure for evaluating CDCV857/CDCV857A.

3.1 Testing Equipment

1. Tektronix scope TDS694C or equivalent
2. M1 system
3. DC power supply
4. Function generator HP8133A or Tektronix HFS9003 or equivalent

3.2 Testing Circuit Diagram

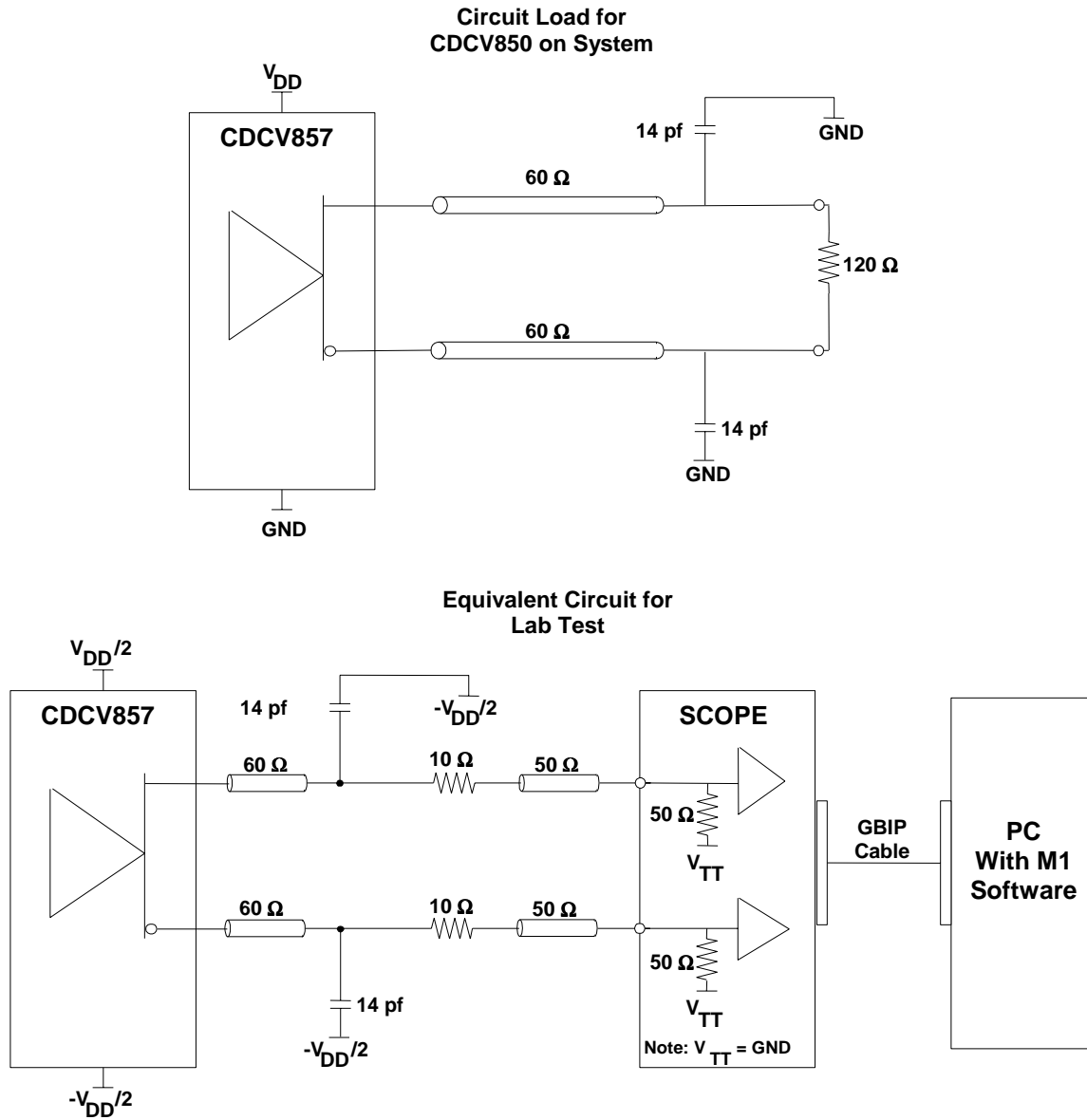


Figure 7. Testing Circuit

3.3 Testing Procedure

3.3.1 Measuring Jitter

After connecting the board as shown in Figure 7, open the M1 software from the PC. Select the radio button as shown in Figure 8 for measuring jitter.

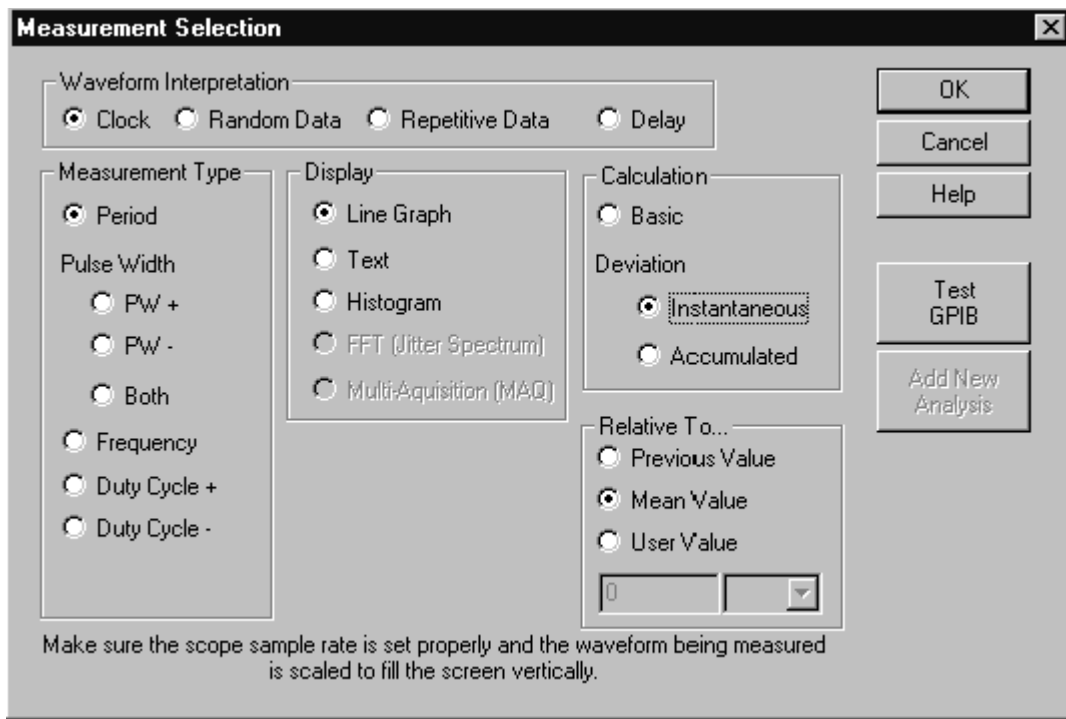


Figure 8. M1 Window for Jitter Measurement

Select OK after the selection has been made. Another window will be opened after OK has been selected. If Y and Y# are connected to channel 1 and channel 2 of the oscilloscope, the radio buttons on M1 display will be selected (+) for channel 1 and (-) for channel 2 and click OK as shown in Figure 9.

To measure jitter, select control → run → single shot (or continuous). Single shot takes only one acquisition while continuous takes acquisitions continuously. Period jitter is displayed in min and max places, cycle-cycle jitter is displayed in Lg Disp+ and Lg Disp-, and peak-peak jitter is shown in peak-peak.

To measure static and dynamic phase offsets, connect CLK and CLK# to channel 1 and 2 and connect FBIN and FBIN# to channel 3 and 4 respectively. On the first M1 window, select the Delay radio button as shown in Figure 10 and then click OK. When another window appears, select Delay from channel 1 and 2 to channel 3 and 4 as shown in Figure 11. Taking measurement acquisitions in single shot (or continuous) is the same as taking measurement on jitter. The static phase offset shows in Mean. Dynamic phase offset is the difference from max and min to the mean value.

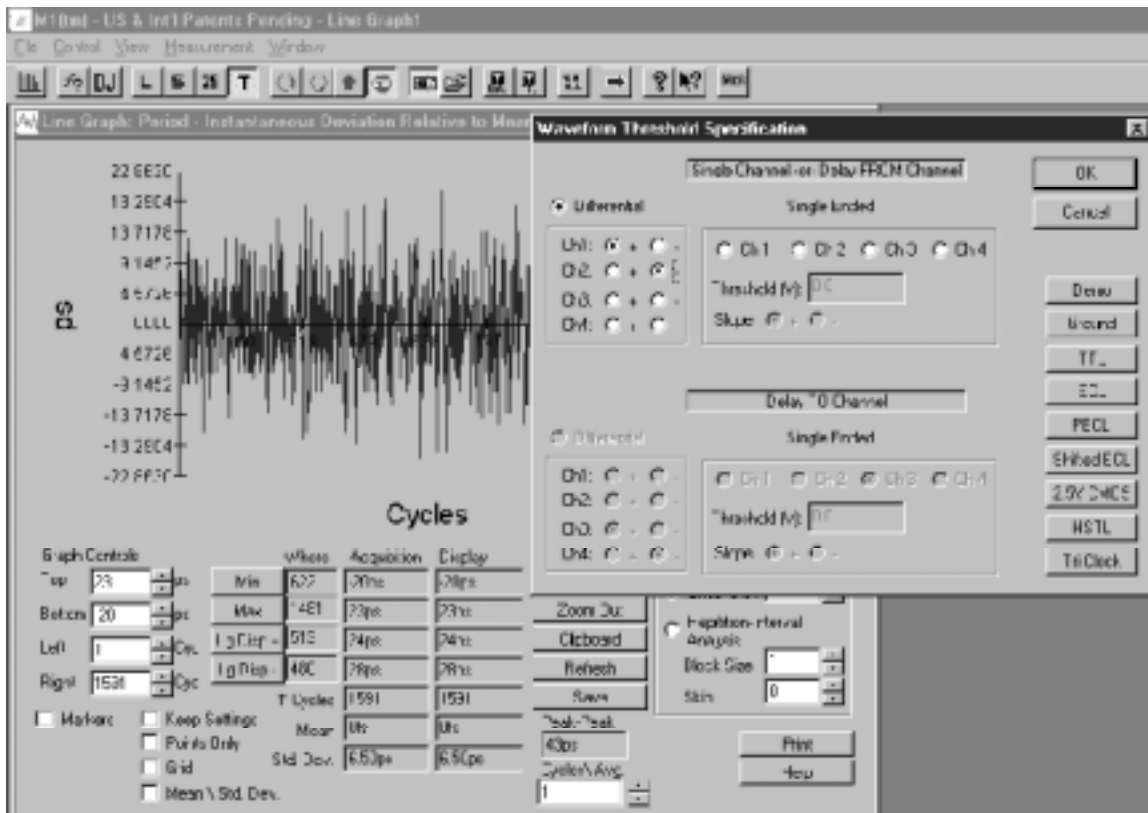


Figure 9. M1 Windows for Selecting O'Scope Channels to Measure Jitter

To measure output skew, connect one pair of outputs to channel one and two and the other pair to channel 3 and 4. The measurement procedure is the same as measuring phase offset. The output skew is shown in the Mean value.

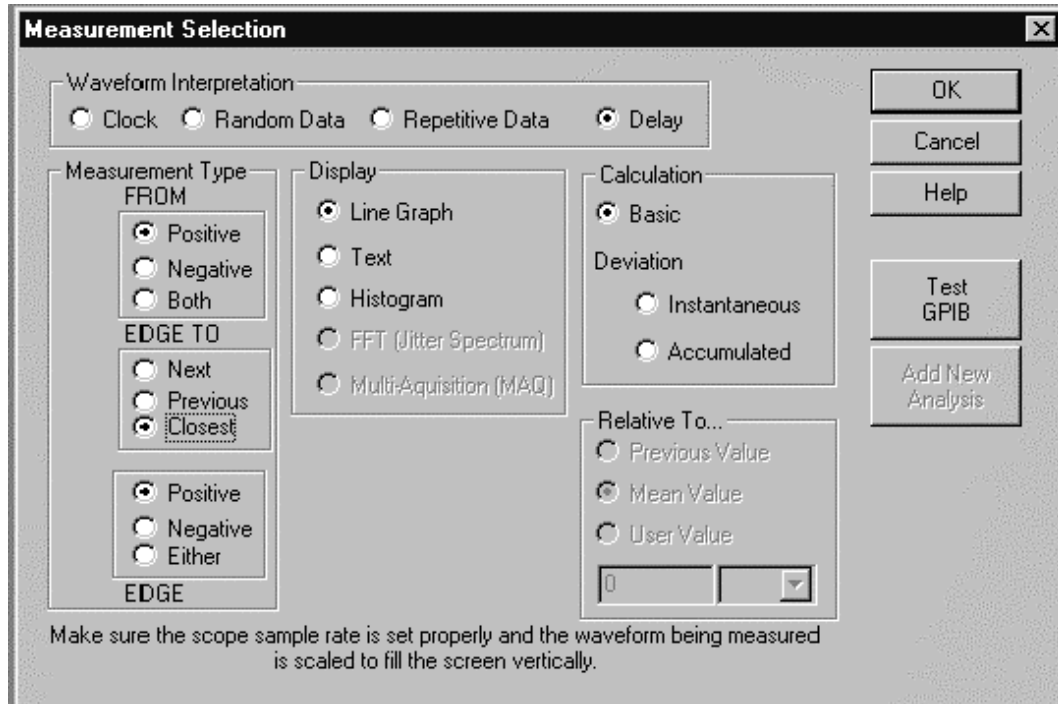


Figure 10. M1 Window for Delay Measurement

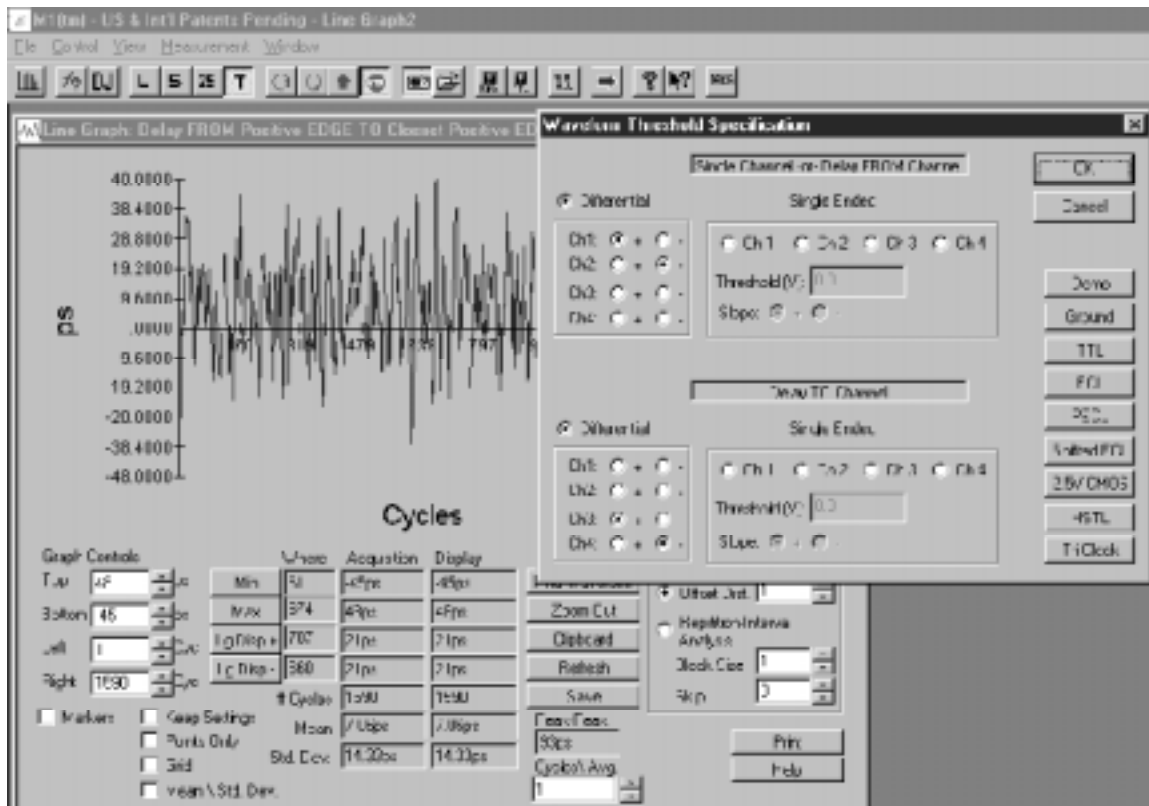


Figure 11. Selecting Channels to Measure Delay in M1

4 Recommended Layout

Avoid making vias if possible to reduce signal reflection due to discontinuity caused by vias.

Trace lengths of clock signal should be matched and each output should have equal load to minimize output skew.

Impedance on clock signals should be well-controlled to eliminate signal reflection and output skew.

It is recommended to terminate the clock signals differentially at the end of the transmission line.

Use at least one bypass capacitor of 0.1 μF for each VDDQ pin. The capacitor is placed as close to the device pin as possible. It is recommended to use a high-quality, surface-mount, low-inductance, and low-ESR capacitor. A surface mount capacitor in size of 0603 and types of mica or monolithic, ceramic are recommended. If possible, isolate the analog power plane (AVDD) from the digital power through a ferrite bead. Figure 12 and Figure 13 are two recommended circuits for filtering power. Figure 12 is recommended where there are no real estate constraints, while Figure 13 is the choice where there is limited board space.

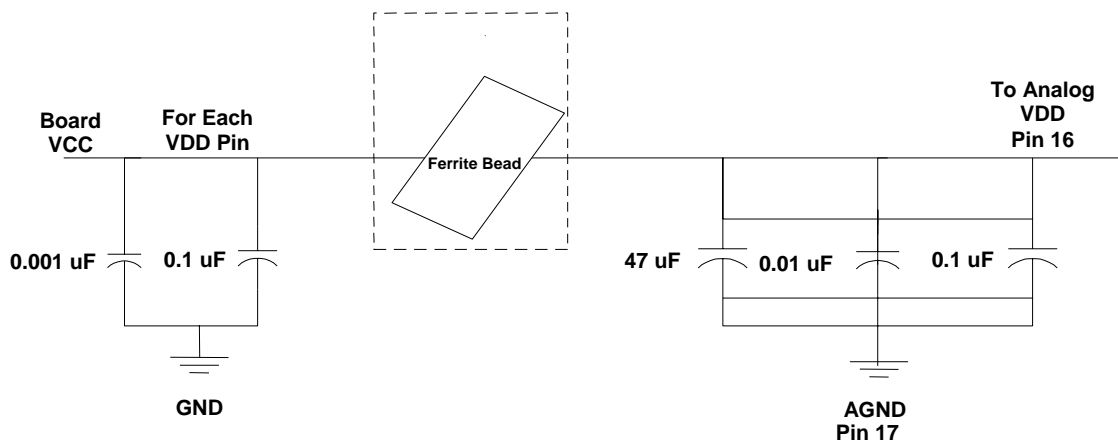


Figure 12. CDCV857/CDCV857A Filter Circuit

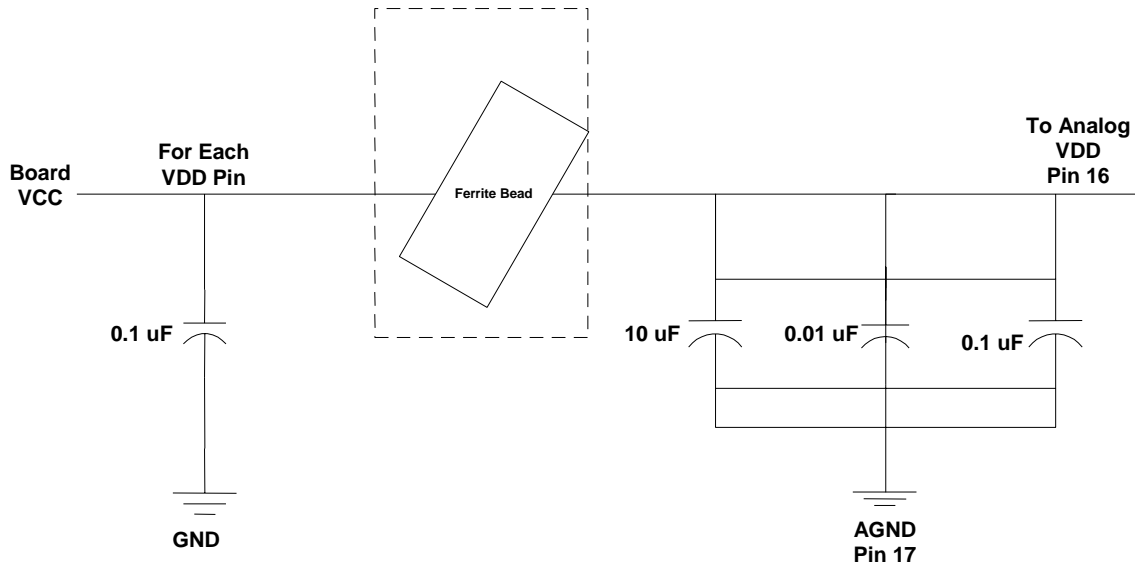


Figure 13. CDCV857/CDCV857A Alternate Filter Circuit

4.1 How to Choose Bypass Capacitor Values

Figures 12 and 13 are common circuits for power filtering. However, choosing efficient values for bypass capacitors requires a little math analysis.

In a system where there are many gates switching simultaneously, the dc voltage may fluctuate producing ac ripple voltage or noise components. If the ripple voltage is too high, it renders the circuit nonfunctional. The main function of bypass capacitors is to dampen this ac ripple component or noise. One function of a bypass capacitor connected between VDD and GND is to allow the ac ripple component of VDD to pass through to ground. Another function is to help compensate for voltage droop caused by large I_{CC} transient when multiple outputs switch simultaneously.

Assume the maximum step change in supply current is ΔI , the maximum amount supply noise that CDCV857/CDCV857A can tolerate is ΔV , and then the maximum common-pad (between Power and GND) impedance that CDCV857/CDCV857A can tolerate is:

$$X_{\max} = \frac{\Delta V}{\Delta I} \quad (1)$$

Assume all drivers on the board switch at the same frequency, then:

$$\Delta I = NC \frac{\Delta V}{\Delta t} \quad (2)$$

where C is the load capacitance on each driver,

N is the number of drivers in the system (number of outputs), and

Δt is the rise time from 10% to 90%.

Assume the power supply has inductance of L_{PSW} , then the circuit needs bypass capacitors if the switching frequency is above F_{PSW} . Where F_{PSW} is calculated using the following formula.

$$F_{PSW} = \frac{X_{max}}{2\pi L_{PSW}} \quad (3)$$

The capacitance that has impedance X_{MAX} at F_{PSW} is:

$$C_{MIN} = \frac{1}{2\pi F_{PSW} X_{MAX}} \quad (4)$$

The bypass capacitance (C_{BYPASS}) is chosen at least as big as C_{MIN} . The common range of C_{BYPASS} is from C_{MIN} to $100C_{MIN}$.

The noise voltage is due to the changing current through total inductance in the system when drivers are switching. The maximum inductance that the system can tolerate is:

$$L_{tot} = \frac{X_{max} T_r}{\pi} \quad (5)$$

where T_r is the rise time from 10% to 90%.

Since each bypass capacitor has series inductance L_C due to the lead package, an array of parallel capacitors is needed to reduce the inductance. The number of capacitors is determined based on equation 6.

$$N = \frac{L_C}{L_{tot}} \quad (6)$$

From the total capacitance calculated in equation 4, the capacitance of each capacitor in the array is:

$$C_{element} = \frac{C_{min}}{N} \quad (7)$$

preventing noise translating from the clock driver to the main PCB.

The clock drivers have switching noise associated with them. Using a ferrite bead between the clock driver's power supply and the main PCB power plane effectively eliminates this problem. The ferrite bead does not enhance nor degrade the performance of the driver; it is only used to provide noise isolation.

4.2 Prevent Noise Translating From Clock Driver to the Main PCB

The clock driver has switching noise associated with them. Using a ferrite bead between the clock driver's power supply and the main PCB power plane is a good method to effectively eliminate this problem. The ferrite bead does not enhance or degrade the performance of the driver; it is only used to provide noise isolation.

5 DDR Termination

Common use of CDCV857/CDCV857A is for DDR DIMM. The termination scheme in DDR DIMM is shown in Figure 14.

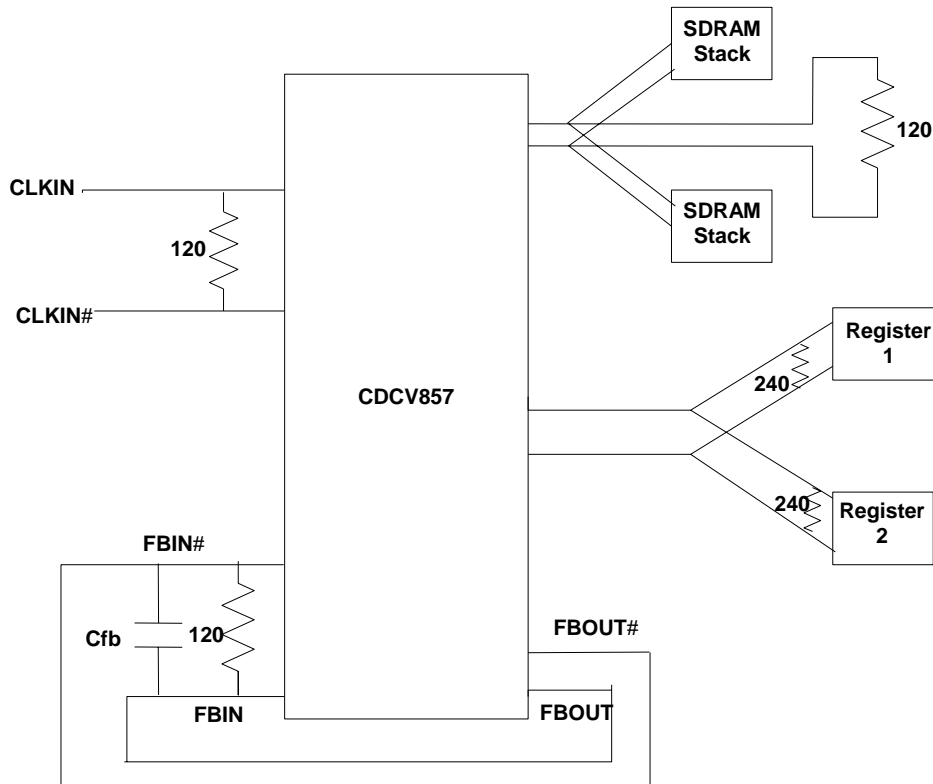


Figure 14. CDCV857/CDCV857A in DDR Register DIMM

The impedance of all traces connecting CDCV857/CDCV857A in DDR DIMM is 60-Ω single ended or 120-Ω differential. The length of each trace to meet the timing requirement for different raw cards of DDR DIMM is specified in the DDR SDRAM specification written by the IBM or JEDEC committee.

In some applications such as SERDES where single-ended clock is required, the CDCV857/CDCV857A outputs can be terminated single-ended to $V_{CC}/2$ as shown in Figure 15. The unused signal can be left floating.

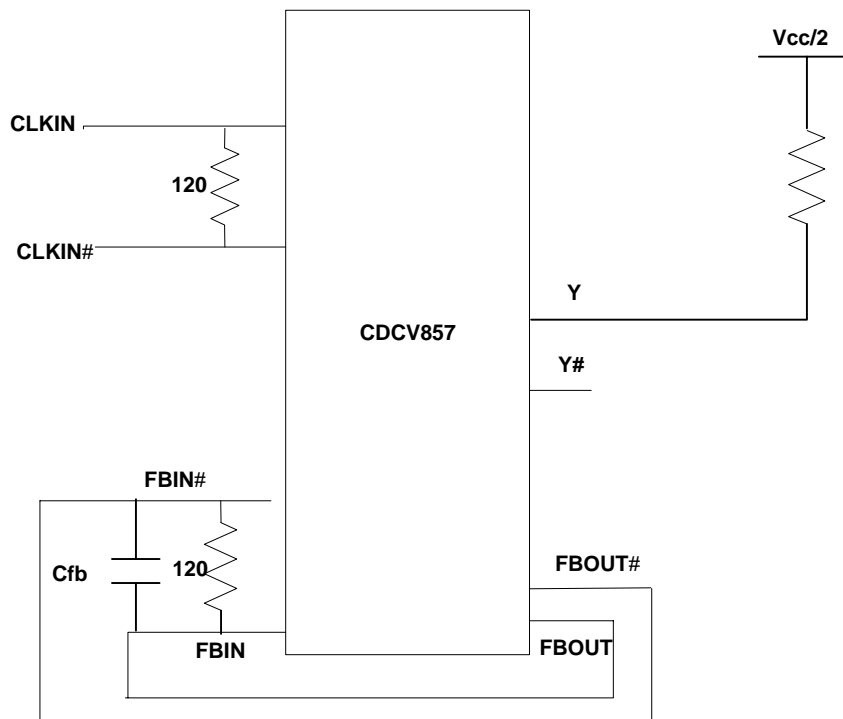


Figure 15. Using CDCV857/CDCV857A for Single-Ended Outputs

In some applications where the driver of CDCV857/CDCV857A is available in single-ended only, the CDCV857/CDCV857A can take single-ended input with a bias network as shown in Figure 16.

The designer must pay special attention on how to choose the values for R1, R2, R3, R4, and C in Figure 3. The dc voltage (V_{bias}) at nodes CLK and CLK# should be equal to $V_{cc}/2$ when no input signal is connected to input node. Thus,

$$\frac{R2}{R1 + R2} = \frac{R3}{R3 + R4} = \frac{1}{2} \quad \text{and}$$

$$R1 \parallel R2 = Z$$

where Z is the impedance of the transmission line of the driver driving the CDCV857/CDCV857A. Typically, $Z = 60 \Omega$. One selection for a 60- Ω transmission line is $R1 = R2 = R3 = R4 = 120 \Omega$.

C and a combination of parallel network R1 and R2 form a high-pass filter. Therefore, C should be large enough to pass the lowest frequency. A recommended value of C is 680 pF.

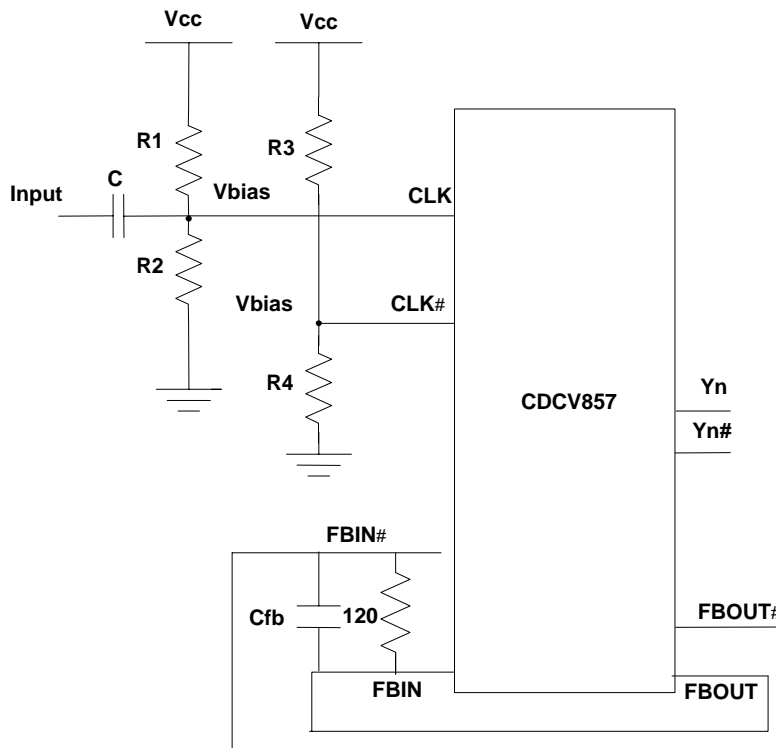


Figure 16. Using CDCV857/CDCV857A as a Single-Ended Input

5.1 Zero-Delay Tuning

The CDCV857/CDCV857A is a PLL clock driver. The propagation delay from the PLL input (CLK, CLK#) to the SDRAM input can be tuned to zero through the feedback capacitor (Cfb) as shown in Figure 14, Figure 15, or Figure 16. For zero delay from the PLL input to the SDRAM input, the trace length and trace characteristics of the feedback (FBOU, FBOU#) and the outputs (Yn, Yn#) have to be matched. Since the input capacitance of the FBIN and FBIN# pins of the CDCV857/CDCV857A is less than the loading capacitance on the output pins (total input capacitance of SDRAM), SDRAM input is slightly lagging the PLL input when Cfb = 0. Increasing the Cfb advances the SDRAM inputs relative to the PLL inputs. With a small value increase in Cfb, delay from the PLL input to the SDRAM input can be tuned to zero. If the SDRAM input is leading PLL input, decreasing Cfb adjusts the PLL input to SDRAM input to zero. Figure 17 is the graph of the normalized delay from Y0/Y0# to CLK/CLK# measured on the TI test board on a CDCV857A device. This delay is normalized to zero when there is no discrete feedback capacitor on feedback trace. With a small amount of capacitance added on each pin of FBOU and FBOU# to Vcc/2, the output Y0/Y0# advances with respect to input and increases the delay from output to input. The designer can use this graph as a reference to tune zero-delay from input to outputs.

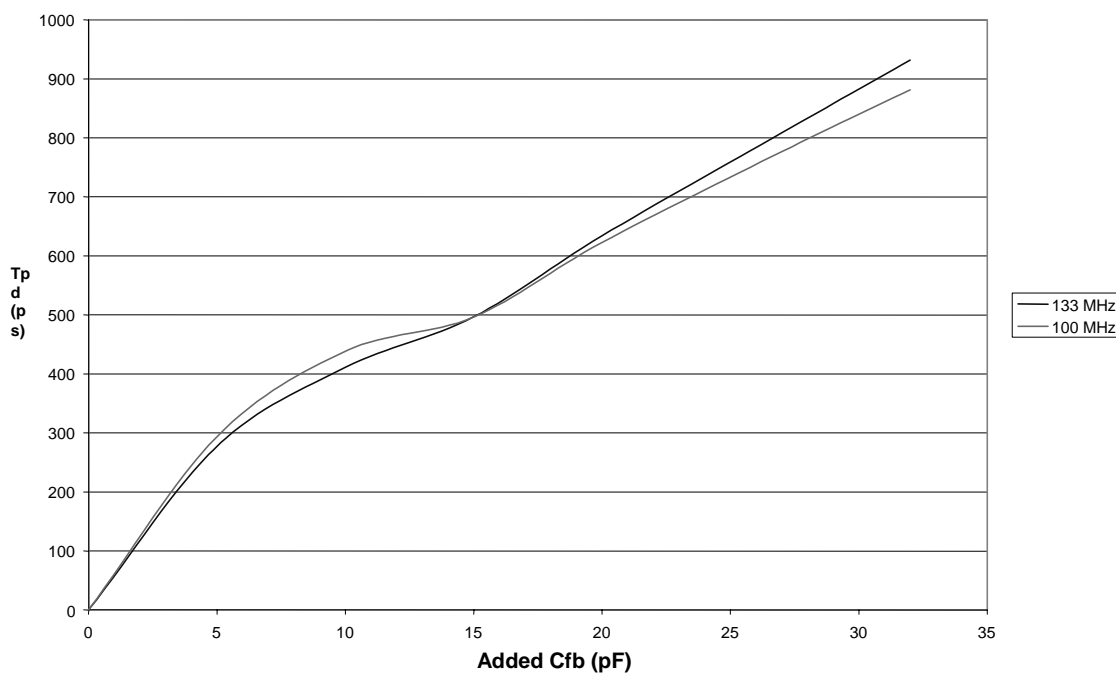


Figure 17. Normalized Delay From Y0/Y0# to CLK/CLK# as a Function of Feedback Capacitance (Cfb)

6 References

1. *DDR SDRAM Registered DIMM Design Specification* revision 1.0, July 2000, IBM, Micron Technology, and ServerWorks
2. Johnson, H.W., and Gram, M. *High-Speed Digital Design*. Prentice Hall, 1993.
3. *JEDEC Standard No. 65*, September 1998
4. *Using the CDC857 and CDCV850 to Transform a Single-Ended Clock Signal Into Differential Outputs* Texas Instruments application note, literature number SCAA043

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