



JEDEC DDRII Spec vs TI's PLL

Parameter	JEDEC PC3200/4300	CDCU877 CDCU877A
Vdd(V)	1.7~1.9	1.7~1.9
Idd(mA)	300	135
Freq(MHz)	125~270	125~400
Period Jitter(ps)	+/- 40	+/- 30
Output Skew(ps)	+/- 40	+/- 30
C-C jitter(ps)	+/- 40	+/- 30
Half Period Jitter(ps) @200MHz	+/- 75	+/- 75
Half Period Jitter(ps) @270MHz	+/- 75	+/- 40
PLL Lock time(us)	15	10
Temp(deg)	0, 70	-40, 85
SPO(ps)	+/- 50	+/- 50
DPO(ps)	+/- 50	+/- 20
Output Duty Cycle(%)	48.5 - 51.5%	49.5~50.5%
Slew Rate(V/ns)	1.5~3.0	1.5~3.0
Vcross(mV)	+/- 100	+/- 100

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