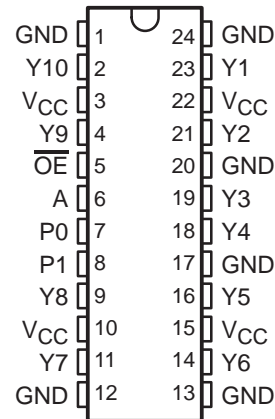


# CDC2351 1-LINE TO 10-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS442D – FEBRUARY 1994 – REVISED SEPTEMBER 2000

- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V  $V_{CC}$
- LVTTTL-Compatible Inputs and Outputs
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Distributes One Clock Input to Ten Outputs
- Outputs Have Internal Series Damping Resistor to Reduce Transmission Line Effects
- Distributed  $V_{CC}$  and Ground Pins Reduce Switching Noise
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages
- Available in Q-Temp Automotive High Reliability Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

DB OR DW PACKAGE  
(TOP VIEW)



## description

The CDC2351 is a high-performance clock-driver circuit that distributes one input (A) to ten outputs (Y) with minimum skew for clock distribution. The output-enable ( $\overline{OE}$ ) input disables the outputs to a high-impedance state. Each output has an internal series damping resistor to improve signal integrity at the load. The CDC2351 operates at nominal 3.3-V  $V_{CC}$ .

The propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part-to-part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

The CDC2351 is characterized for operation from 0°C to 70°C. The CDC2351Q is characterized for operation over the full automotive temperature range of –40°C to 125°C.

FUNCTION TABLE

INPUTS		OUTPUTS
A	$\overline{OE}$	In
L	H	Z
H	H	Z
L	L	L
H	L	H



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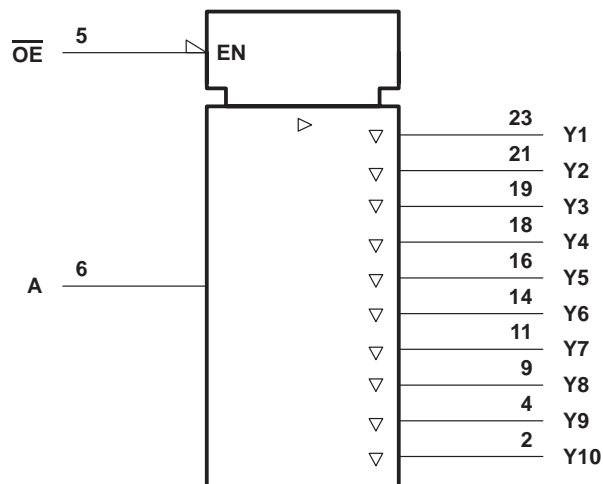


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# CDC2351 1-LINE TO 10-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

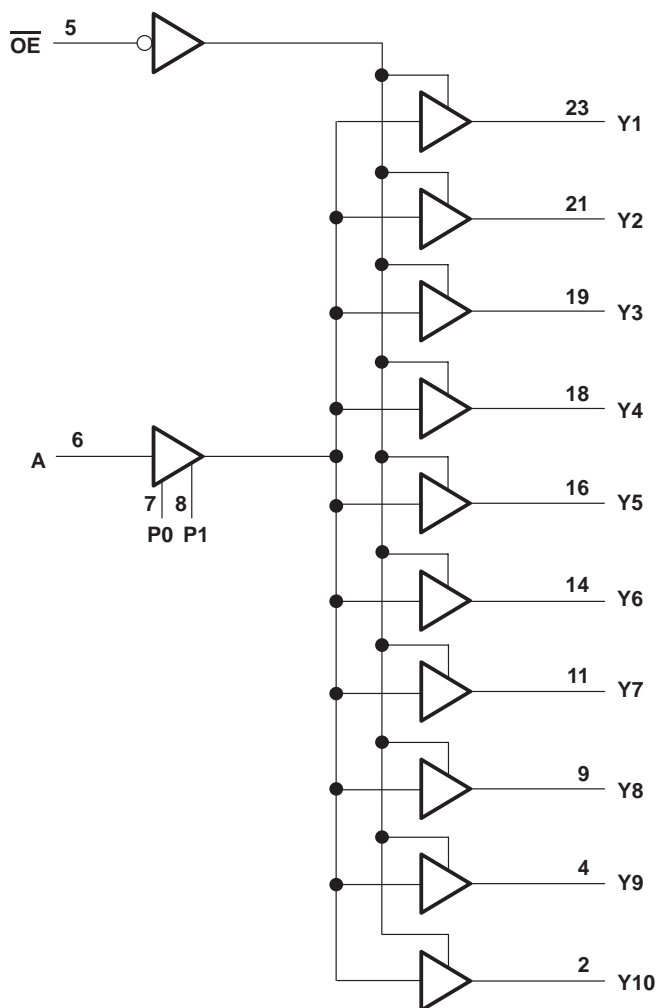
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# CDC2351 1-LINE TO 10-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 3.6 V
Current into any output in the low state, $I_O$ .....	24 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_I < 0$ ) .....	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package .....	0.65 W
DW package .....	1.7 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.  
 For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	3	3.6	V	
$V_{IH}$	High-level input voltage	2		V	
$V_{IL}$	Low-level input voltage		0.8	V	
$V_I$	Input voltage	0	5.5	V	
$I_{OH}$	High-level output current		–12	mA	
$I_{OL}$	Low-level output current		12	mA	
$f_{clock}$	Input clock frequency		100	MHz	
$T_A$	Operating free-air temperature	CDC2351	0	70	°C
		CDC2351Q	–40	125	

NOTE 3: Unused pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IK}$	$V_{CC} = 3\text{ V}$ ,	$I_I = -18\text{ mA}$			–1.2	V
$V_{OH}$	$V_{CC} = 3\text{ V}$ ,	$I_{OH} = -12\text{ mA}$	2			V
$V_{OL}$	$V_{CC} = 3\text{ V}$ ,	$I_{OL} = 12\text{ mA}$			0.8	V
$I_I$	$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}$ or GND			$\pm 1$	$\mu\text{A}$
$I_{O\ddagger}$	$V_{CC} = 3.6\text{ V}$ ,	$V_O = 2.5\text{ V}$	–7		–70	mA
$I_{OZ}$	$V_{CC} = 3.6\text{ V}$ ,	$V_{CC} = 3\text{ V}$ or 0			$\pm 10$	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ ,	$I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high		0.3	mA
			Outputs low		15	
			Outputs disabled		0.3	
$C_i$	$V_I = V_{CC}$ or GND,	$V_{CC} = 3.3\text{ V}$ ,	$f = 10\text{ MHz}$		4	pF
$C_o$	$V_O = V_{CC}$ or GND,	$V_{CC} = 3.3\text{ V}$ ,	$f = 10\text{ MHz}$		6	pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



**CDC2351**  
**1-LINE TO 10-LINE CLOCK DRIVER**  
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**switching characteristics,  $C_L = 50 \text{ pF}$  (see Figures 1 and 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CDC2351			CDC2351Q		CDC2351		UNIT
			$V_{CC} = 3.3 \text{ V}$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , $T_A = -40^\circ\text{C to } 125^\circ\text{C}$		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , $T_A = 0^\circ\text{C to } 70^\circ\text{C}$		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	3.8	4.3	4.8	1.1	11			ns
$t_{PHL}$			3.6	4.1	4.6	1	9.7			
$t_{PZH}$	$\overline{OE}$	Y	2.4	4.9	6.0	1	12	1.8	6.9	ns
$t_{PZL}$			2.4	4.3	6.0	1	11.1	1.8	6.9	
$t_{PHZ}$	$\overline{OE}$	Y	2.2	4.4	6.3	1	11.1	2.1	7.1	ns
$t_{PLZ}$			2.2	4.6	6.3	1	11.5	2.1	7.3	
$t_{sk(o)}$	A	Y		0.3	0.5		2.5		0.5	ns
$t_{sk(p)}$	A	Y		0.2	0.8		3		0.8	ns
$t_{sk(pr)}$	A	Y			1				1	ns
$t_r$	A	Y					2.5		2.5	ns
$t_f$	A	Y					2.5		2.5	ns

**switching characteristics temperature and  $V_{CC}$  coefficients over recommended operating free-air temperature and  $V_{CC}$  range (see Note 4)**

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$\propto t_{PLH}(T)$	Average temperature coefficient of low to high propagation delay	A	Y		85 <sup>†</sup>	ps/10°C
$\propto t_{PHL}(T)$	Average temperature coefficient of high to low propagation delay	A	Y		50 <sup>†</sup>	ps/10°C
$\propto t_{PLH}(V_{CC})$	Average $V_{CC}$ coefficient of low to high propagation delay	A	Y		-145 <sup>‡</sup>	ps/ 100 mV
$\propto t_{PHL}(V_{CC})$	Average $V_{CC}$ coefficient of high to low propagation delay	A	Y		-100 <sup>‡</sup>	ps/ 100 mV

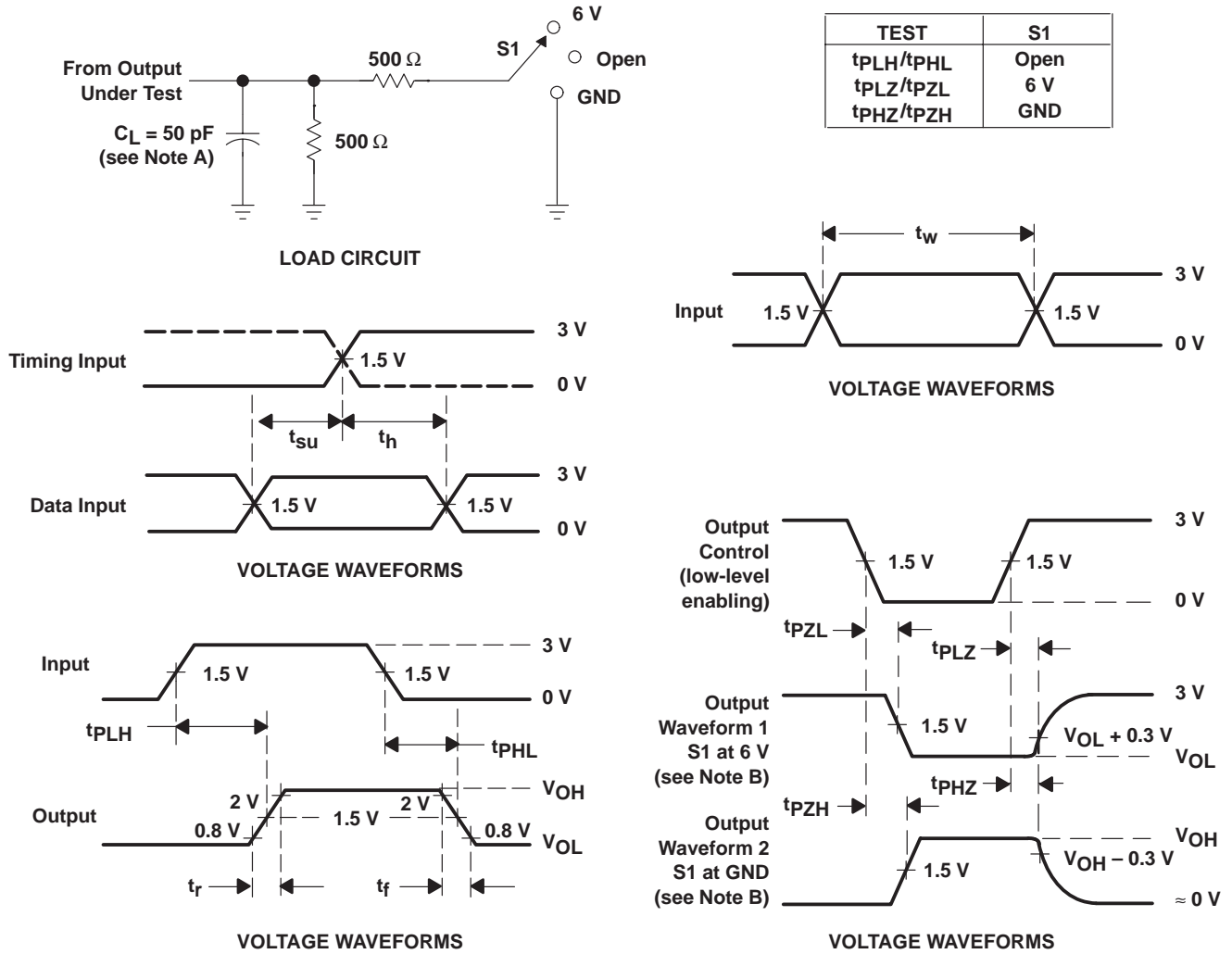
<sup>†</sup>  $\propto t_{PLH}(T)$  and  $\propto t_{PHL}(T)$  are virtually independent of  $V_{CC}$ .

<sup>‡</sup>  $\propto t_{PLH}(V_{CC})$  and  $\propto t_{PHL}(V_{CC})$  are virtually independent of temperature.

NOTE 4: This data was extracted from characterization material and are not tested at the factory.



**PARAMETER MEASUREMENT INFORMATION**



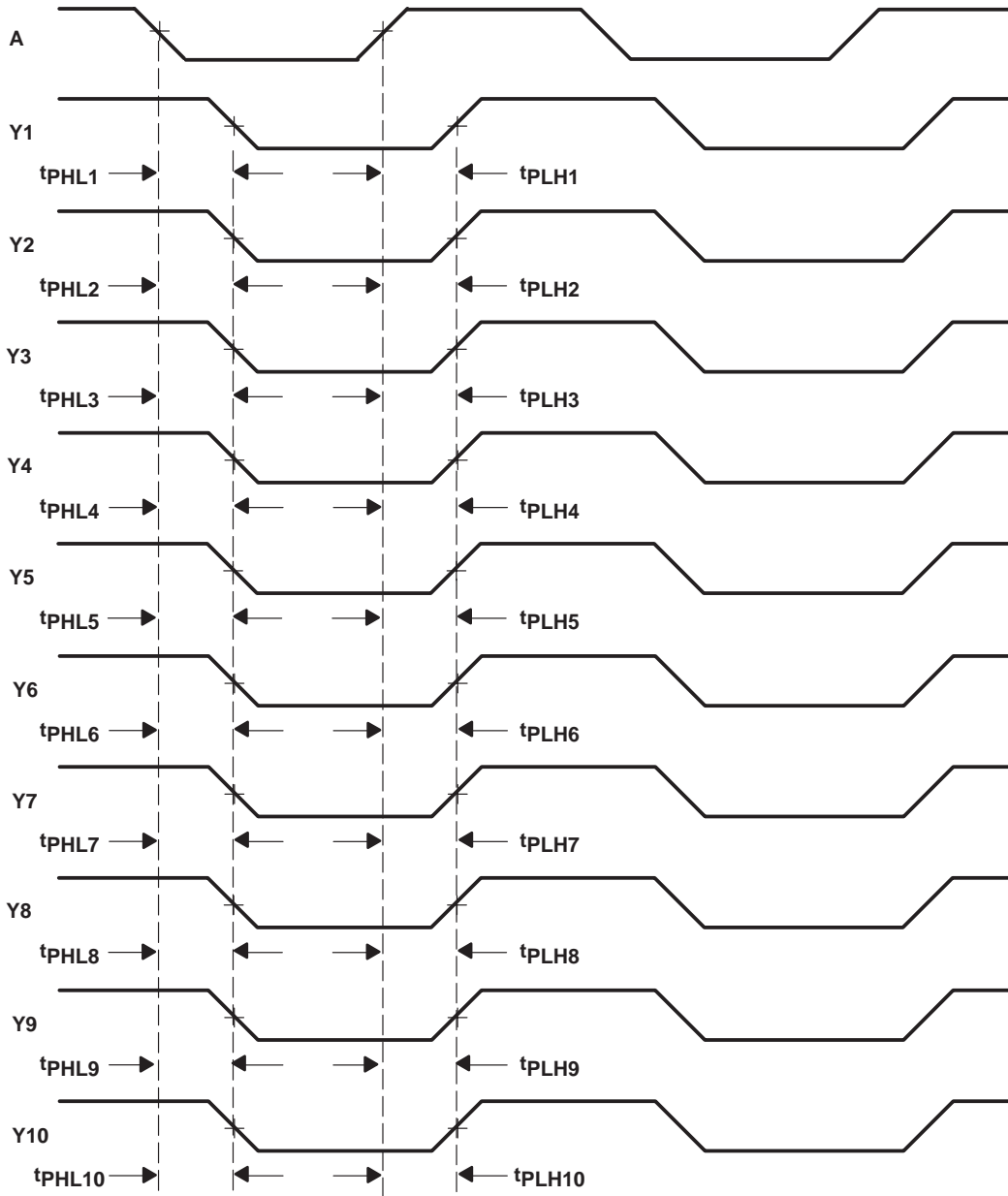
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**CDC2351**  
**1-LINE TO 10-LINE CLOCK DRIVER**  
**WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. Output skew,  $t_{sk(o)}$ , is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$ )
  - The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$ )
- B. Pulse skew,  $t_{sk(p)}$ , is calculated as the greater of  $|t_{PLHn} - t_{PHLn}|$  ( $n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$ ).
- C. Process skew,  $t_{sk(pr)}$ , is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$ ) across multiple devices under identical operating conditions
  - The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$ ) across multiple devices under identical operating conditions

**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$ ,  $t_{sk(p)}$ ,  $t_{sk(pr)}$**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CDC2351DB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351DBG4	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	
CDC2351DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351PWR	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	
CDC2351PWRG4	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	
CDC2351QDB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351QDBG4	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351QDBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CDC2351QDBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

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<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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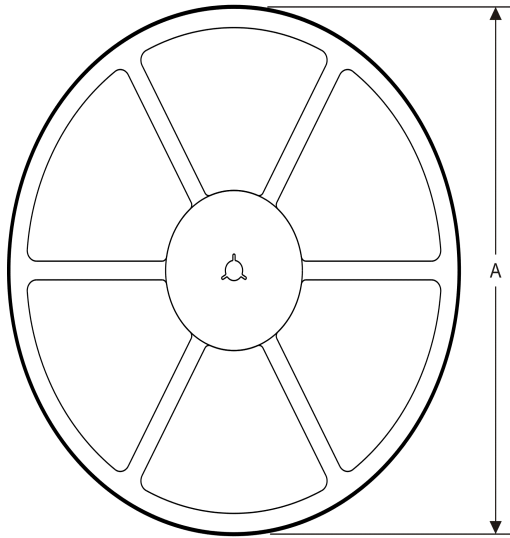
- Enhanced Product: [CDC2351-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC2351DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
CDC2351QDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

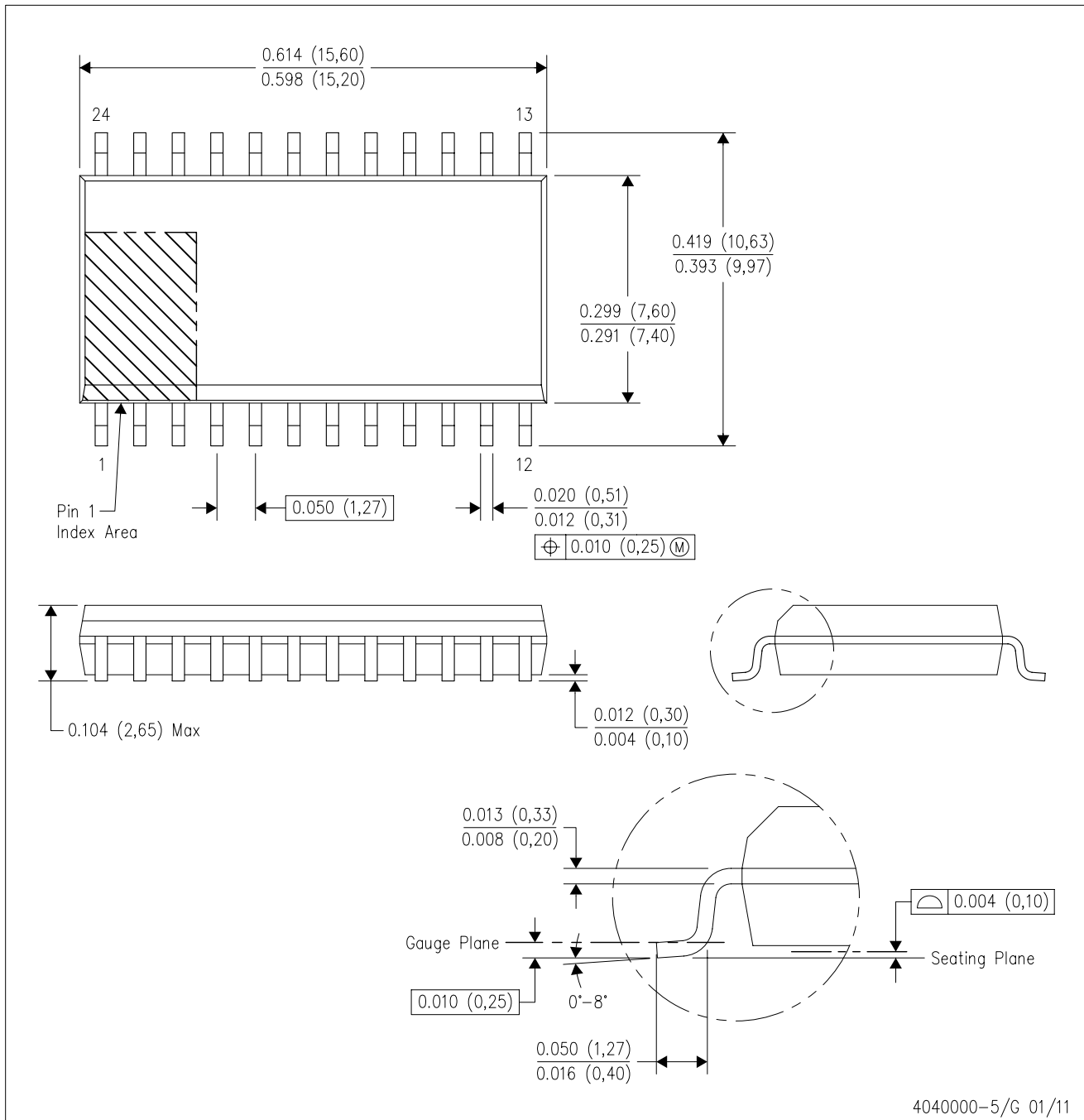
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC2351DBR	SSOP	DB	24	2000	367.0	367.0	38.0
CDC2351QDBR	SSOP	DB	24	2000	367.0	367.0	38.0

DW (R-PDSO-G24)

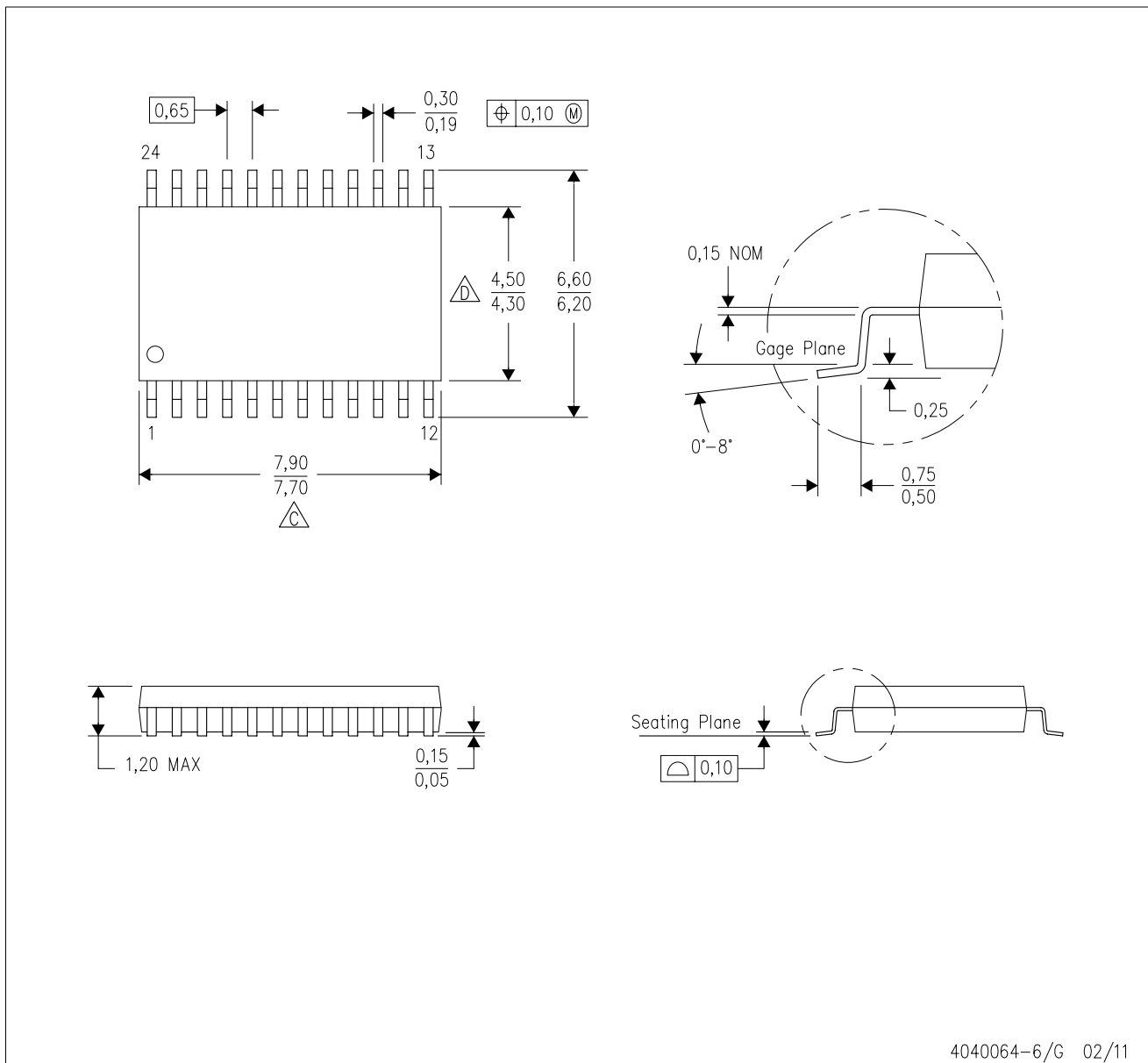
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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