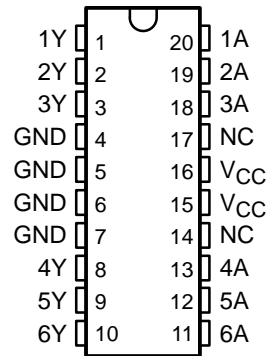


- Replaces 74AC11203
- Low-Skew Propagation Delay Specifications for Clock Driver Applications
- Operates at 3.3-V  $V_{CC}$
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Packaged in Plastic Small-Outline Package

**DW PACKAGE**  
**(TOP VIEW)**



NC – No internal connection

**description**

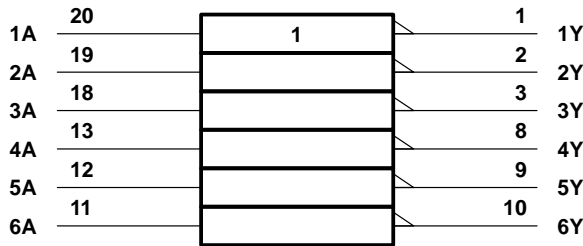
The CDC203 contains six independent inverters. The device performs the Boolean function  $Y = \bar{A}$ . It is designed specifically for applications requiring low skew between switching outputs.

The CDC203 is characterized for operation from 25°C to 70°C.

**FUNCTION TABLE**

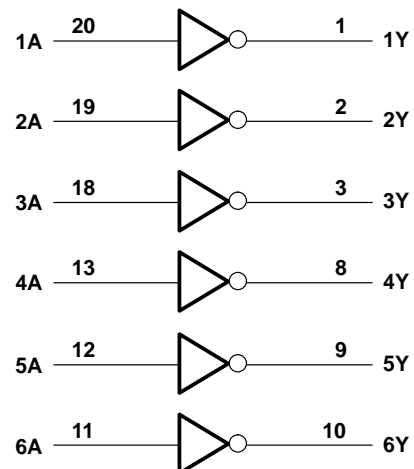
INPUT A	OUTPUT Y
H	L
L	H

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



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# CDC203

## 3.3-V HEX INVERTER/CLOCK DRIVER

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 150$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	1.6 W
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 3.6$ V	2.5		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 3.6$ V		1.1	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3$ V		-12	mA
		$V_{CC} = 3.6$ V		-12	
$I_{OL}$	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 3.6$ V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
$f_{clock}$	Input clock frequency			40	MHz
$T_A$	Operating free-air temperature	25		70	$^\circ\text{C}$



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = - 50 μA	3 V	2.9			2.9		V
		3.6 V	3.5			3.5		
	I <sub>OH</sub> = - 12 mA	3 V	2.58			2.48		
		3.6 V	3.18			3.08		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V				0.1	0.1	V
		3.6 V				0.1	0.1	
	I <sub>OL</sub> = 12 mA	3 V				0.36	0.44	
		3.6 V				0.36	0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V				±0.1	±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V				4	40	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V				4		pF

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (see Note 3 and Figures 1 and 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>PLH</sub>	A	Y	3.5	6.1	ns
t <sub>PHL</sub>			3.5	6.1	
t <sub>sk(o)</sub>	A	Y		0.7	ns

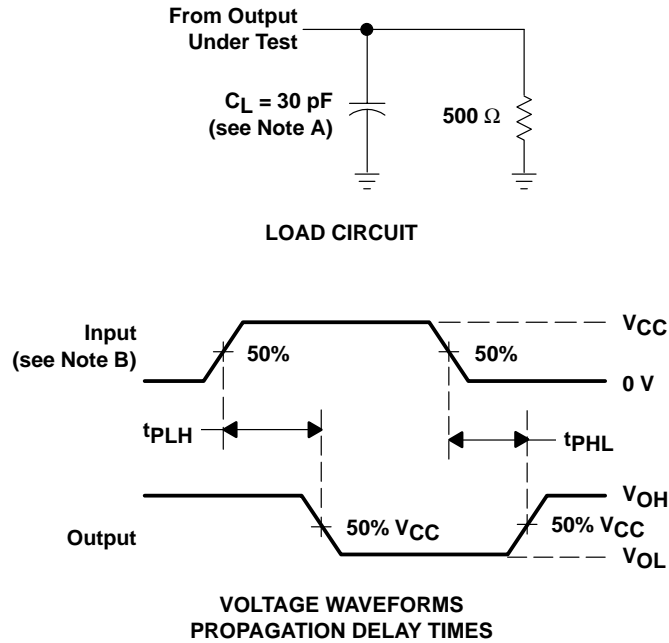
NOTE 3: All specifications are valid only for all outputs switching in phase simultaneously.

# CDC203

## 3.3-V HEX INVERTER/CLOCK DRIVER

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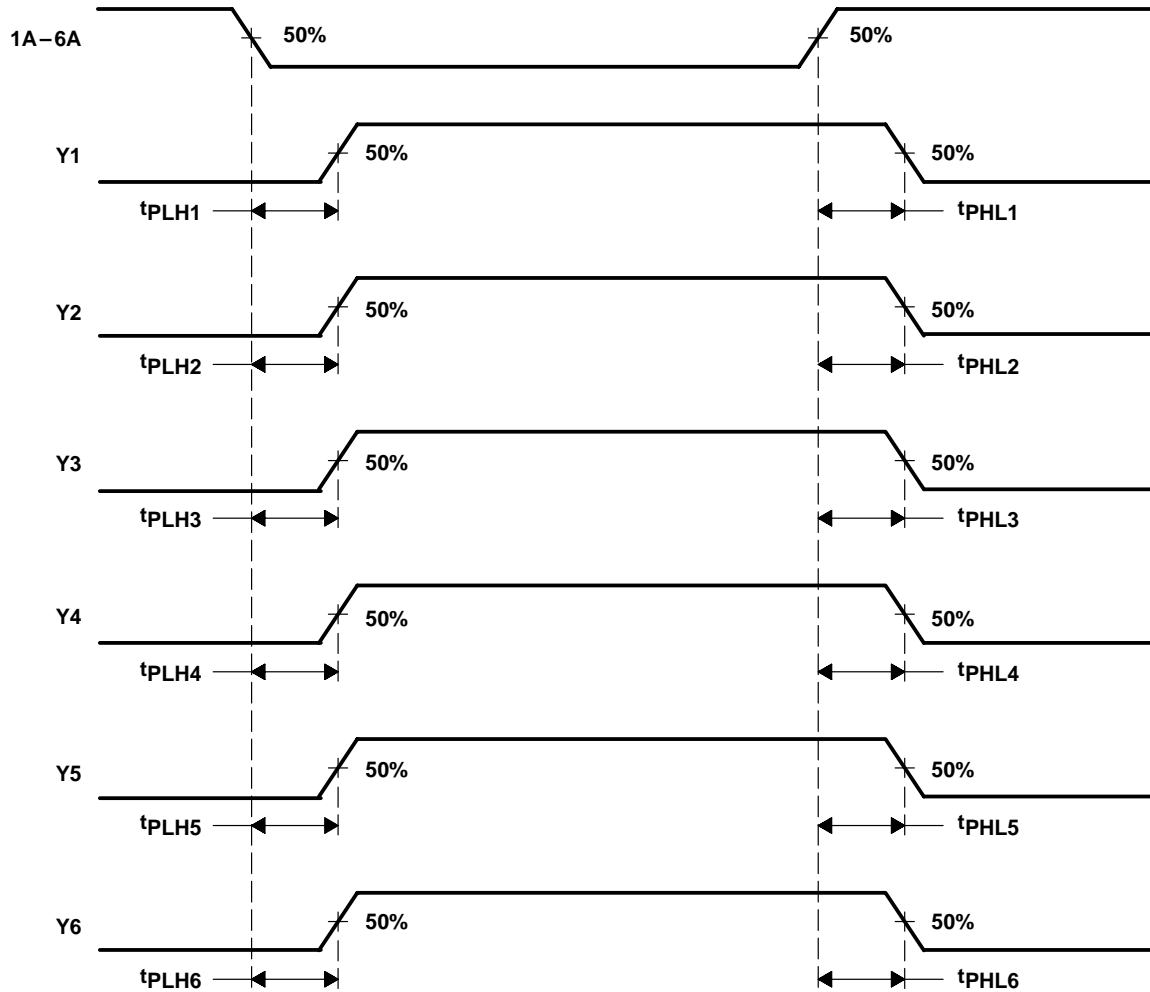
### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew,  $t_{sk(o)}$ , is calculated as the greater of:  
 – The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, \dots, 6$ )  
 – The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1, 2, \dots, 6$ )

Figure 2. Waveforms for Calculation of  $t_{sk(o)}$

# CDC203

## 3.3-V HEX INVERTER/CLOCK DRIVER

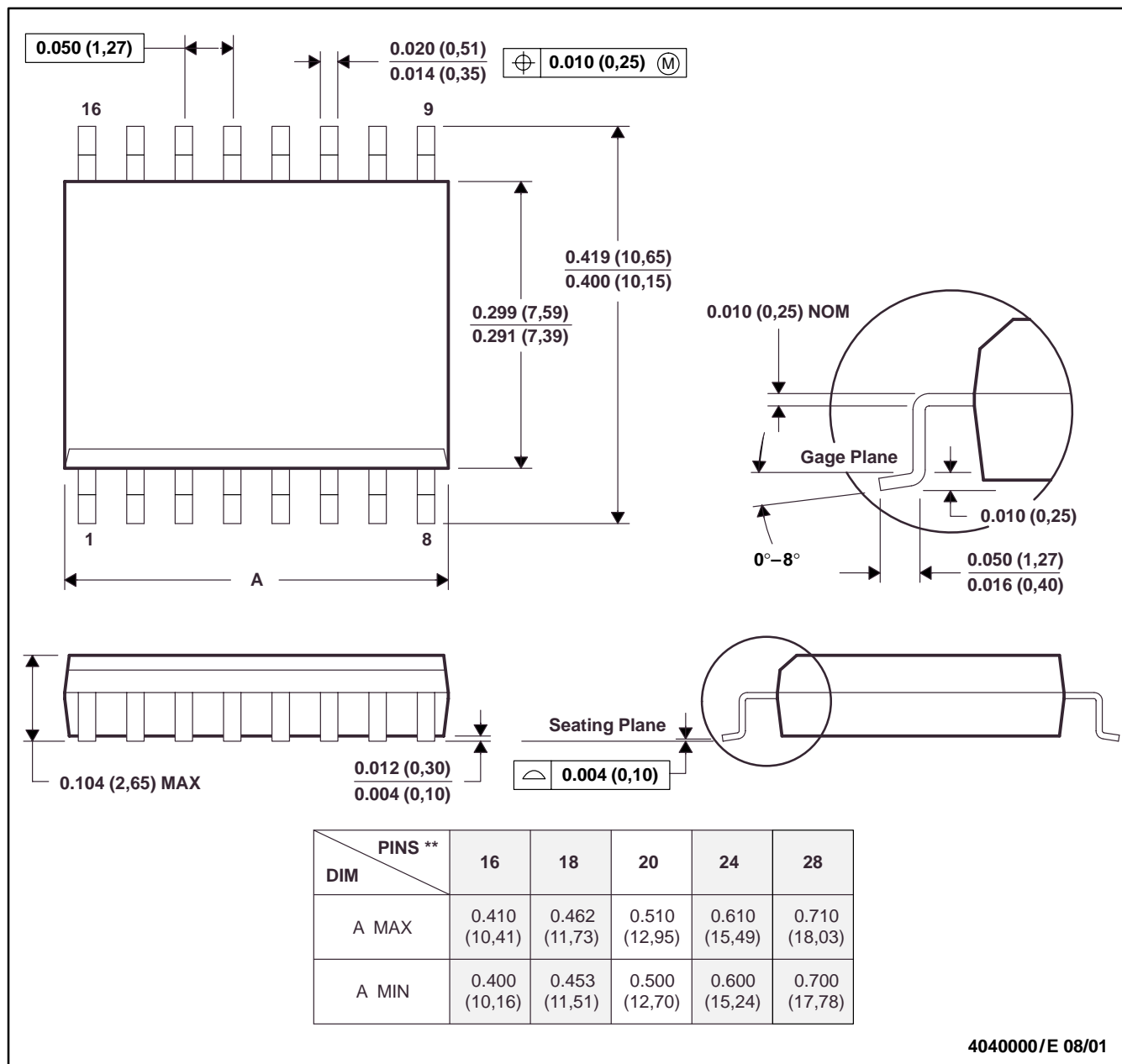
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### MECHANICAL DATA

DW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDC203DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC203DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC203DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC203DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC203DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC203DWR	SOIC	DW	20	2000	346.0	346.0	41.0

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