

August 1997 - Revised September 2003

**High-Speed CMOS Logic  
4-Bit Binary Ripple Counter**

**Features**

- Can Be Configured to Divide By 2, 8, and 16
- Asynchronous Master Reset
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

**Description**

The CD74HC93 and CD74HCT93 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ( $\overline{CP0}$  and  $\overline{CP1}$ ) to initiate state changes of the counter on the HIGH to LOW clock transition. State changes of the  $Q_n$  outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

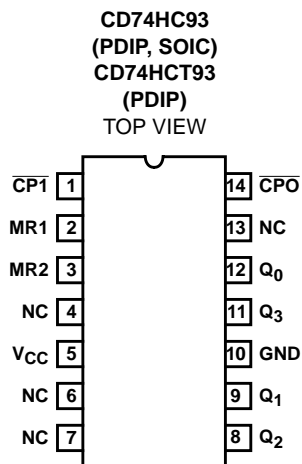
A gated AND asynchronous master reset (MR1 and MR2 is provided which overrides both clocks and resets (clears) all flip-flops.

Because the output from the divide by two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a 4-bit ripple counter the output  $Q_0$  must be connected externally to input  $\overline{CP1}$ . The input count pulses are applied to clock input  $\overline{CP0}$ . Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the  $Q_0$ ,  $Q_1$ ,  $Q_2$ , and  $Q_3$  outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input  $\overline{CP1}$ .

Simultaneous frequency divisions of 2, 4, and 8 are available at the  $Q_1$ ,  $Q_2$ ,  $Q_3$  outputs. Independent use of the first flip-flop is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

**Pinout**



**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC93E	-55 to 125	14 Ld PDIP
CD74HC93M	-55 to 125	14 Ld SOIC
CD74HC93MT	-55 to 125	14 Ld SOIC
CD74HC93M96	-55 to 125	14 Ld SOIC
CD74HCT93E	-55 to 125	14 Ld PDIP

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

## CD74HC93, CD74HCT93

**TRUTH TABLE**

COUNT	OUTPUTS			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High Voltage Level, L = Low Voltage Level

**MODE SELECTION**

RESET OUTPUTS		OUTPUTS			
MR1	MR2	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
H	H	L	L	L	L
L	H	Count	Count	Count	Count
H	L				
L	L				

H = High Voltage Level, L = Low Voltage Level

## CD74HC93, CD74HCT93

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package .....	80
M (SOIC) Package .....	86
Maximum Junction Temperature .....	150 $^{\circ}C$
Maximum Storage Temperature Range .....	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	300 $^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range ( $T_A$ ) .....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

## CD74HC93, CD74HCT93

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
CP0, CP1	0.6
MR1, MR2	0.4

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

### Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>									
Maximum Clock Frequency	f <sub>MAX</sub>	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
Clock Pulse Width CP0, CP1	t <sub>w</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns

## CD74HC93, CD74HCT93

### Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS $V_{CC}$ (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS	
			MIN	MAX	MIN	MAX	MIN	MAX		
Reset Pulse Width	$t_W$	2	80	-	100	-	120	-	ns	
		4.5	16	-	20	-	24	-	ns	
		6	14	-	17	-	20	-	ns	
Reset Removal Time	$t_{REM}$	2	50	-	65	-	75	-	ns	
		4.5	10	-	13	-	15	-	ns	
		6	9	-	11	-	13	-	ns	
<b>HCT TYPES</b>										
Maximum Clock Frequency	$f_{MAX}$	4.5	30	-	24	-	20	-	mHz	
Clock Pulse Width CP0, CP1	$t_W$	4.5	16	-	20	-	24	-	ns	
Reset Pulse Width	$t_W$	4.5	16	-	20	-	24	-	ns	
Reset Removal Time	$t_{REM}$	4.5	10	-	13	-	15	-	ns	

### Switching Specifications Input $t_r, t_f = 6ns$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay Time $\overline{CP0}$ to Q0	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	2	-	-	125	-	155	-	190	ns
		$C_L = 50pF$	4.5	-	-	25	-	31	-	38	ns
		$C_L = 15pF$	5	-	10	-	-	-	-	-	ns
		$C_L = 50pF$	6	-	-	21	-	26	-	32	ns
$\overline{CP1}$ to Q1	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	2	-	-	135	-	170	-	205	ns
		$C_L = 50pF$	4.5	-	-	27	-	34	-	41	ns
		$C_L = 50pF$	6	-	-	23	-	29	-	35	ns
$\overline{CP1}$ to Q2	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	2	-	-	185	-	230	-	280	ns
		$C_L = 50pF$	4.5	-	-	37	-	46	-	56	ns
		$C_L = 50pF$	6	-	-	31	-	39	-	48	ns
$\overline{CP1}$ to Q3	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	2	-	-	245	-	305	-	370	ns
		$C_L = 50pF$	4.5	-	-	49	-	61	-	74	ns
		$C_L = 15pF$	5	-	21	-	-	-	-	-	ns
		$C_L = 50pF$	6	-	-	42	-	52	-	63	ns
MR1, MR2 to Qn	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	2	-	-	155	-	195	-	235	ns
		$C_L = 50pF$	4.5	-	-	31	-	39	-	47	ns
		$C_L = 15pF$	5	-	13	-	-	-	-	-	ns
		$C_L = 50pF$	6	-	-	26	-	33	-	40	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50pF$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_{IN}$	$C_L = 50pF$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}$	-	-	-	25	-	-	10	-	19	pF

# CD74HC93, CD74HCT93

## Switching Specifications Input $t_r$ , $t_f$ = 6ns (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>											
Propagation Delay Time $\overline{CP0}$ to Q0	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	4.5	-	-	34	-	43	-	51	ns
		$C_L = 15pF$	5	-	14	-	-	-	-	-	ns
$\overline{CP1}$ to Q1	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	4.5	-	-	34	-	43	-	51	ns
		$C_L = 15pF$	5	-	-	-	-	-	-	-	ns
$\overline{CP1}$ to Q2	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	4.5	-	-	46	-	58	-	69	ns
		$C_L = 15pF$	5	-	-	-	-	-	-	-	ns
$\overline{CP1}$ to Q3	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	4.5	-	-	58	-	73	-	87	ns
		$C_L = 15pF$	5	-	24	-	-	-	-	-	ns
MR1, MR2 to Qn	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	4.5	-	-	33	-	41	-	50	ns
		$C_L = 15pF$	5	-	13	-	-	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50pF$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	$C_{IN}$	$C_L = 50pF$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}$	-	-	-	25	-	-	-	-	-	pF

## Test Circuits and Waveforms

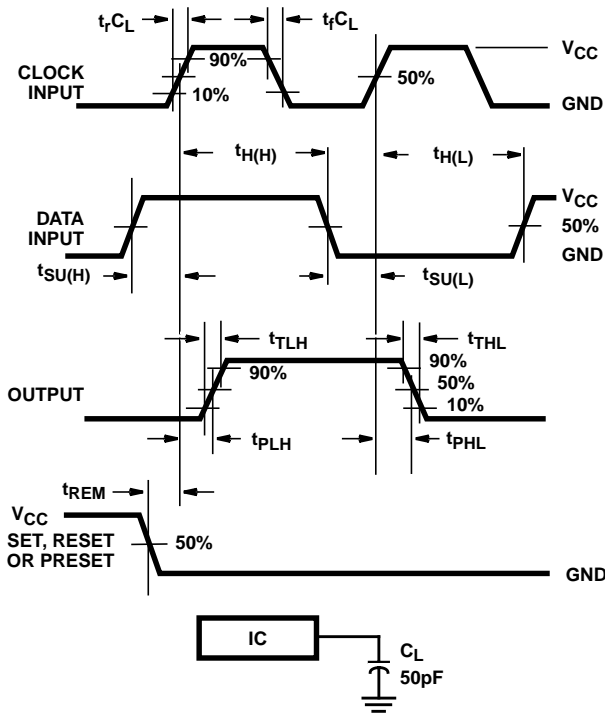


FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

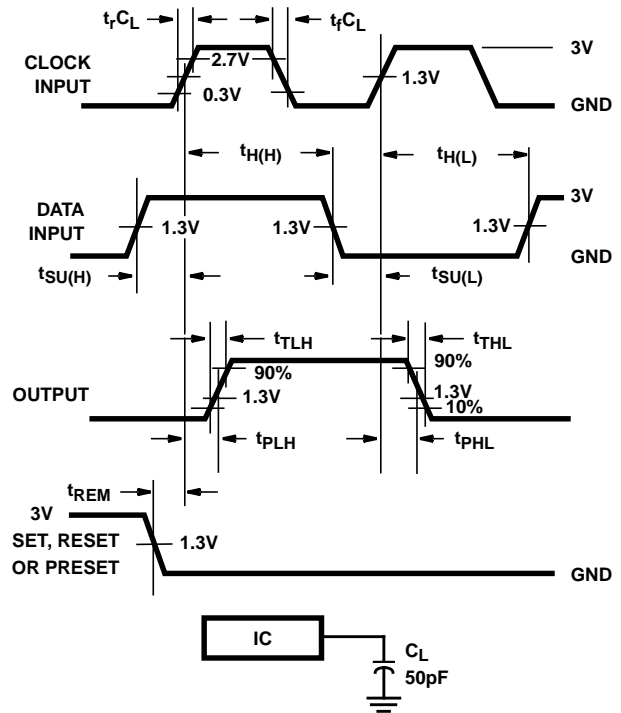


FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74HC93E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC93EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC93M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC93M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC93M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC93M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC93ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC93MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC93MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC93MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC93MTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT93E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT93EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

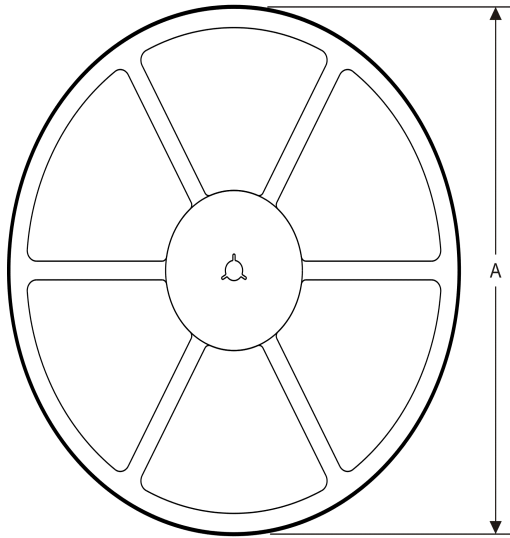
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC93M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC93MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC93M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC93MT	SOIC	D	14	250	367.0	367.0	38.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



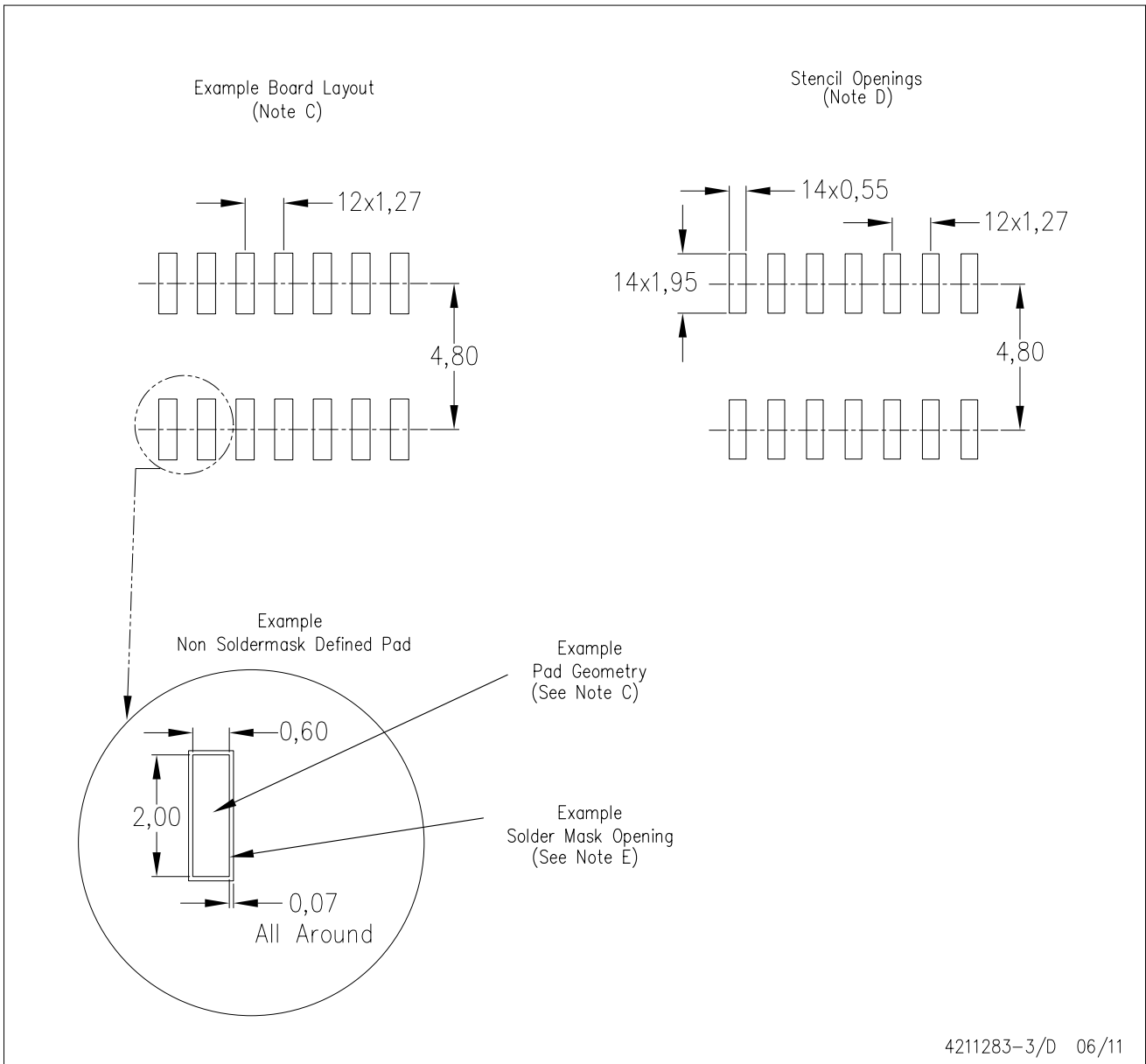
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/D 06/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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