

Features

- **Buffered Inputs and Outputs**
- **Four Operating Modes**
- **Typical Propagation Delay of 15ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$**
- **Fanout (Over Temperature Range)**
 - **Standard Outputs 10 LSTTL Loads**
 - **Bus Driver Outputs 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
 - **2V to 6V Operation**
 - **High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$**
- **HCT Types**
 - **4.5V to 5.5V Operation**
 - **Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)**
 - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}**

Description

The 'HC259 and 'HCT259 Addressable Latch features the low-power consumption associated with CMOS circuitry and has speeds comparable to low-power Schottky.

This latches three active modes and one reset mode. When both the Latch Enable (\overline{LE}) and Master Reset (\overline{MR}) inputs are low (8-line Demultiplexer mode) the output of the addressed latch follows the Data input and all other outputs are forced low. When both \overline{MR} and \overline{LE} are high (Memory Mode), all outputs are isolated from the Data input, i.e., all latches hold the last data presented before the \overline{LE} transition from low to high. A condition of \overline{LE} low and \overline{MR} high (Addressable Latch mode) allows the addressed latch's output to follow the data input; all other latches are unaffected. The Reset mode (all outputs low) results when \overline{LE} is high and \overline{MR} is low.

Ordering Information

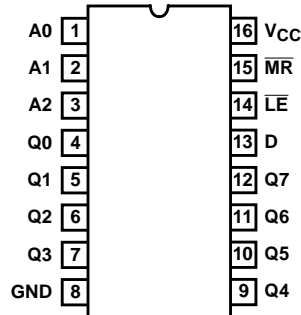
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---------------|------------------|--------------|
| CD54HC259F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT259F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC259E | -55 to 125 | 16 Ld PDIP |
| CD74HC259M | -55 to 125 | 16 Ld SOIC |
| CD74HC259MT | -55 to 125 | 16 Ld SOIC |
| CD74HC259M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT259E | -55 to 125 | 16 Ld PDIP |
| CD74HCT259M | -55 to 125 | 16 Ld SOIC |
| CD74HCT259MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT259M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

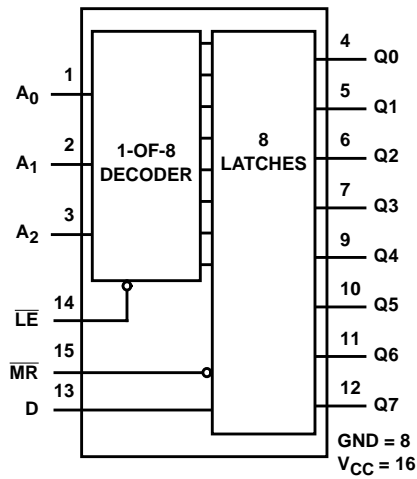
CD54HC259, CD74HC259, CD54HCT259, CD74HCT259

Pinout

CD54HC259, CD54HCT259
(CERDIP)
CD74HC259, CD74HCT259
(PDIP, SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

| INPUTS | | OUTPUT OF ADDRESS LATCH | EACH OTHER OUTPUT | FUNCTION |
|-----------------|-----------------|-------------------------|-------------------|----------------------|
| \overline{MR} | \overline{LE} | | | |
| H | L | D | Q_{i0} | Addressable Latch |
| H | H | Q_{i0} | Q_{i0} | Memory |
| L | L | D | L | 8-Line Demultiplexer |
| L | H | L | L | Reset |

LATCH SELECTION TABLE

| SELECT INPUTS | | | LATCH ADDRESSED |
|---------------|----|----|-----------------|
| A2 | A1 | A0 | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

H = High Voltage Level

L = Low Voltage Level

D = The level at the data input

Q_{i0} = The level of Q_i ($i = 0, 1...7$, as appropriate) before the indicated steady-state input conditions were established.

CD54HC259, CD74HC259, CD54HCT259, CD74HCT259

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Drain Current, per Output, I_O | |
| For $-0.5V < V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} | $\pm 50mA$ |

Thermal Information

| | |
|--|--|
| Thermal Resistance (Typical, Note 1) | θ_{JA} ($^{\circ}C/W$) |
| E (PDIP) Package | 67 |
| M (SOIC) Package | 73 |
| Maximum Junction Temperature | 150 $^{\circ}C$ |
| Maximum Storage Temperature Range | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$ (SOIC - Lead Tips Only) |

Operating Conditions

| | |
|--|------------------------------------|
| Temperature Range, T_A | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25 $^{\circ}C$ | | | -40 $^{\circ}C$ TO 85 $^{\circ}C$ | | -55 $^{\circ}C$ TO 125 $^{\circ}C$ | | UNITS | |
|---|----------|----------------------|------------|--------------|----------------|------|-----------|-----------------------------------|---------|------------------------------------|---------|---------|---|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| HC TYPES | | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V | |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V | |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V | |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V | |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V | |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V | |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V | |
| | | | | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V | |
| | | | | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V | |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V | |
| | | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V | |
| | | | | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V | |
| | | | | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V | |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V | |
| | | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA | |

CD54HC259, CD74HC259, CD54HCT259, CD74HCT259

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 2) | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|--------------------------|------------|
| A0 - A2, \overline{LE} | 1.5 |
| D | 1.2 |
| MR | 0.75 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Prerequisite for Switching Specifications

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|--------------------------------|-----------------|---------------------|------|-----|-----|---------------|-----|-----|----------------|-----|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| HC TYPES | | | | | | | | | | | | |
| Pulse Width \overline{LE} | t _{WL} | 2 | 70 | - | - | 90 | - | - | 105 | - | - | ns |
| | | 4.5 | 14 | - | - | 18 | - | - | 21 | - | - | ns |
| | | 6 | 12 | - | - | 15 | - | - | 18 | - | - | ns |

CD54HC259, CD74HC259, CD54HCT259, CD74HCT259

Prerequisite for Switching Specifications (Continued)

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|--|-----------------|---------------------|------|-----|-----|---------------|-----|-----|----------------|-----|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| MR | t _{WL} | 2 | 70 | - | - | 90 | - | - | 105 | - | - | ns |
| | | 4.5 | 14 | - | - | 18 | - | - | 21 | - | - | ns |
| | | 6 | 12 | - | - | 15 | - | - | 18 | - | - | ns |
| Setup Time D to \overline{LE} A to \overline{LE} | t _{SU} | 2 | 80 | - | - | 100 | - | - | 120 | - | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | - | 24 | - | - | ns |
| | | 6 | 14 | - | - | 17 | - | - | 20 | - | - | ns |
| Hold Time D to \overline{LE} A to \overline{LE} | t _H | 2 | 0 | - | - | 0 | - | - | 0 | - | - | ns |
| | | 4.5 | 0 | - | - | 0 | - | - | 0 | - | - | ns |
| | | 6 | 0 | - | - | 0 | - | - | 0 | - | - | ns |
| HCT TYPES | | | | | | | | | | | | |
| Pulse Width \overline{LE} MR | t _{WL} | 4.5 | 18 | - | - | 23 | - | - | 27 | - | - | ns |
| Setup Time D to \overline{LE} A to \overline{LE} | t _{SU} | 4.5 | 17 | - | - | 21 | - | - | 26 | - | - | ns |
| Hold Time D to \overline{LE} A to \overline{LE} | t _H | 4.5 | 0 | - | - | 0 | - | - | 0 | - | - | ns |

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|-----------------------------|------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay D to Q | t _{PHL} | C _L = 50pF | 2 | - | - | 185 | - | 230 | - | 280 | ns |
| | | | 4.5 | - | - | 37 | - | 46 | - | 56 | ns |
| | | C _L = 15pF | 5 | - | 15 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 31 | - | 39 | - | 48 | ns |
| \overline{LE} to Q | t _{PHL} | C _L = 50pF | 2 | - | - | 170 | - | 215 | - | 255 | ns |
| | | | 4.5 | - | - | 34 | - | 43 | - | 51 | ns |
| | | C _L = 15pF | 5 | - | 14 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 29 | - | 37 | - | 43 | ns |

CD54HC259, CD74HC259, CD54HCT259, CD74HCT259

Switching Specifications $C_L = 50\text{pF}$, Input t_r , $t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|--------------------|---------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| A to Q | t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | - | 185 | - | 230 | - | 280 | ns |
| | | | 4.5 | - | - | 37 | - | 46 | - | 56 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 15 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | - | 31 | - | 39 | - | 48 | ns |
| \overline{MR} to Q | t_{PHL}, t_{PLH} | $C_L = 50\text{pF}$ | 2 | - | - | 155 | - | 195 | - | 235 | ns |
| | | | 4.5 | - | - | 31 | - | 39 | - | 47 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 13 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | - | 26 | - | 33 | - | 40 | ns |
| Output Transition Time | t_{THL}, t_{TLH} | $C_L = 50\text{pF}$ | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Power Dissipation Capacitance (Notes 3, 4) | C_{PD} | $C_L = 15\text{pF}$ | 5 | - | 21 | - | - | - | - | - | pF |
| Input Capacitance | C_I | $C_L = 50\text{pF}$ | - | 10 | - | 10 | - | 10 | - | 10 | pF |
| HCT TYPES | | | | | | | | | | | |
| Propagation Delay D to Q | t_{PHL}, t_{PLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 39 | - | 49 | - | 59 | ns |
| | | | $C_L = 15\text{pF}$ | 5 | - | 16 | - | - | - | - | - |
| \overline{LE} to Q | t_{PHL}, t_{PLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | | | $C_L = 15\text{pF}$ | 5 | - | 16 | - | - | - | - | - |
| A to Q | t_{PHL}, t_{PLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 41 | - | 51 | - | 61 | ns |
| | | | $C_L = 15\text{pF}$ | 5 | - | 17 | - | - | - | - | - |
| \overline{MR} to Q | t_{PHL}, t_{PLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 39 | - | 49 | - | 59 | ns |
| | | | $C_L = 15\text{pF}$ | 5 | - | 16 | - | - | - | - | - |
| Power Dissipation Capacitance (Notes 3, 4) | C_{PD} | $C_L = 15\text{pF}$ | 5 | - | 22 | - | - | - | - | - | pF |
| Input Capacitance | C_I | $C_L = 50\text{pF}$ | - | 10 | - | 10 | - | 10 | - | 10 | pF |
| Output Transition Time | t_{THL}, t_{TLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |

NOTES:

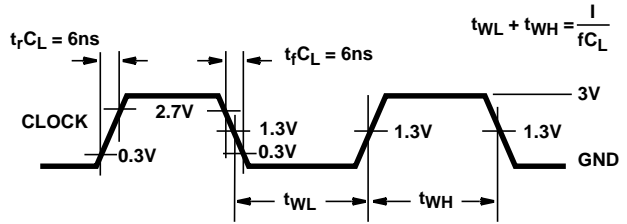
- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_O$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

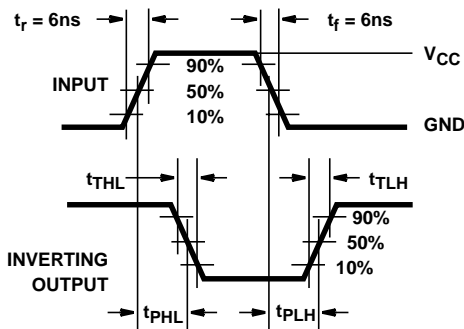


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

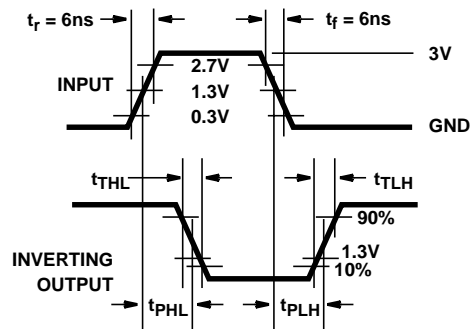


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

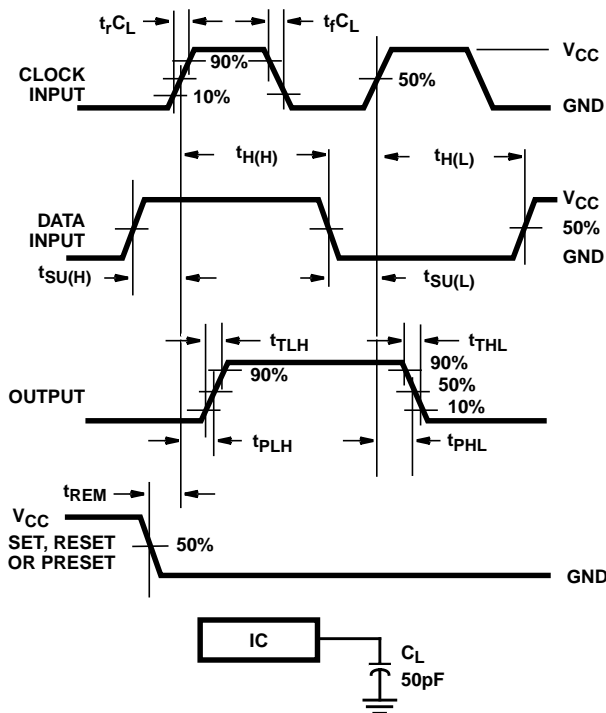


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

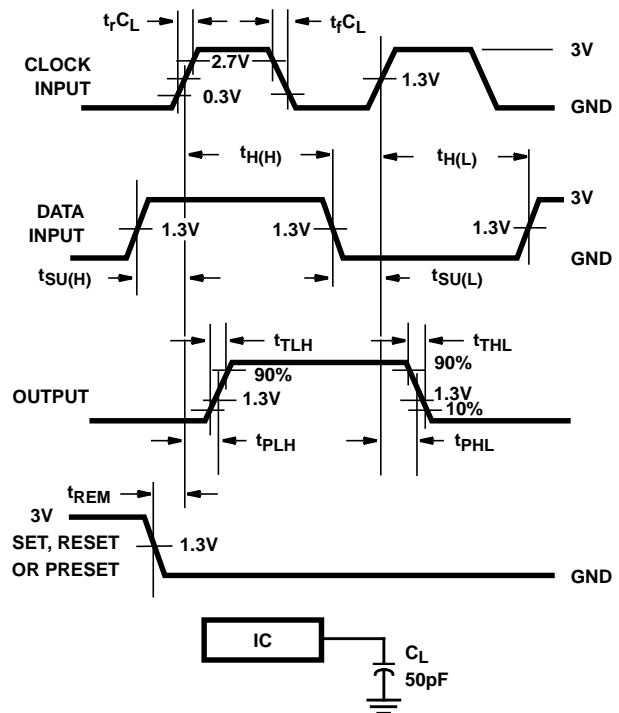


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

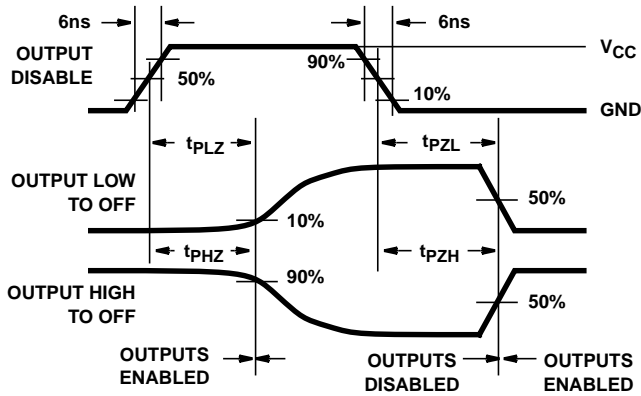


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

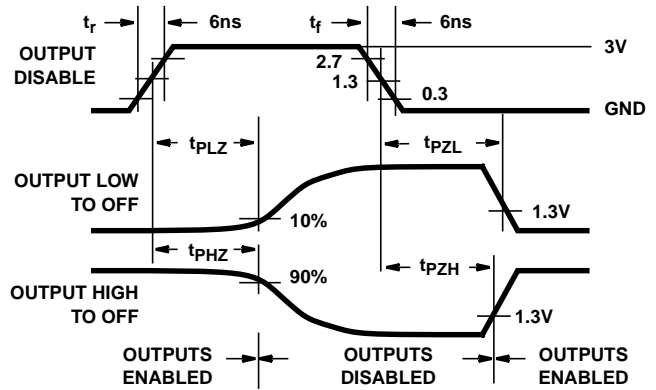
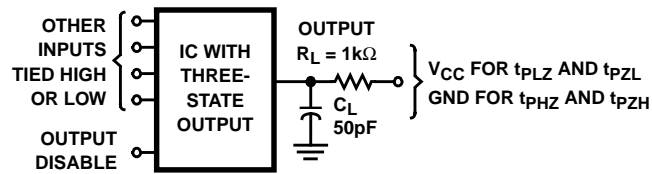


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZH} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-8985201EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD54HC259F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD54HCT259F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD74HC259E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC259EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC259M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC259M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC259M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC259M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC259ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC259MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC259MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC259MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC259MTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT259EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT259M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT259MTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC259M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT259M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC259M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HCT259M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

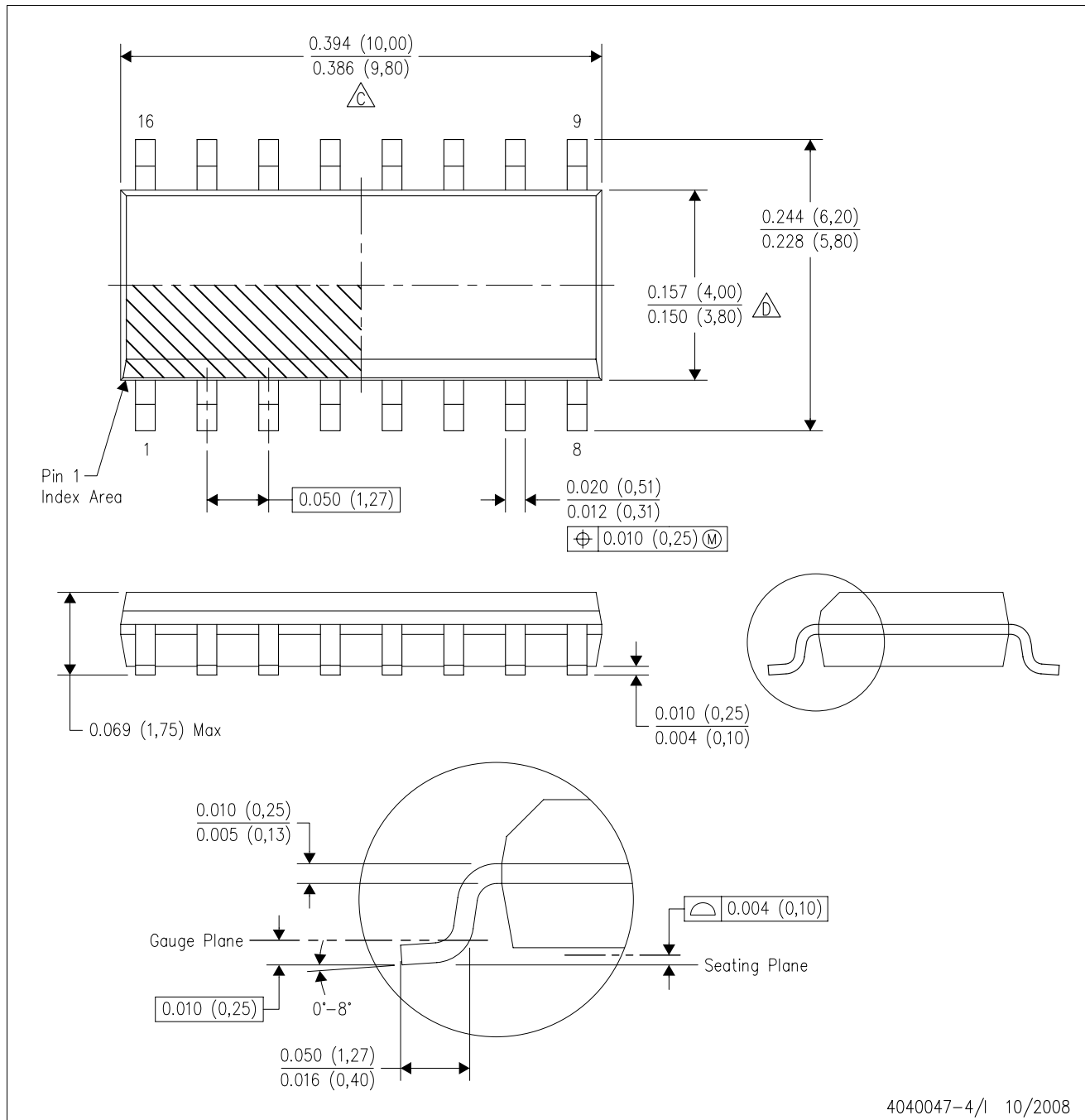


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

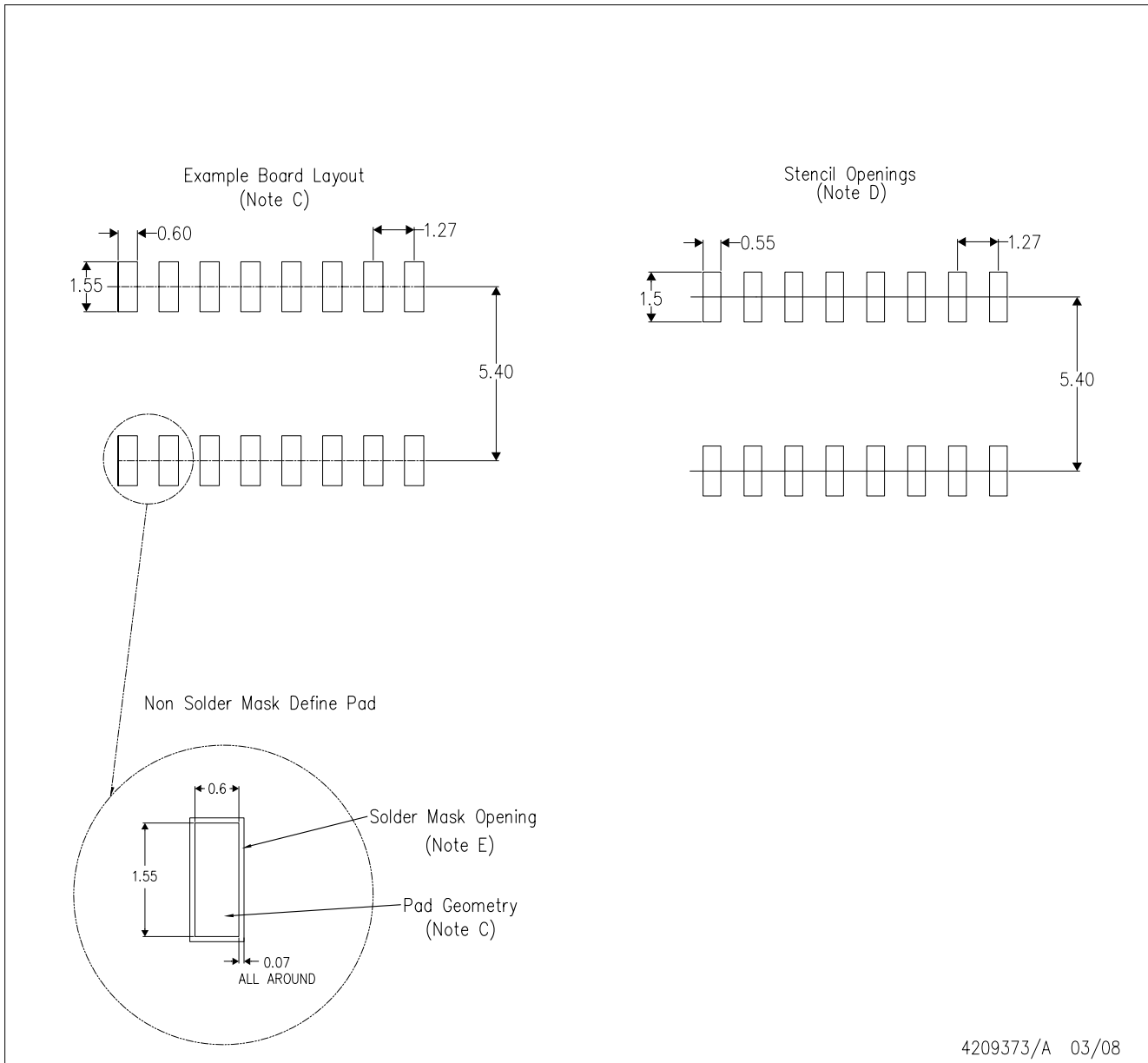
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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