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Jameco Part Number 823963

### Features

- Selects One of Eight Binary Data Inputs
- Three-State Output Capability
- True and Complement Outputs
- Typical (Data to Output) Propagation Delay of 14ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC251 and 'HCT251 are 8-channel digital multiplexers with three-state outputs, fabricated with high-speed silicon-gate CMOS technology. Together with the low power consumption of standard CMOS integrated circuits, they possess the ability to drive 10 LSTTL loads. The three-state feature makes them ideally suited for interfacing with bus lines in a bus-oriented system.

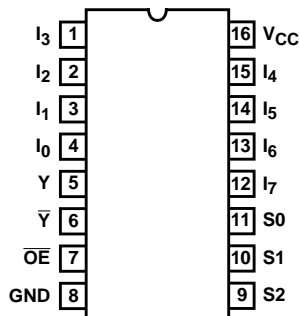
This multiplexer features both true (Y) and complement ( $\bar{Y}$ ) outputs as well as an output enable ( $\bar{OE}$ ) input. The  $\bar{OE}$  must be at a low logic level to enable this device. When the  $\bar{OE}$  input is high, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and  $\bar{Y}$  outputs. The 'HCT251 logic family is speed, function, and pin-compatible with the standard 'LS251.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC251F3A	-55 to 125	16 Ld CERDIP
CD54HCT251F3A	-55 to 125	16 Ld CERDIP
CD74HC251E	-55 to 125	16 Ld PDIP
CD74HC251M	-55 to 125	16 Ld SOIC
CD74HC251MT	-55 to 125	16 Ld SOIC
CD74HC251M96	-55 to 125	16 Ld SOIC
CD74HCT251E	-55 to 125	16 Ld PDIP
CD74HCT251M	-55 to 125	16 Ld SOIC
CD74HCT251MT	-55 to 125	16 Ld SOIC
CD74HCT251M96	-55 to 125	16 Ld SOIC

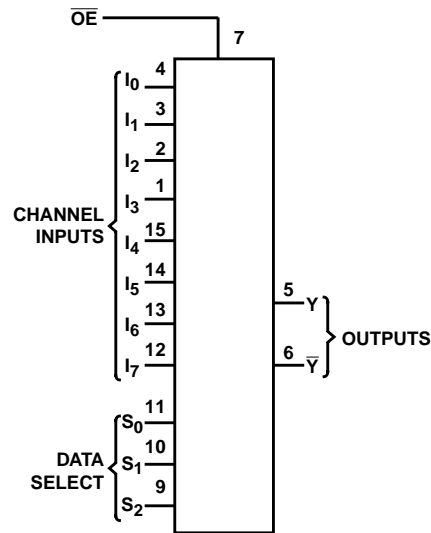
### Pinout

CD54HC251, CD54HCT251  
(CERDIP)  
CD74HC251, CD74HCT251  
(PDIP, SOIC)  
TOP VIEW



NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

**Functional Diagram**



**TRUTH TABLE**

INPUTS			OUTPUT		
SELECT			OUTPUT CONTROL $\overline{OE}$	Y	$\overline{Y}$
S2	S1	S0			
X	X	X	H	Z	Z
L	L	L	L	$I_0$	$\overline{I_0}$
L	L	H	L	$I_1$	$\overline{I_1}$
L	H	L	L	$I_2$	$\overline{I_2}$
L	H	H	L	$I_3$	$\overline{I_3}$
H	L	L	L	$I_4$	$\overline{I_4}$
H	L	H	L	$I_5$	$\overline{I_5}$
H	H	L	L	$I_6$	$\overline{I_6}$
H	H	H	L	$I_7$	$\overline{I_7}$

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, Z = High Impedance (Off),  $I_0, I_1 \dots I_7$  = the level of the respective input.

# CD54HC251, CD74HC251, CD54HCT251, CD74HCT251

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package .....	67
M (SOIC) Package .....	73
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

**CD54HC251, CD74HC251, CD54HCT251, CD74HCT251**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
Three-State Leakage Current	-	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	6	-	-	±0.5	-	±5.0	-	±10	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Three-State Leakage Current	-	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	6	-	-	±0.5	-	±5.0	-	±10	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
S0, S1, S2	0.55
I0 - I7	0.5
OE	2.65

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**CD54HC251, CD74HC251, CD54HCT251, CD74HCT251**

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay Select to Outputs	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	245	-	305	-	370	ns
			4.5	-	-	49	-	61	-	74	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	42	-	52	-	63	ns
Data to Outputs	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	12	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	30	-	37	-	45	ns
Enable to High Z and Enable from High Z	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	140	-	175	-	210	ns
			4.5	-	-	28	-	35	-	42	ns
		$C_L = 15\text{pF}$	5	-	11	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	24	-	30	-	36	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_{IN}$	-	-	-	10	-	10	-	10	pF	
Three-State Output Capacitance	$C_O$	-	-	-	15	-	15	-	15	pF	
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	-	60	-	-	-	-	pF	
<b>HCT TYPES</b>											
Propagation Delay Select to Outputs	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
Data to Outputs	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	12	-	-	-	-	-	ns
Enable to High Z and Enable from High Z	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	30	-	38	-	45	ns
		$C_L = 15\text{pF}$	5	-	12	-	-	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	$C_{IN}$	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	-	60	-	-	-	-	pF	

NOTES:

- $C_{PD}$  is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

Test Circuits and Waveforms

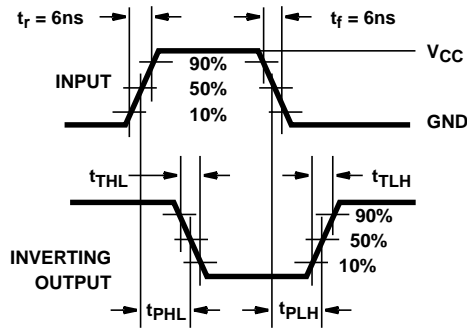


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

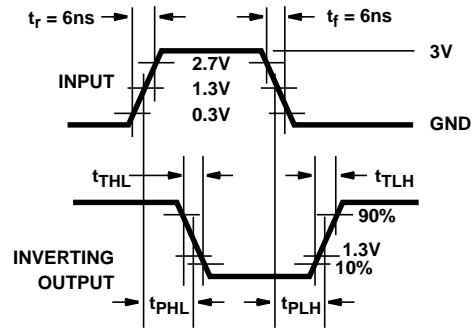


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

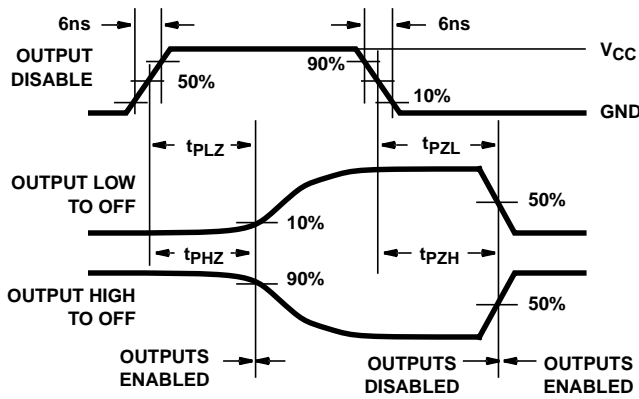


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

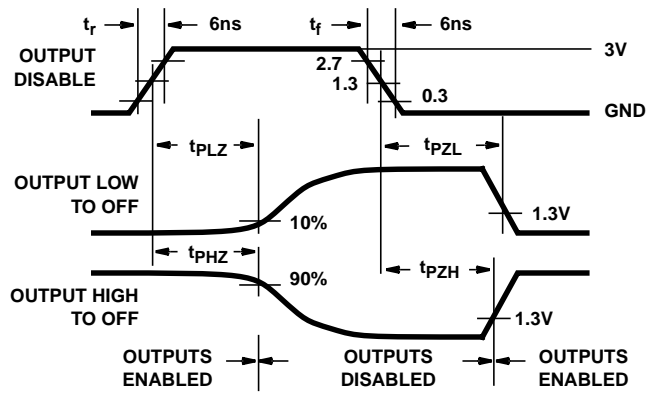


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$   $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9052401MEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC251F	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC251F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HCT251F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC251E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC251EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC251M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC251M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC251M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC251ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC251MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC251MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT251E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT251EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT251M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT251M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT251M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT251ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT251MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT251MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265