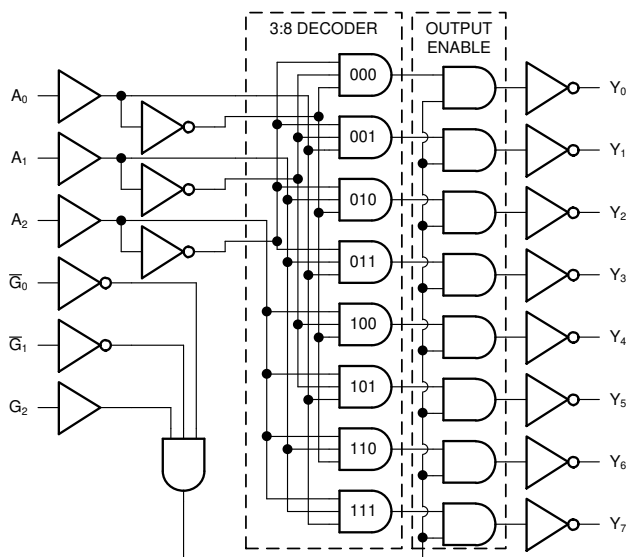


CDx4HC138、CDx4HCT138、CDx4HC238、CDx4HCT238 高速 CMOS 逻辑 3 线至 8 线解码器/多路解复用器（反向和同向）

1 特性

- 选择一个数据输出（共八个）：
 - 针对 '138 的低电平有效
 - 针对 '238 的高电平有效
- I/O 端口或存储器选择器
- 三个使能输入以简化级联
- 当 $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$ 时的传播延迟典型值为 13ns
- 扇出（在温度范围内）
 - 总线驱动器输出：15 个 LSTTL 负载
 - 标准输出：10 个 LSTTL 负载
- 宽工作温度范围：-55°C 至 125°C
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗
- HC 类型
 - 工作电压为 2V 至 6V
 - 高抗噪性：当 $V_{CC} = 5V$ 时， $N_{IL} = 30\%$, $N_{IH} = V_{CC}$ 的 30%
- HCT 类型
 - 4.5V 至 5.5V 工作电压
 - 直接 LSTTL 输入逻辑兼容性， $V_{IL} = 0.8V$ （最大值）， $V_{IH} = 2V$ （最小值）
 - CMOS 输入兼容性，当电压为 V_{OL} 、 V_{OH} 时， $I_I \leq 1\mu A$



功能框图 '138

2 说明

CDx4HC(T)138 和 '238 是 3 线至 8 线解码器，具有一个标准输出选通 (G_2) 和两个低电平有效的输出选通 (\bar{G}_1 和 \bar{G}_0)。当输出受到任何选通输入控制时，这些输出全都强制进入高电平状态。当选通输入未禁用输出时，只有选定输出为低电平，而所有其他输出为高电平。

CDx4HC(T)238 是 3 线至 8 线解码器，具有一个标准输出选通 (G_2) 和两个低电平有效的输出选通 (\bar{G}_1 和 \bar{G}_0)。当输出受到任何选通输入控制时，这些输出全都强制进入低电平状态。当选通输入未禁用输出时，只有选定输出为高电平，而所有其他输出为低电平。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
CD74HC138E	PDIP (16)	25.40mm × 6.35mm
CD74HCT138E	PDIP (16)	25.40mm × 6.35mm
CD74HCT238E	PDIP (16)	25.40mm × 6.35mm
CD74HC138M	SOIC (16)	9.90mm × 3.90mm
CD74HCT238M	SOIC (16)	9.90mm × 3.90mm
CD74HC238NS	SO (16)	10.20mm × 5.30mm
CD74HC238PW	TSSOP (16)	5.00mm × 4.40mm
CD74HCT238PW	TSSOP (16)	5.00mm × 4.40mm
CD54HC138F	陶瓷双列直插封装 (CDIP) (16)	21.34mm × 6.92mm
CD54HCT138F	陶瓷双列直插封装 (CDIP) (16)	21.34mm × 6.92mm
CD54HCT238F	陶瓷双列直插封装 (CDIP) (16)	21.34mm × 6.92mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



Table of Contents

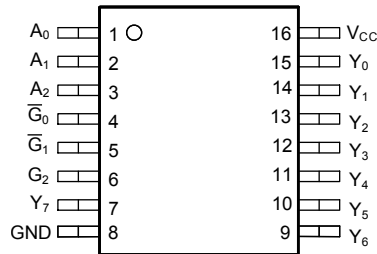
1 特性	1	7.3 Device Functional Modes.....	10
2 说明	1	8 Power Supply Recommendations	11
3 Revision History	2	9 Layout	11
4 Pin Configuration and Functions	3	9.1 Layout Guidelines.....	11
5 Specifications	4	10 Device and Documentation Support	12
5.1 Absolute Maximum Ratings.....	4	10.1 Documentation Support.....	12
5.2 Recommended Operating Conditions.....	4	10.2 接收文档更新通知.....	12
5.3 Thermal Information.....	4	10.3 支持资源.....	12
5.4 Electrical Characteristics.....	5	10.4 Trademarks.....	12
5.5 Switching Characteristics ⁽²⁾	6	10.5 Electrostatic Discharge Caution.....	12
6 Parameter Measurement Information	7	10.6 Glossary.....	12
7 Detailed Description	8	11 Mechanical, Packaging, and Orderable Information	12
7.1 Overview.....	8		
7.2 Functional Block Diagram.....	8		

3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (August 2004) to Revision J (November 2021)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....	1
• 更新了引脚名称，以符合现行的 TI 命名约定 E ₃ 现在是 G ₂ ，E ₂ 现在是 G ₁ ，E ₁ 现在是 G ₀	1

4 Pin Configuration and Functions



J, N, D, NS, or PW package
16-Pin CDIP, PDIP, SOIC, SO, or TSSOP
Top View

Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
SOIC or TSSOP NO.	NAME		
1	A ₀	I	Address select 0
2	A ₁	I	Address select 1
3	A ₂	I	Address select 2
4	\overline{G}_0	I	Output strobe 0, active low
5	\overline{G}_1	I	Output strobe 1, active low
6	G ₂	I	Output strobe 2
7	Y ₇	O	Output 7
8	GND	—	Ground
9	Y ₆	O	Output 6
10	Y ₅	O	Output 5
11	Y ₄	O	Output 4
12	Y ₃	O	Output 3
13	Y ₂	O	Output 2
14	Y ₁	O	Output 1
15	Y ₀	O	Output 0
16	V _{CC}	—	Positive supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
I _{IK}	Input clamp diode current	For V _I < 0.5V or V _I > V _{CC} + 0.5V		±20 mA
I _{OK}	Output clamp diode current	For V _O < -0.5V or V _O > V _{CC} + 0.5V		±20 mA
I _O	Output source or sink current per output pin	For V _O > -0.5V or V _O < V _{CC} + 0.5V		±25 mA
	Continuous current through V _{CC} or GND			±50 mA
T _J	Junction temperature			150 °C
T _{stg}	Storage temperature range	-65	150	°C
	Lead temperature (Soldering 10s) (SOIC - Lead Tips Only)			300 °C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V _I	Input voltage	0	V _{CC}	V	
V _O	Output voltage	0	V _{CC}	V	
t _t	Input rise and fall time	V _{CC} = 2V	1000		ns
		V _{CC} = 4.5V	500		
		V _{CC} = 6V	400		
T _A	Temperature range	-55	125	°C	

5.3 Thermal Information

THERMAL METRIC		CD74HC(T)138, CD74HC(T)238				UNIT
		N (PDIP)	D (SOIC)	NS (SOP)	PW (TSSOP)	
		16 Pins	16 Pins	16 Pins	16 Pins	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	67	73	64	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER	TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TYPES											
V _{IH}	High-level input voltage		2	1.5		1.5		1.5		V	
			4.5	3.15		3.15		3.15		V	
			6	4.2		4.2		4.2		V	
V _{IL}	Low-level input voltage		2		0.5		0.5		0.5	V	
			4.5		1.35		1.35		1.35	V	
			6		1.8		1.8		1.8	V	
V _{OH}	High-level output voltage	I _{OH} = - 20 μA	2	1.9		1.9		1.9		V	
		I _{OH} = - 20 μA	4.5	4.4		4.4		4.4		V	
		I _{OH} = - 20 μA	6	5.9		5.9		5.9		V	
	High-level output voltage	I _{OH} = - 4 mA	4.5	3.98		3.84		3.7		V	
		I _{OH} = - 5.2 mA	6	5.48		5.34		5.2		V	
V _{OL}	Low-level output voltage	I _{OL} = 20 μA	2		0.1		0.1		0.1	V	
		I _{OL} = 20 μA	4.5		0.1		0.1		0.1	V	
		I _{OL} = 20 μA	6		0.1		0.1		0.1	V	
	Low-level output voltage	I _{OL} = 4 mA	4.5		0.26		0.33		0.4	V	
		I _{OL} = 5.2 mA	6		0.26		0.33		0.4	V	
I _I	Input leakage current	V _I = V _{CC} or GND	6		±0.1		±1		±1	μA	
I _{CC}	Supply current	V _I = V _{CC} or GND	6		8		80		160	μA	
HCT TYPES											
V _{IH}	High-level input voltage		4.5 to 5.5	2		2		2		V	
V _{IL}	Low-level input voltage		4.5 to 5.5		0.8		0.8		0.8	V	
V _{OH}	High-level output voltage	I _{OH} = - 20 μA	4.5	4.4		4.4		4.4		V	
	High-level output voltage	I _{OH} = - 4 mA	4.5	3.98		3.84		3.7		V	
V _{OL}	Low-level output voltage	I _{OL} = 20 μA	4.5		0.1		0.1		0.1	V	
	Low-level output voltage	I _{OH} = 4 mA	4.5		0.26		0.33		0.4	V	
I _I	Input leakage current	V _I = V _{CC} and GND	5.5		±0.1		±1		±1	μA	
I _{CC}	Supply current	V _I = V _{CC} and GND	5.5		8		80		160	μA	
ΔI _{CC}	Additional supply current per input pin	A ₀ - A ₂ inputs held at V _{CC} - 2.1 V	4.5 to 5.5		100	540		675		735	μA
		\overline{G}_0 and \overline{G}_1 inputs held at V _{CC} - 2.1 V	4.5 to 5.5		100	450		562.5		612.5	μA
		G ₂ input held at V _{CC} - 2.1 V	4.5 to 5.5		100	360		450		490	μA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics⁽²⁾

Input $t_f = 6\text{ns}$. (See [Parameter Measurement Information](#))

PARAMETER	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_{pd}	Address to output	$C_L = 50\text{pF}$	2		150		190		225	ns
			4.5	13 ⁽³⁾	30		38		45	
			6		26		33		38	
	Strobe $\overline{G}_0, \overline{G}_1, G_2$ to output HC/HCT 138	$C_L = 50\text{pF}$	2		150		190		265	ns
			4.5		30		38		53	
			6		26		33		45	
t_t	Output transition time	$C_L = 50\text{pF}$	2		75		95		110	MHz
			4.5		15		19		22	
			6		13		16		19	
C_{pd}	Power dissipation capacitance ⁽¹⁾	$C_L = 15\text{pF}$	5	67					pF	
C_i	Input capacitance				10		10		10	pF
HCT TYPES										
t_{pd}	Address to output	$C_L = 50\text{pF}$	4.5	14 ⁽³⁾	35		44		53	ns
	Strobe G_2 to output HC/HCT138	$C_L = 50\text{pF}$	4.5		35		44		53	ns
	Strobe $\overline{G}_0, \overline{G}_1$ to output HC/HCT238	$C_L = 15\text{pF}$	4.5		40		50		60	ns
t_t	Output transition time	$C_L = 15\text{pF}$	4.5		15		19		22	
C_{pd}	Power dissipation capacitance ⁽¹⁾	$C_L = 15\text{pF}$	5	67						pF
C_i	Input capacitance				10		10		10	pF

(1) C_{PD} is used to determine the dynamic power consumption, per gate.

(2) For details on power calculation, see [SCAA035B](#)

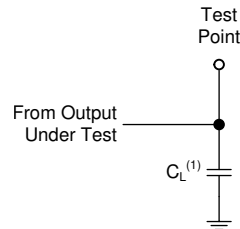
(3) $C_L = 15\text{pF}$ and $V_{CC} = 5$

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

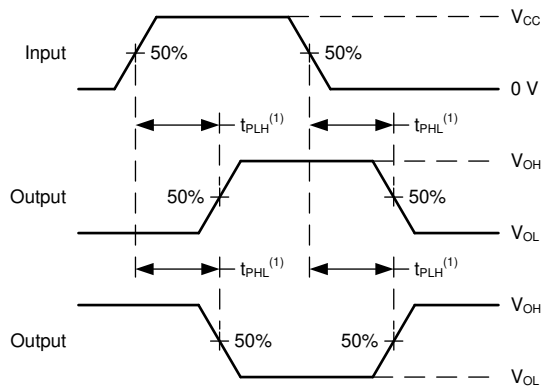
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



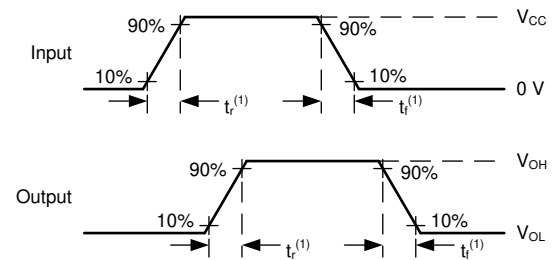
(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs



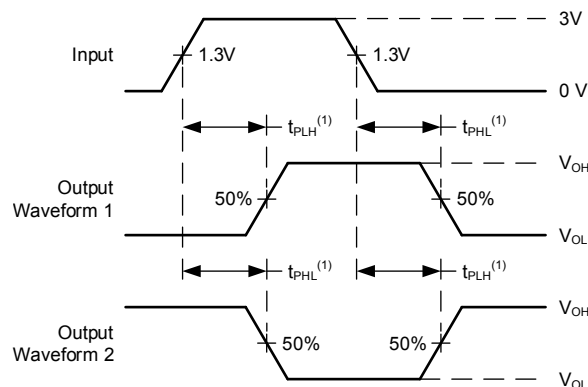
(1) The greater between t_{pLH} and t_{pHL} is the same as t_{pd} .

图 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

图 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{pLH} and t_{pHL} is the same as t_{pd} .

图 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

The CDx4HC(T)138 and '238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. They contain a single 3:8 decoder.

The CDx4HC(T)138 and '238 have three address select inputs (A_2 , A_1 , and A_0). The circuit functions as a normal one-of-eight decoder.

Three strobe inputs (G_2 , \bar{G}_1 and \bar{G}_0) are provided to simplify cascading and to facilitate demultiplexing. When any input strobe is active, all outputs are forced into the high state for the '138 function. When any input strobe is active, all outputs are forced into the low state for the '238 function.

The demultiplexing function is accomplished by first using the select inputs to choose the desired output, and then using one of the strobe inputs as the data input.

The outputs for the CDx4HC(T)138 are normally low when selected. The outputs for the CDxHC(T)238 are normally high when selected.

7.2 Functional Block Diagram

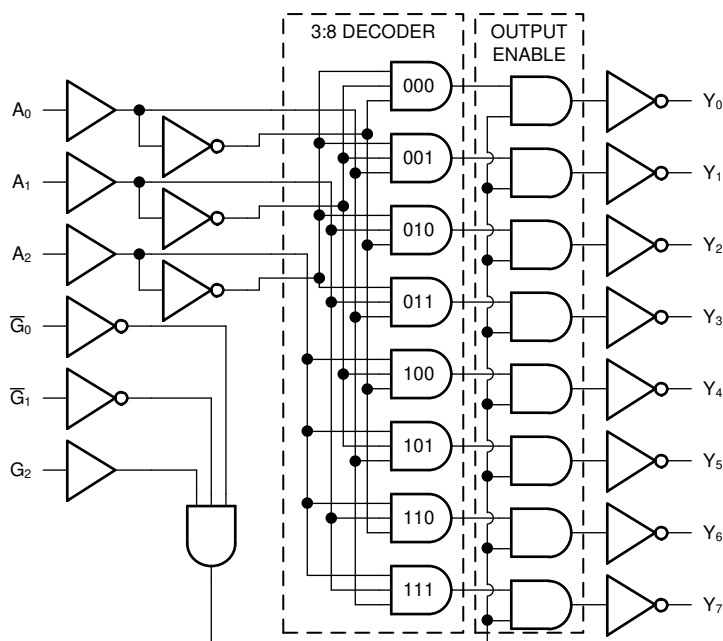


图 7-1. Functional Block Diagram '138

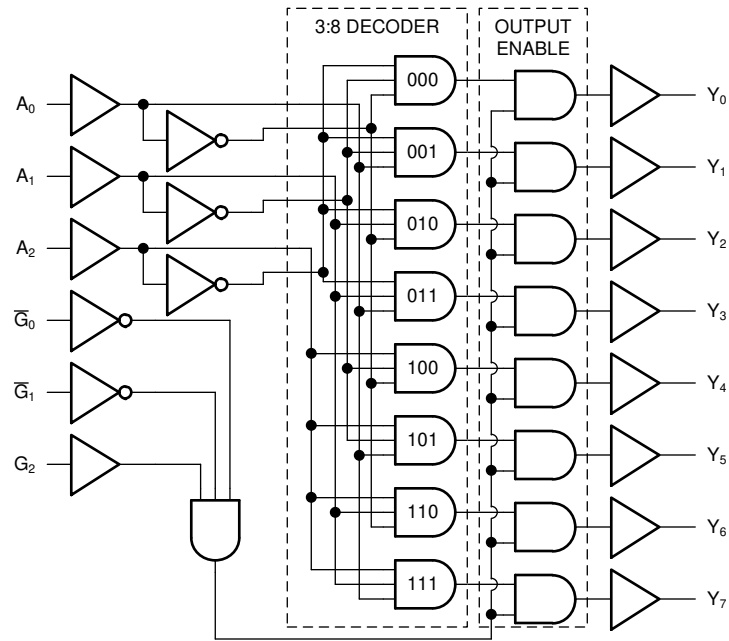


图 7-2. Functional Block Diagram '238

7.3 Device Functional Modes

表 7-1. Function Table 'HC138, 'HCT138

INPUTS						OUTPUTS							
STROBE			ADDRESS										
G2	$\overline{G1}$	$\overline{G0}$	A ₂	A ₁	A ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

表 7-2. Function Table 'HC238, 'HCT238

INPUTS						OUTPUTS							
STROBE			ADDRESS										
G2	$\overline{G1}$	$\overline{G0}$	A ₂	A ₁	A ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8688401EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688401EA CD54HC238F3A	Samples
CD54HC138F	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC138F	Samples
CD54HC138F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8406201EA CD54HC138F3A	Samples
CD54HC238F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688401EA CD54HC238F3A	Samples
CD54HCT138F	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT138F	Samples
CD54HCT138F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8550401EA CD54HCT138F3A	Samples
CD54HCT238F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8974501EA CD54HCT238F3A	Samples
CD74HC138E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC138E	Samples
CD74HC138EE4	ACTIVE	PDIP	N	16	25	TBD	Call TI	Call TI	-55 to 125		Samples
CD74HC138M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC138M	Samples
CD74HC138M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC138M	Samples
CD74HC138M96E4	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-55 to 125		Samples
CD74HC138ME4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC138M	Samples
CD74HC138MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC138M	Samples
CD74HC138MTG4	ACTIVE	SOIC	D	16	250	TBD	Call TI	Call TI	-55 to 125		Samples
CD74HC238E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC238E	Samples
CD74HC238EE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC238E	Samples
CD74HC238M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC238M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC238M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC238M	Samples
CD74HC238M96E4	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-55 to 125		Samples
CD74HC238MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC238M	Samples
CD74HC238NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC238M	Samples
CD74HC238PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ238	Samples
CD74HC238PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HJ238	Samples
CD74HC238PWRE4	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-55 to 125		Samples
CD74HC238PWRG4	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-55 to 125		Samples
CD74HC238PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ238	Samples
CD74HCT138E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT138E	Samples
CD74HCT138M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT138M	Samples
CD74HCT138M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT138M	Samples
CD74HCT138M96G4	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-55 to 125		Samples
CD74HCT238E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT238E	Samples
CD74HCT238M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT238M	Samples
CD74HCT238M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT238M	Samples
CD74HCT238M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT238M	Samples
CD74HCT238PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK238	Samples
CD74HCT238PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK238	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC138, CD54HC238, CD54HCT138, CD54HCT238, CD74HC138, CD74HC238, CD74HCT138, CD74HCT238 :

- Catalog : [CD74HC138](#), [CD74HC238](#), [CD74HCT138](#), [CD74HCT238](#)
- Automotive : [CD74HC138-Q1](#), [CD74HC138-Q1](#)
- Military : [CD54HC138](#), [CD54HC238](#), [CD54HCT138](#), [CD54HCT238](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

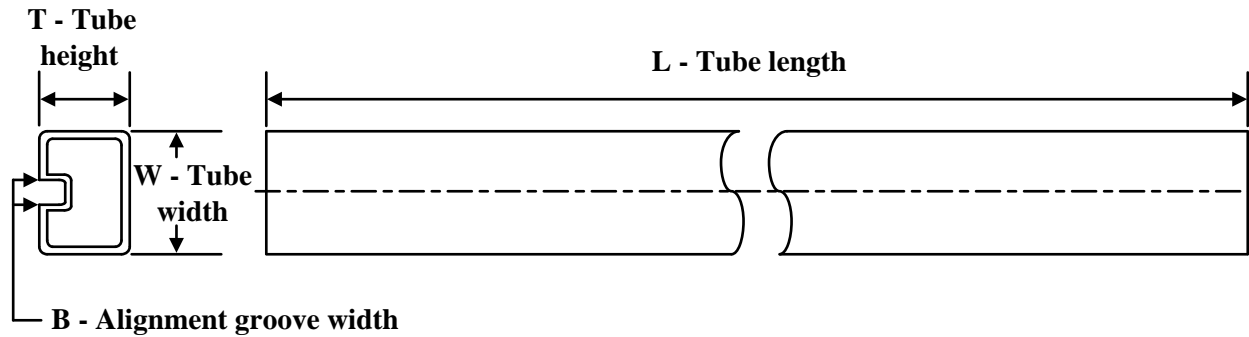

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC138M96	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HC138M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC138M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC238M96	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HC238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC238NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC238PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC238PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC238PWR	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
CD74HC238PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT138M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT238PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC138M96	SOIC	D	16	2500	366.0	364.0	50.0
CD74HC138M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC138M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC238M96	SOIC	D	16	2500	366.0	364.0	50.0
CD74HC238M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC238M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC238NSR	SO	NS	16	2000	356.0	356.0	35.0
CD74HC238PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC238PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC238PWR	TSSOP	PW	16	2000	366.0	364.0	50.0
CD74HC238PWT	TSSOP	PW	16	250	356.0	356.0	35.0
CD74HCT138M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT238M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT238PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC138M	D	SOIC	16	40	507	8	3940	4.32
CD74HC138ME4	D	SOIC	16	40	507	8	3940	4.32
CD74HC238E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238M	D	SOIC	16	40	507	8	3940	4.32
CD74HC238PW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD74HCT138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT138M	D	SOIC	16	40	507	8	3940	4.32
CD74HCT238E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT238E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT238M	D	SOIC	16	40	507	8	3940	4.32
CD74HCT238PW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司