

## High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

### Features

- Overriding Reset Terminates Output Pulse
- Triggering From the Leading or Trailing Edge
- Q and  $\bar{Q}$  Buffered Outputs
- Separate Resets
- Wide Range of Output-Pulse Widths
- Schmitt Trigger on Both  $\bar{A}$  and B Inputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC123, 'HCT123, CD74HC423 and CD74HCT423 are dual monostable multivibrators with resets. They are all retriggerable and differ only in that the 123 types can be triggered by a negative to positive reset pulse; whereas the 423 types do not have this feature. An external resistor ( $R_X$ ) and an external capacitor ( $C_X$ ) control the timing and the accuracy for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. Pulse triggering on the  $\bar{A}$  and B inputs occur at a particular voltage level and is not related to the rise and fall times of the trigger pulses.

Once triggered, the output pulse width may be extended by retriggering inputs  $\bar{A}$  and B. The output pulse can be terminated by a LOW level on the Reset (R) pin. Trailing edge triggering ( $\bar{A}$ ) and leading edge triggering (B) inputs are provided for triggering from either edge of the input pulse. If either Mono is not used each input on the unused device ( $\bar{A}$ , B, and R) must be terminated high or low.

The minimum value of external resistance,  $R_X$  is typically 5k $\Omega$ . The minimum value external capacitance,  $C_X$ , is 0pF. The calculation for the pulse width is  $t_W = 0.45 R_X C_X$  at  $V_{CC} = 5V$ .

### Ordering Information

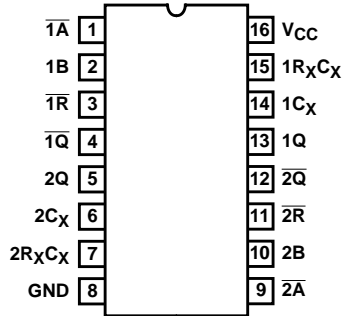
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC123F3A	-55 to 125	16 Ld CERDIP
CD54HCT123F3A	-55 to 125	16 Ld CERDIP
CD74HC123E	-55 to 125	16 Ld PDIP
CD74HC123M	-55 to 125	16 Ld SOIC
CD74HC123MT	-55 to 125	16 Ld SOIC
CD74HC123M96	-55 to 125	16 Ld SOIC
CD74HC123NSR	-55 to 125	16 Ld SOP
CD74HC123PW	-55 to 125	16 Ld TSSOP
CD74HC123PWR	-55 to 125	16 Ld TSSOP
CD74HC123PWT	-55 to 125	16 Ld TSSOP
CD74HC423E	-55 to 125	16 Ld PDIP
CD74HC423M	-55 to 125	16 Ld SOIC
CD74HC423MT	-55 to 125	16 Ld SOIC
CD74HC423M96	-55 to 125	16 Ld SOIC
CD74HC423NSR	-55 to 125	16 Ld SOP
CD74HCT123E	-55 to 125	16 Ld PDIP
CD74HCT123M	-55 to 125	16 Ld SOIC
CD74HCT123MT	-55 to 125	16 Ld SOIC
CD74HCT123M96	-55 to 125	16 Ld SOIC
CD74HCT423E	-55 to 125	16 Ld PDIP
CD74HCT423MT	-55 to 125	16 Ld SOIC
CD74HCT423M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

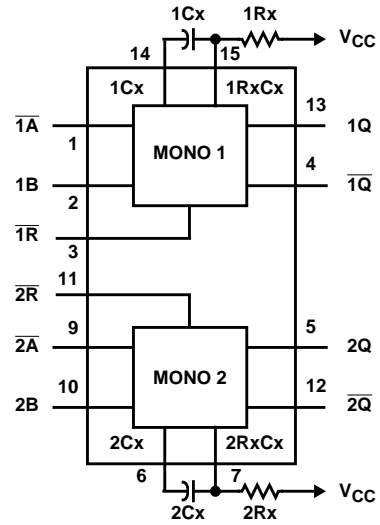
# CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

## Pinout

**CD54HC123, CD54HCT123**  
 (CERDIP)  
**CD74HC123**  
 (PDIP, SOIC, SOP, TSSOP)  
**CD74HC423**  
 (PDIP, SOIC, SOP)  
**CD74HCT123, CD74HCT423**  
 (PDIP, SOIC)  
 TOP VIEW



## Functional Diagram



### TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{A}$	B	$\overline{R}$	Q	$\overline{Q}$
<b>CD74HC/HCT123</b>				
H	X	H	L	H
X	L	H	L	H
L	↑	H		
↓	H	H		
X	X	L	L	H
L	H	↑		
<b>CD74HC/HCT423</b>				
H	X	H	L	H
X	L	H	L	H
L	↑	H		
↓	H	H		
X	X	L	L	H

H = High Voltage Level, L = Low Voltage Level,  
 X = Don't Care.

## CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

### Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 1):	
E (PDIP) Package .....	67°C/W
M (SOIC) Package .....	73°C/W
NS (SOP) Package .....	64°C/W
PW (TSSOP) Package .....	108°C/W
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C
(SOIC - Lead Tips Only)	

### Operating Conditions

Temperature Range ( $T_A$ ) .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

**CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
All	0.35

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g. 360μA max at 25°C.

**Prerequisite for Switching Specifications**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>HC TYPES</b>												
Minimum Input, Pulse Width A	t <sub>WL</sub>	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns
B	t <sub>WH</sub>	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns

**CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423**

**Prerequisite for Switching Specifications (Continued)**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\bar{R}$	t <sub>WL</sub>	2	100	-	-	125	-	-	150	-	150	ns
		4.5	20	-	-	25	-	-	30	-	30	ns
		6	17	-	-	21	-	-	26	-	26	ns
$\bar{A}$ and B Hold Time	t <sub>H</sub>	2	50	-	-	65	-	-	75	-	75	ns
		4.5	10	-	-	13	-	-	15	-	15	ns
		6	9	-	-	11	-	-	13	-	13	ns
Reset Removal Time	t <sub>REM</sub>	2	50	-	-	65	-	-	75	-	75	ns
		4.5	10	-	-	13	-	-	15	-	15	ns
		6	9	-	-	11	-	-	13	-	13	ns
Retrigger Time Number R <sub>X</sub> = 10KΩ, C <sub>X</sub> = 0	t <sub>rT</sub>	5	-	-	-	-	-	-	-	-	-	ns
			-	50	-	-	63	-	-	76	-	ns
Output Pulse Width Q or $\bar{Q}$ R <sub>X</sub> = 10KΩ, C <sub>X</sub> = 10nF	t <sub>W</sub>	5	40	-	50	38.7	-	51.3	38.2	-	51.8	μs
<b>HCT TYPES</b>												
Minimum Input, Pulse Width $\bar{A}$	t <sub>WL</sub>	5	20	-	-	25	-	-	30	-	-	ns
B	t <sub>WH</sub>		20	-	-	25	-	-	30	-	-	ns
$\bar{R}$	t <sub>WL</sub>		20	-	-	25	-	-	30	-	-	ns
$\bar{A}$ and B Hold Time	t <sub>H</sub>	5	10	-	-	13	-	-	15	-	-	ns
Reset Removal Time	t <sub>REM</sub>	5	10	-	-	13	-	-	15	-	-	ns
Retrigger Time Number (Note 3) R <sub>X</sub> = 10KΩ, C <sub>X</sub> = 0	t <sub>rT</sub>	5	-	50	-	-	63	-	-	76	-	ns
Output Pulse Width Q or $\bar{Q}$ R <sub>X</sub> = 10KΩ, C <sub>X</sub> = 10nF	t <sub>W</sub>	5	40	-	50	38.7	-	51.3	38.2	-	51.8	μs

**NOTE:**

- Time to trigger depends on the values of R<sub>X</sub> and C<sub>X</sub>. The output pulse width can only be extended when the time between the active-going edges of the trigger input pulses meet the minimum retrigger time requirement.

**CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423**

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$ ,  $R_X = 10\text{K}\Omega$ ,  $C_X = 0$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNIT S
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Trigger Propagation Delay $\bar{A}, B, \bar{R}$ to $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	51	-	64	-	76	ns
$\bar{A}, B, \bar{R}$ to $\bar{Q}$	$t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	320	-	400	-	480	ns
			4.5	-	-	64	-	80	-	96	ns
		$C_L = 15\text{pF}$	5	-	26	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	54	-	68	-	82	ns
Reset Propagation Delay $\bar{R}$ to $\bar{Q}$ or $\bar{Q}$	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	2	-	-	215	-	270	-	325	ns
			4.5	-	-	43	-	54	-	65	ns
			6	-	-	37	-	46	-	55	ns
Output Transition Time	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Pulse Width $R_X = 10\text{K}\Omega, C_X = 10\text{nF}$	-	-	5	-	45	-	-	-	-	$\mu\text{s}$	
Pulse Width Match Between Circuits In the Same Package $R_X = 10\text{K}\Omega, C_X = 10\text{pF}$	-	-	5	-	$\pm 2$	-	-	-	-	%	
Power Dissipation Capacitance (Note 4)	$C_{PD}$	$C_L = 15\text{pF}$	5	-	-	-	-	-	-	-	pF
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF
<b>HCT TYPES</b>											
Trigger Propagation Delay $\bar{A}, B, \bar{R}$ to $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
$\bar{A}, B, \bar{R}$ to $\bar{Q}$	$t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	68	-	85	-	102	ns
		$C_L = 15\text{pF}$	5	-	27	-	-	-	-	-	ns
Reset Propagation Delay $\bar{R}$ to $\bar{Q}$ or $\bar{Q}$	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	48	-	60	-	72	ns
Output Transition Time	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Output Pulse Width $R_X = 10\text{K}\Omega, C_X = 10\text{nF}$	-	-	5	-	45	-	-	-	-	-	$\mu\text{s}$

**CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423**

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$ ,  $R_X = 10\text{K}\Omega$ ,  $C_X = 0$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNIT S
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Pulse Width Match Between Circuits In the Same Package $R_X = 10\text{K}\Omega$ , $C_X = 10\text{pF}$	-	-	5		$\pm 2$	-	-	-	-	-	%
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF

NOTE:

4.  $C_{PD}$  is used to determine the dynamic power consumption, per multivibrator.

$$P_D = (C_{PD} + C_X) V_{CC}^2 f_i \sum (C_L V_{CC}^2 f_O)$$

Where

$f_i$  = input frequency

$f_O$  = Output Frequency

$C_L$  = Output Load Capacitance

$C_X$  = External Capacitance

$V_{CC}$  = Supply Voltage,

assuming  $f_i \ll \frac{1}{t_W}$

## Test Circuits and Waveforms

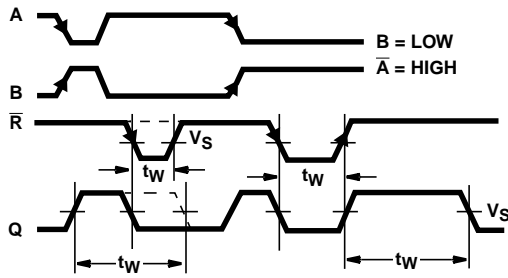


FIGURE 1. OUTPUT PULSE CONTROL USING RESET INPUT ( $\bar{R}$ ) PULSE FOR 123

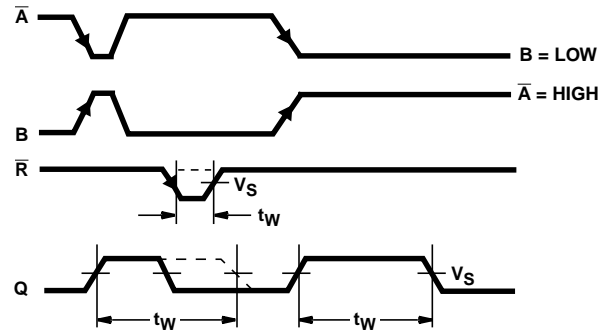
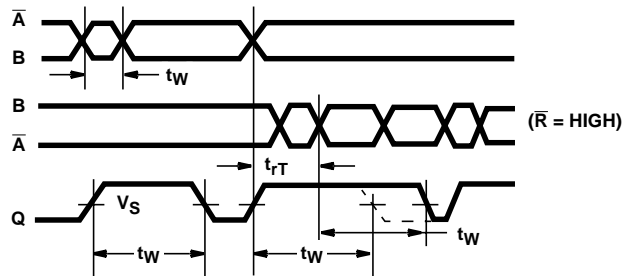


FIGURE 2. OUTPUT PULSE CONTROL USING RESET INPUT ( $\bar{R}$ ) FOR 423



NOTE: Output pulse control using retrigger pulse for 123 and 423.

FIGURE 3. TRIGGERING OF ONE SHOT BY INPUT  $\bar{A}$  OR INPUT B FOR A PERIOD  $t_w$

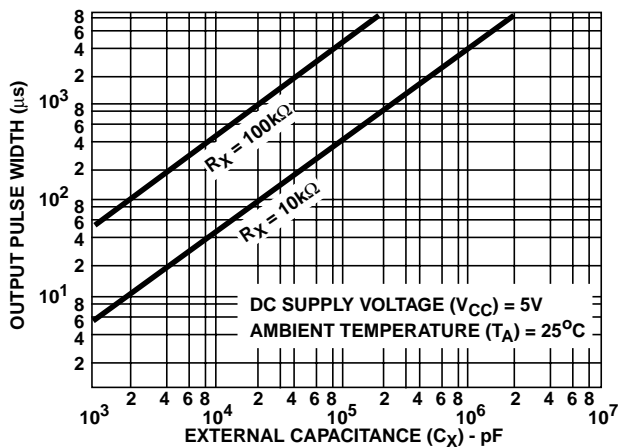


FIGURE 4. TYPICAL OUTPUT PULSE WIDTH AS A FUNCTION OF  $C_x$  FOR  $R_x = 10k\Omega$  AND  $100k\Omega$

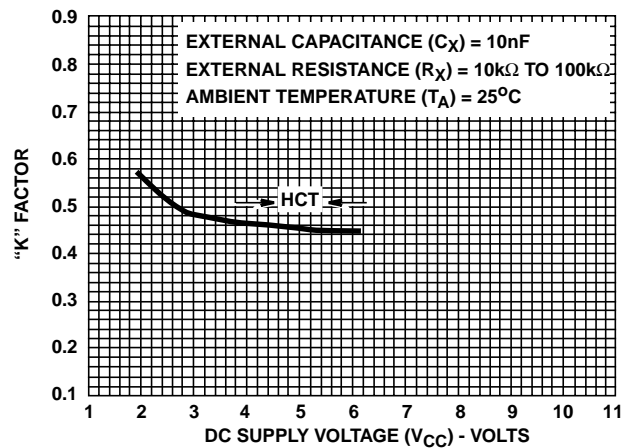


FIGURE 5. TYPICAL "K" FACTOR AS A FUNCTION OF  $V_{CC}$

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8684701EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8684701EA CD54HC123F3A	<a href="#">Samples</a>
5962-8970001EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8970001EA CD54HCT123F3A	<a href="#">Samples</a>
CD54HC123F	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC123F	<a href="#">Samples</a>
CD54HC123F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8684701EA CD54HC123F3A	<a href="#">Samples</a>
CD54HCT123F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8970001EA CD54HCT123F3A	<a href="#">Samples</a>
CD74HC123E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC123E	<a href="#">Samples</a>
CD74HC123EE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC123E	<a href="#">Samples</a>
CD74HC123M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123M96E4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123ME4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123MG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123MTG4	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC123M	<a href="#">Samples</a>
CD74HC123PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ123	<a href="#">Samples</a>
CD74HC123PWE4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ123	<a href="#">Samples</a>
CD74HC123PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HJ123	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC123PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ123	<a href="#">Samples</a>
CD74HC123PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ123	<a href="#">Samples</a>
CD74HC123PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ123	<a href="#">Samples</a>
CD74HC423E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC423E	<a href="#">Samples</a>
CD74HC423M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC423M	<a href="#">Samples</a>
CD74HC423M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC423M	<a href="#">Samples</a>
CD74HC423M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC423M	<a href="#">Samples</a>
CD74HC423MG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC423M	<a href="#">Samples</a>
CD74HC423MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC423M	<a href="#">Samples</a>
CD74HC423NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC423M	<a href="#">Samples</a>
CD74HCT123E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT123E	<a href="#">Samples</a>
CD74HCT123M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT123M	<a href="#">Samples</a>
CD74HCT123M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT123M	<a href="#">Samples</a>
CD74HCT123M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT123M	<a href="#">Samples</a>
CD74HCT123MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT123M	<a href="#">Samples</a>
CD74HCT423E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT423E	<a href="#">Samples</a>
CD74HCT423M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT423M	<a href="#">Samples</a>
CD74HCT423M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT423M	<a href="#">Samples</a>
CD74HCT423MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT423M	<a href="#">Samples</a>
CD74HCT423MTE4	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT423M	<a href="#">Samples</a>
CD74HCT423MTG4	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT423M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC123, CD54HCT123, CD74HC123, CD74HCT123 :**

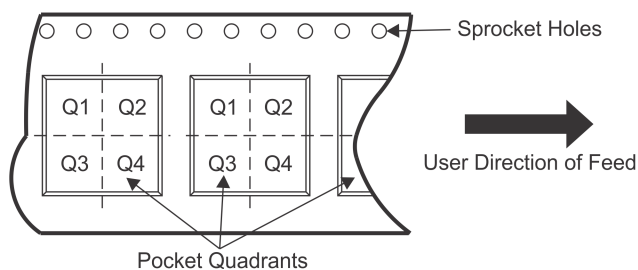
● Catalog : [CD74HC123](#), [CD74HCT123](#)

● Military : [CD54HC123](#), [CD54HCT123](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


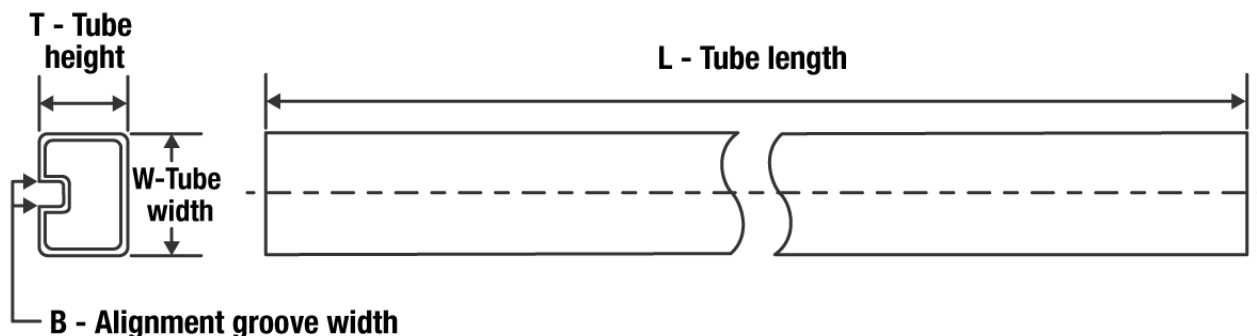
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC123M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC123M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC123M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC123NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC123PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC123PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC123PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC123PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC423M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC423NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HCT123M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT423M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC123M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC123M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC123M96G4	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC123NSR	SO	NS	16	2000	853.0	449.0	35.0
CD74HC123PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC123PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
CD74HC123PWRG4	TSSOP	PW	16	2000	853.0	449.0	35.0
CD74HC123PWT	TSSOP	PW	16	250	853.0	449.0	35.0
CD74HC423M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC423NSR	SO	NS	16	2000	853.0	449.0	35.0
CD74HCT123M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT423M96	SOIC	D	16	2500	340.5	336.1	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC123E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC123E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC123EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC123EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC123M	D	SOIC	16	40	507	8	3940	4.32
CD74HC123ME4	D	SOIC	16	40	507	8	3940	4.32
CD74HC123MG4	D	SOIC	16	40	507	8	3940	4.32
CD74HC123PW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD74HC123PWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
CD74HC423E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC423E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC423M	D	SOIC	16	40	507	8	3940	4.32
CD74HC423MG4	D	SOIC	16	40	507	8	3940	4.32
CD74HCT123E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT123E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT123M	D	SOIC	16	40	507	8	3940	4.32
CD74HCT423E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT423E	N	PDIP	16	25	506	13.97	11230	4.32



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated