

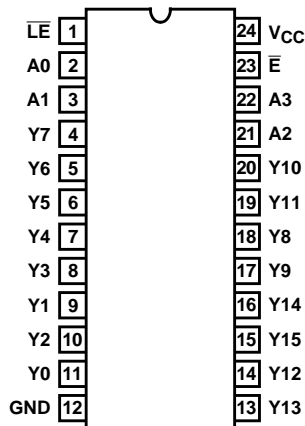
## High-Speed CMOS Logic 4- to 16-Line Decoder/Demultiplexer with Input Latches

### Features

- Multifunction Capability
  - Binary to 1-of-16 Decoder
  - 1-to-16 Line Demultiplexer
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$

### Pinout

CD54HC4514  
(CERDIP)  
CD74HC4514, CD74HC4515  
(PDIP, SOIC)  
TOP VIEW



### Description

The CD54HC4514, CD74HC4514, and CD74HC4515 are high-speed silicon gate devices consisting of a 4-bit strobed latch and a 4- to 16-line decoder. The selected output is enabled by a low on the enable input (E). A high on  $\bar{E}$  inhibits selection of any output. Demultiplexing is accomplished by using the  $\bar{E}$  input as the data input and the select inputs (A0-A3) as addresses. This  $\bar{E}$  input also serves as a chip select when these devices are cascaded.

When Latch Enable ( $\bar{LE}$ ) is high the output follows changes in the inputs (see truth table). When  $\bar{LE}$  is low the output is isolated from changes in the input and remains at the level (high for the 4514, low for the 4515) it had before the latches were enabled. These devices, enhanced versions of the equivalent CMOS types, can drive 10 LSTTL loads.

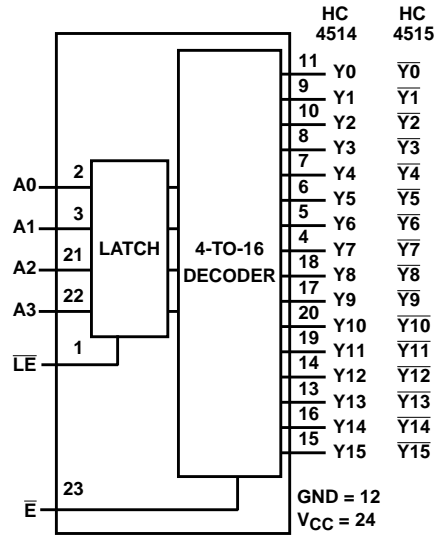
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4514F3A	-55 to 125	24 Ld CERDIP
CD74HC4514E	-55 to 125	24 Ld PDIP
CD74HC4514EN	-55 to 125	24 Ld PDIP
CD74HC4514M	-55 to 125	24 Ld SOIC
CD74HC4514M96	-55 to 125	24 Ld SOIC
CD74HC4515E	-55 to 125	24 Ld PDIP
CD74HC4515EN	-55 to 125	24 Ld PDIP
CD74HC4515M	-55 to 125	24 Ld SOIC
CD74HC4515M96	-55 to 125	24 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

**CD54HC4514, CD74HC4514, CD74HC4515**

**Functional Diagram**



**DECODE TRUTH TABLE ( $\overline{LE} = 1$ )**

ENABLE	DECODER INPUTS				ADDRESSED OUTPUT 4514 = LOGIC 1 (HIGH) 4515 = LOGIC 0 (HIGH)
	A3	A2	A1	A0	
0	0	0	0	0	Y0
0	0	0	0	1	Y1
0	0	0	1	0	Y2
0	0	0	1	1	Y3
0	0	1	0	0	Y4
0	0	1	0	1	Y5
0	0	1	1	0	Y6
0	0	1	1	1	Y7
0	1	0	0	0	Y8
0	1	0	0	1	Y9
0	1	0	1	0	Y10
0	1	0	1	1	Y11
0	1	1	0	0	Y12
0	1	1	0	1	Y13
0	1	1	1	0	Y14
0	1	1	1	1	Y15
1	X	X	X	X	All Outputs = 0, 4514 All Outputs = 1, 4515

X = Don't Care; Logic 1 = High; Logic 0 = Low

# CD54HC4514, CD74HC4514, CD74HC4515

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package (Note 1) .....	67
EN (PDIP) Package (Note 1) .....	67
M (SOIC) Package (Note 2) .....	46
Maximum Junction Temperature .....	150 $^{\circ}C$
Maximum Storage Temperature Range .....	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	300 $^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	2V to 6V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTES:

1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>													
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
			-4	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	-5.2	6	5.48	-	-	5.34	-	5.2	-	V

**CD54HC4514, CD74HC4514, CD74HC4515**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
			0.02	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V	
			0.02	0.02	6	-	-	0.1	-	0.1	-	0.1	V	
-			-	-	-	-	-	-	-	-	-	-	V	
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA		
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA		

**Prerequisite For Switching Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
LE Pulse Width	t <sub>w</sub>	-	2	75	-	-	95	-	110	-	ns
			4.5	30	-	-	19	-	22	-	ns
			6	35	-	-	16	-	19	-	ns
Select to LE Set-Up Time	t <sub>SU</sub>	-	2	100	-	-	125	-	150	-	ns
			4.5	20	-	-	25	-	30	-	ns
			6	17	-	-	21	-	26	-	ns
Select to LE Hold Time	t <sub>H</sub>	-	2	0	-	-	0	-	0	-	ns
			4.5	0	-	-	0	-	0	-	ns
			6	0	-	-	0	-	0	-	ns

**Switching Specifications** C<sub>L</sub> = 50pF, Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay Select to Outputs	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
		C <sub>L</sub> = 15pF	5	-	23	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	47	-	59	-	71	ns
LE to Outputs	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	225	-	280	-	340	ns
			4.5	-	-	45	-	56	-	68	ns
		C <sub>L</sub> = 15pF	5	-	19	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	38	-	48	-	58	ns

# CD54HC4514, CD74HC4514, CD74HC4515

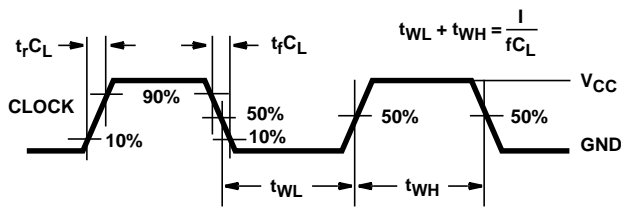
## Switching Specifications $C_L = 50\text{pF}$ , Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\bar{E}$ to Outputs	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	30	-	37	-	45	ns
Output Transition Time	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	-	70	-	-	-	-	-	pF

**NOTES:**

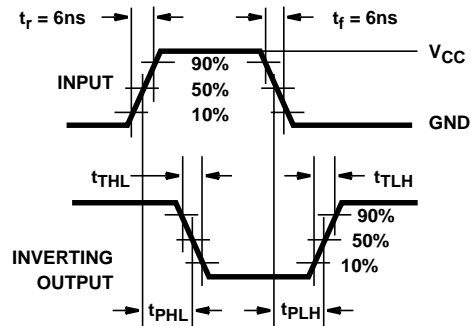
3.  $C_{PD}$  is used to determine the dynamic power consumption, per package.
4.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms

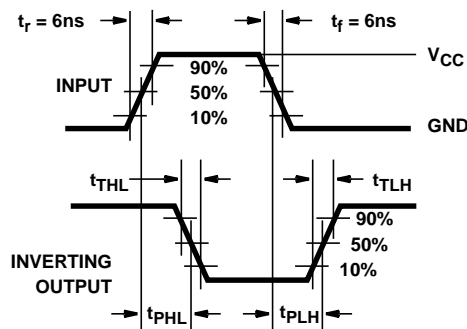


NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



**FIGURE 2. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

Test Circuits and Waveforms (Continued)

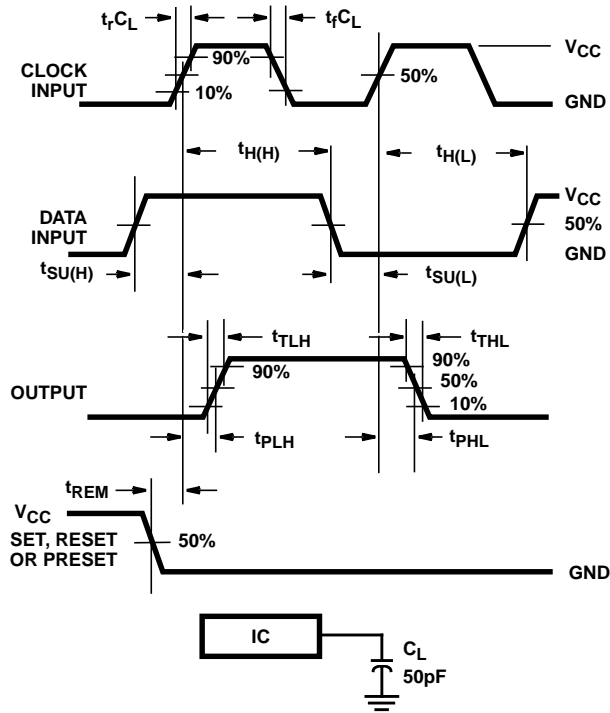


FIGURE 4. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

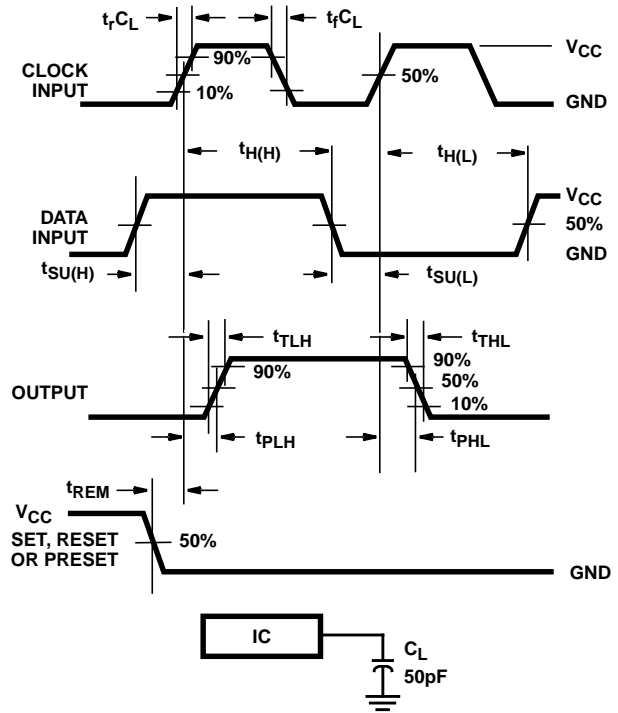
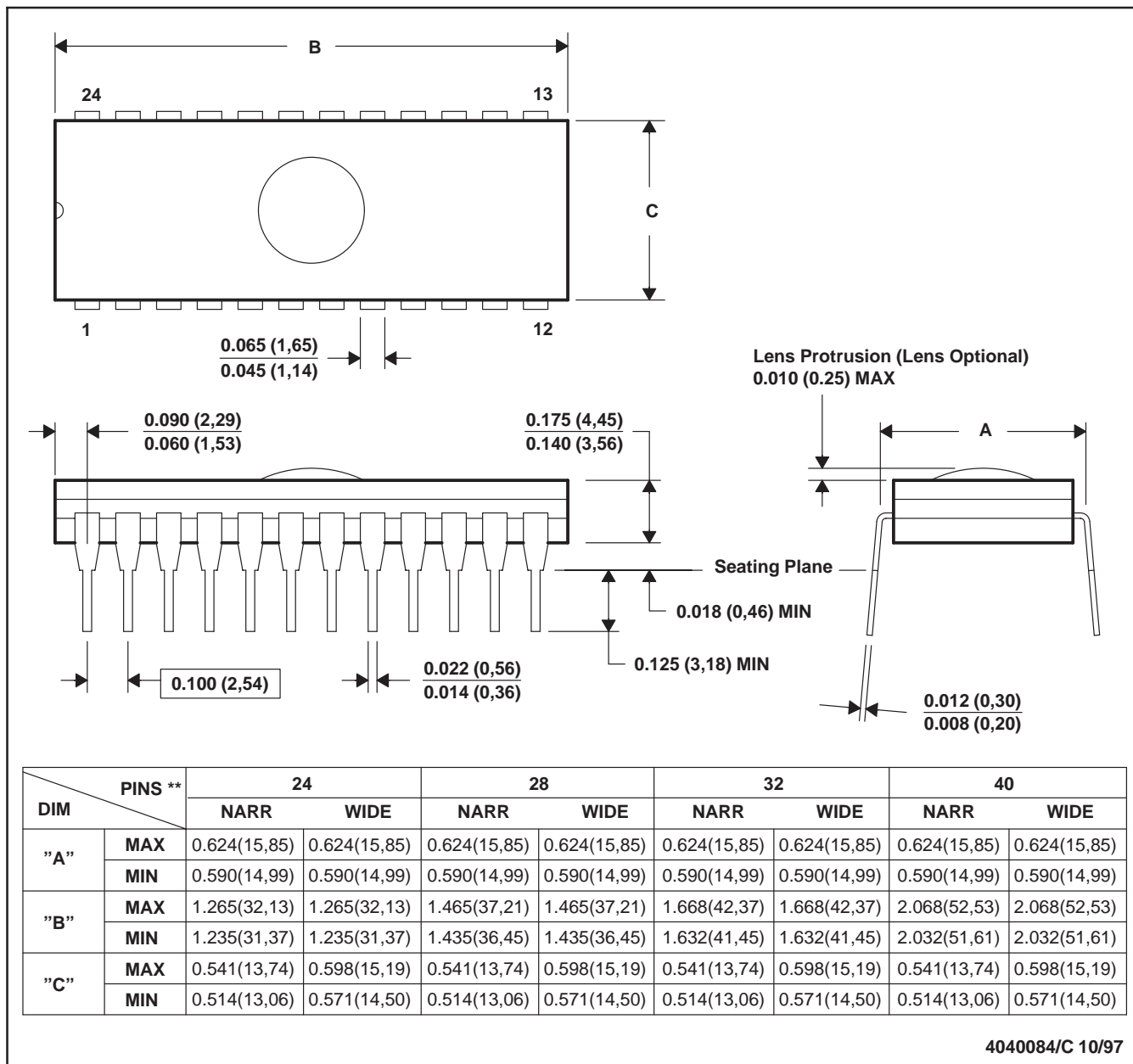


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

J (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN

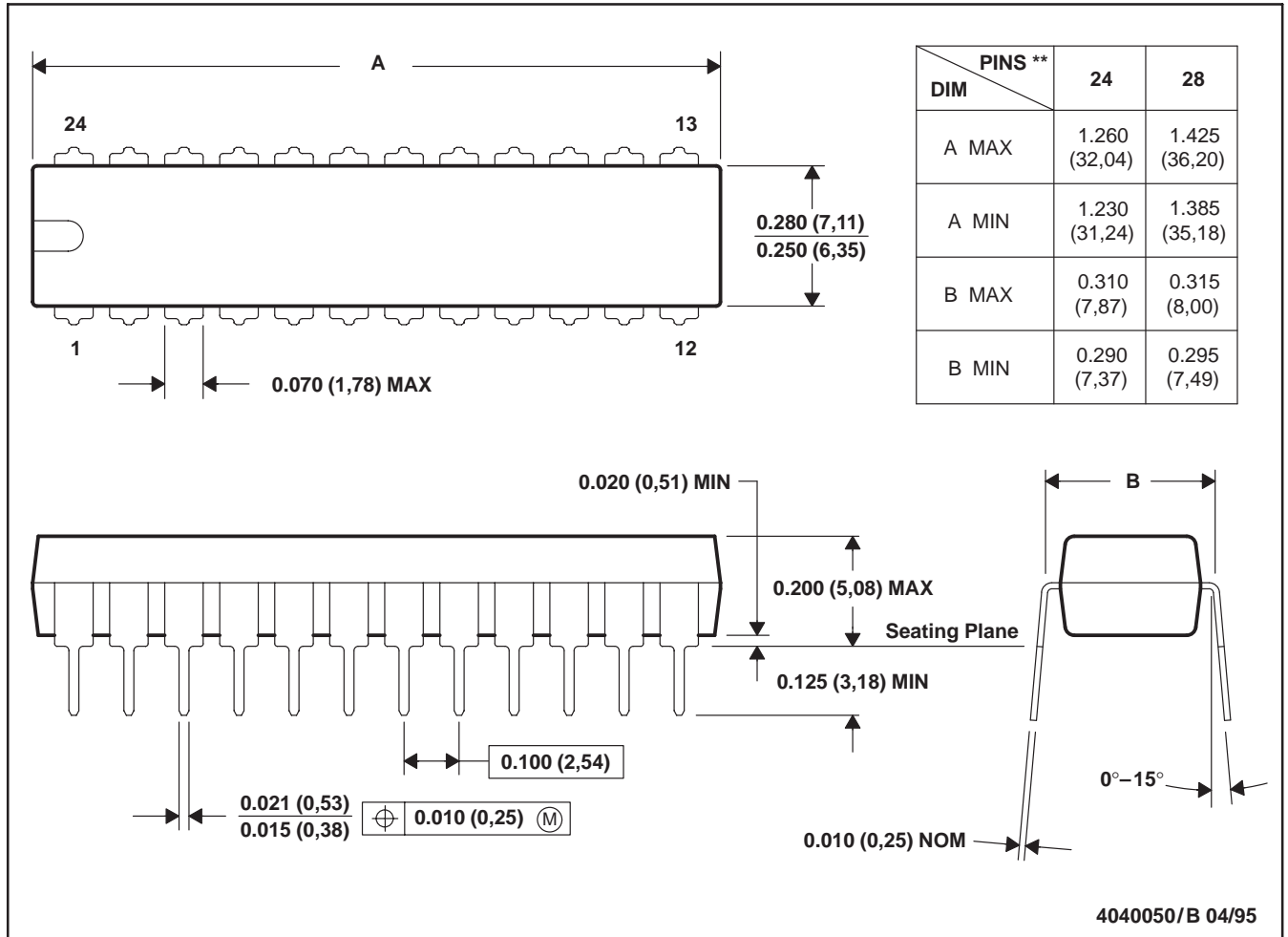


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).  
 D. This package can be hermetically sealed with a ceramic lid using glass frit.  
 E. Index point is provided on cap for terminal identification.

NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

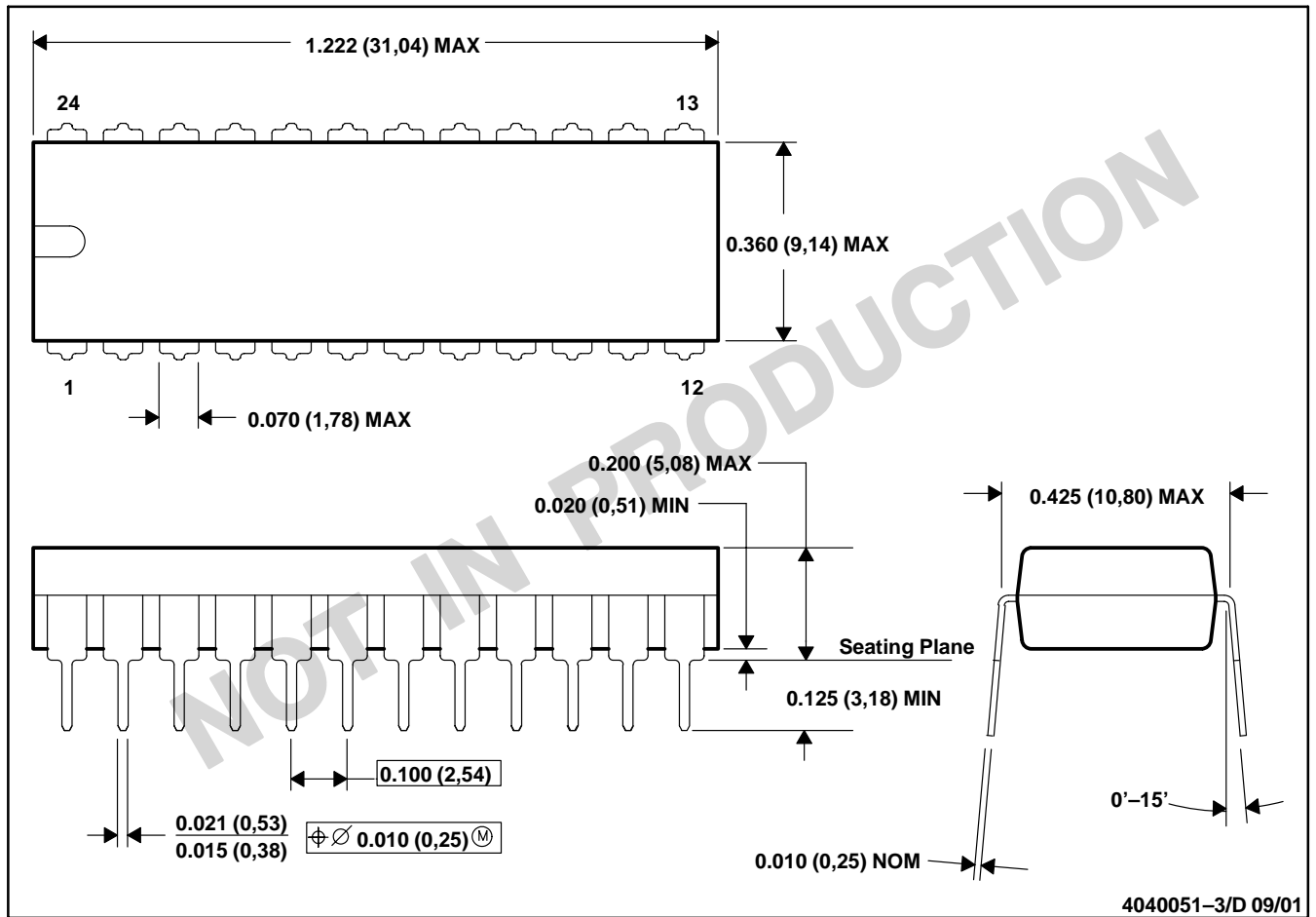
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

N (R-PDIP-T24)

PLASTIC DUAL-IN-LINE

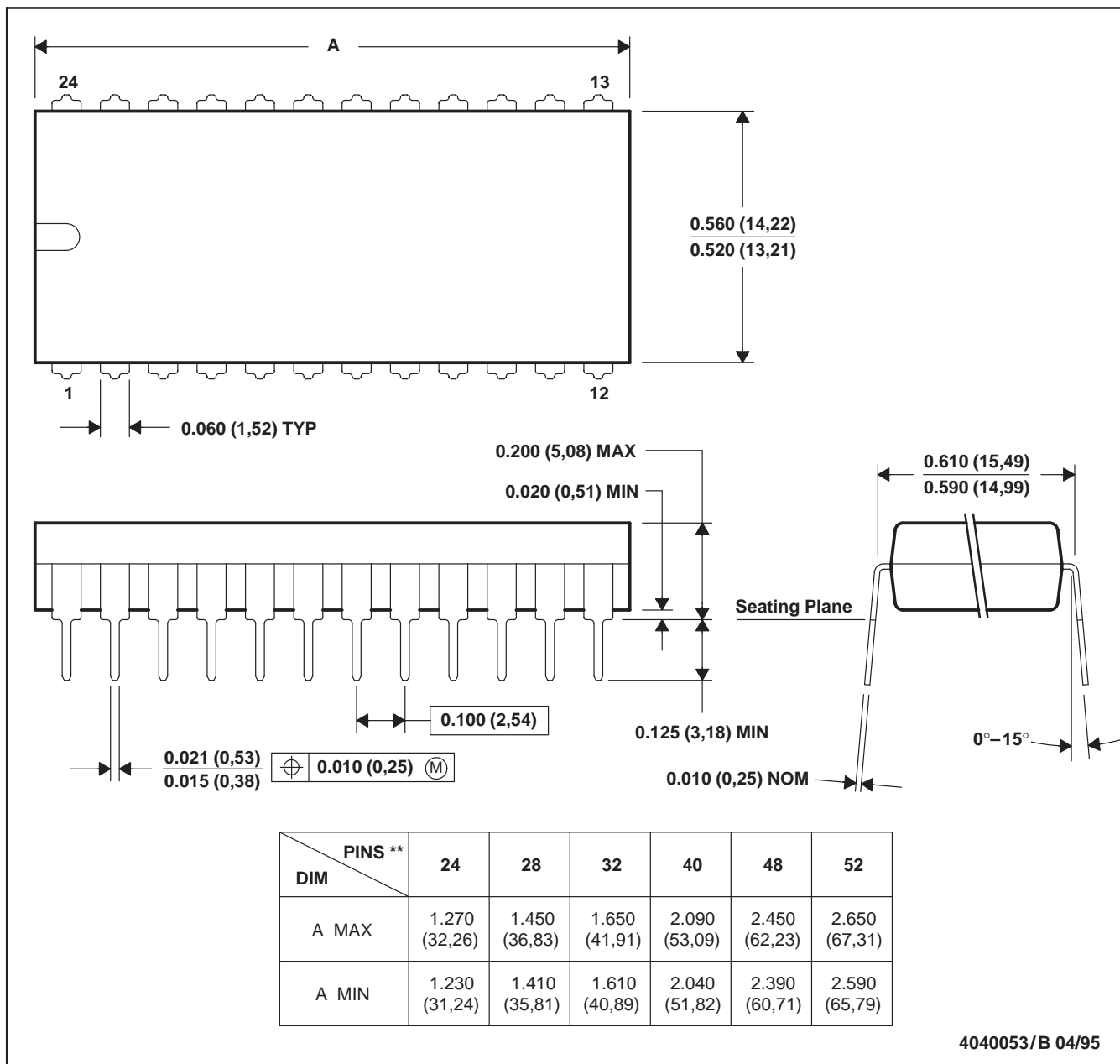


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-010

**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

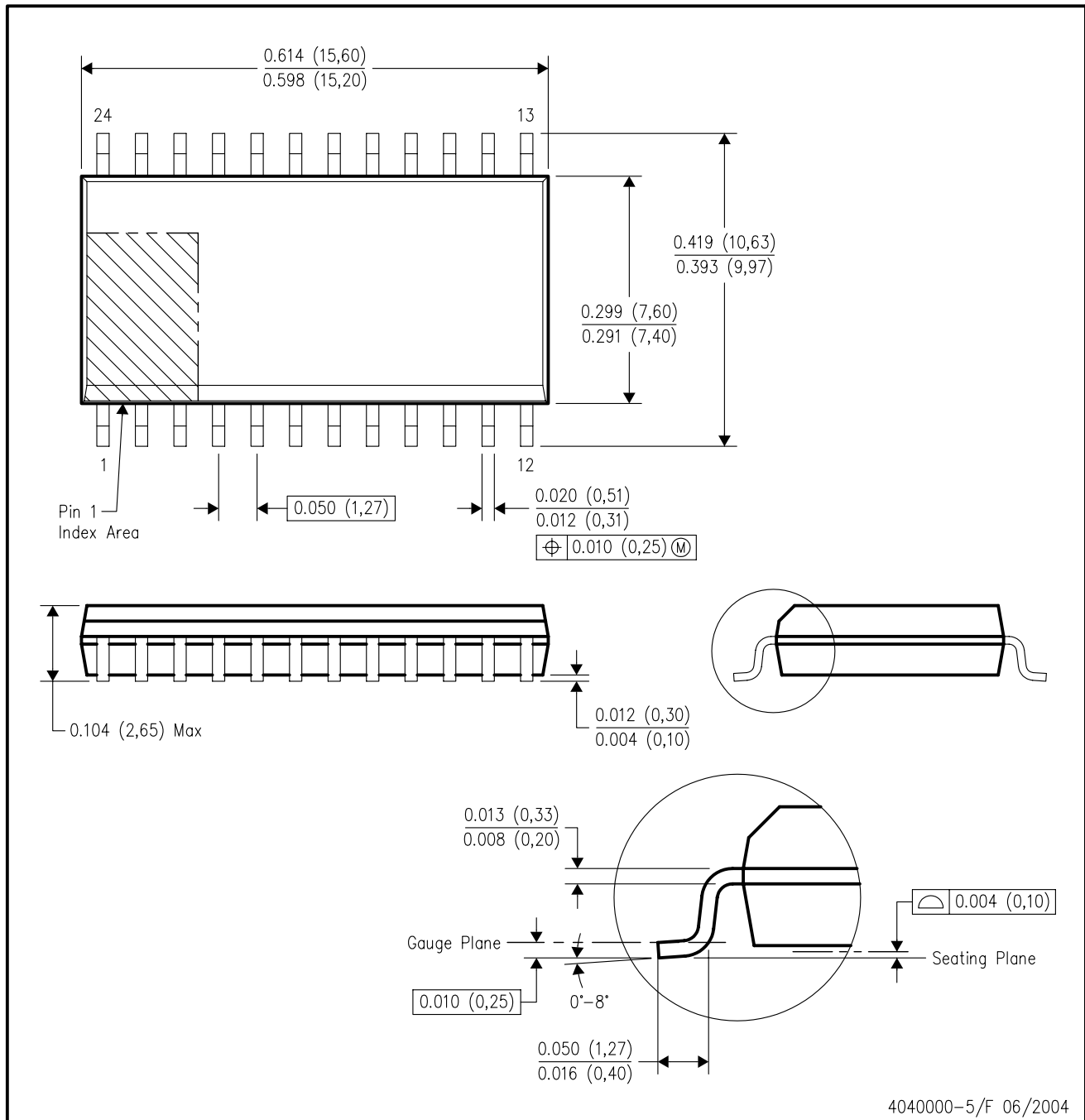
24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-011  
 D. Falls within JEDEC MS-015 (32 pin only)

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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