

# CD54HC251, CD74HC251, CD54HCT251, CD74HCT251

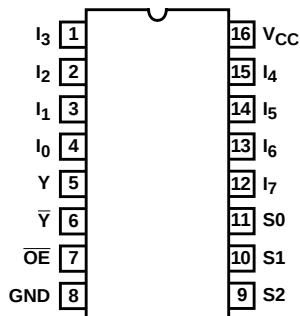
## High-Speed CMOS Logic 8-Input Multiplexer, Three-State

### Features

- Selects One of Eight Binary Data Inputs
- Three-State Output Capability
- True and Complement Outputs
- Typical (Data to Output) Propagation Delay of 14ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Pinout

CD54HC251, CD54HCT251  
(CERDIP)  
CD74HC251, CD74HCT251  
(PDIP, SOIC)  
TOP VIEW



### Description

The 'HC251 and 'HCT251 are 8-channel digital multiplexers with three-state outputs, fabricated with high-speed silicon-gate CMOS technology. Together with the low power consumption of standard CMOS integrated circuits, they possess the ability to drive 10 LSTTL loads. The three-state feature makes them ideally suited for interfacing with bus lines in a bus-oriented system.

This multiplexer features both true (Y) and complement ( $\bar{Y}$ ) outputs as well as an output enable ( $\bar{OE}$ ) input. The  $\bar{OE}$  must be at a low logic level to enable this device. When the  $\bar{OE}$  input is high, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and  $\bar{Y}$  outputs. The 'HCT251 logic family is speed, function, and pin-compatible with the standard 'LS251.

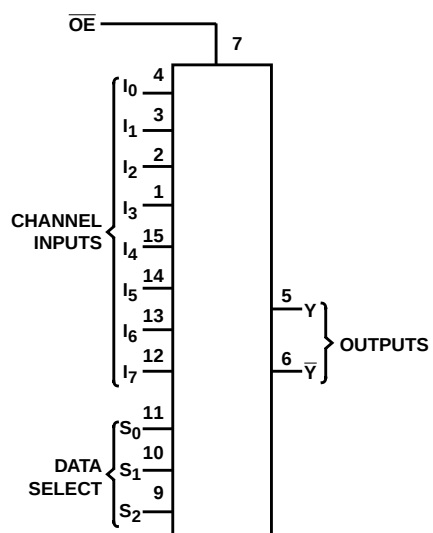
### Ordering Information

| PART NUMBER   | TEMP. RANGE<br>( $^\circ C$ ) | PACKAGE      |
|---------------|-------------------------------|--------------|
| CD54HC251F3A  | -55 to 125                    | 16 Ld CERDIP |
| CD54HCT251F3A | -55 to 125                    | 16 Ld CERDIP |
| CD74HC251E    | -55 to 125                    | 16 Ld PDIP   |
| CD74HC251M    | -55 to 125                    | 16 Ld SOIC   |
| CD74HC251MT   | -55 to 125                    | 16 Ld SOIC   |
| CD74HC251M96  | -55 to 125                    | 16 Ld SOIC   |
| CD74HCT251E   | -55 to 125                    | 16 Ld PDIP   |
| CD74HCT251M   | -55 to 125                    | 16 Ld SOIC   |
| CD74HCT251MT  | -55 to 125                    | 16 Ld SOIC   |
| CD74HCT251M96 | -55 to 125                    | 16 Ld SOIC   |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

# CD54HC251, CD74HC251, CD54HCT251, CD74HCT251

## Functional Diagram



TRUTH TABLE

| INPUTS |    |    |                                   | OUTPUT |             |
|--------|----|----|-----------------------------------|--------|-------------|
| SELECT |    |    | OUTPUT<br>CONTROL $\overline{OE}$ | Y      | $\bar{Y}$   |
| S2     | S1 | S0 |                                   |        |             |
| X      | X  | X  | H                                 | Z      | Z           |
| L      | L  | L  | L                                 | $l_0$  | $\bar{l}_0$ |
| L      | L  | H  | L                                 | $l_1$  | $\bar{l}_1$ |
| L      | H  | L  | L                                 | $l_2$  | $\bar{l}_2$ |
| L      | H  | H  | L                                 | $l_3$  | $\bar{l}_3$ |
| H      | L  | L  | L                                 | $l_4$  | $\bar{l}_4$ |
| H      | L  | H  | L                                 | $l_5$  | $\bar{l}_5$ |
| H      | H  | L  | L                                 | $l_6$  | $\bar{l}_6$ |
| H      | H  | H  | L                                 | $l_7$  | $\bar{l}_7$ |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, Z = High Impedance (Off),  $l_0, l_1 \dots l_7$  = the level of the respective input.

# CD54HC251, CD74HC251, CD54HCT251, CD74HCT251

## Absolute Maximum Ratings

|                                                        |             |
|--------------------------------------------------------|-------------|
| DC Supply Voltage, $V_{CC}$                            | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Drain Current, per Output, $I_O$                    |             |
| For $-0.5V < V_O < V_{CC} + 0.5V$                      | $\pm 25mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$             | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$                | $\pm 50mA$  |

## Thermal Information

|                                          |                                    |
|------------------------------------------|------------------------------------|
| Thermal Resistance (Typical, Note 1)     | $\theta_{JA}$ ( $^{\circ}C/W$ )    |
| E (PDIP) Package                         | 67                                 |
| M (SOIC) Package                         | 73                                 |
| Maximum Junction Temperature             | 150 $^{\circ}C$                    |
| Maximum Storage Temperature Range        | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$                    |
| (SOIC - Lead Tips Only)                  |                                    |

## Operating Conditions

|                                           |                                    |
|-------------------------------------------|------------------------------------|
| Temperature Range ( $T_A$ )               | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, $V_{CC}$            |                                    |
| HC Types                                  | .2V to 6V                          |
| HCT Types                                 | .4.5V to 5.5V                      |
| DC Input or Output Voltage, $V_I$ , $V_O$ | 0V to $V_{CC}$                     |
| Input Rise and Fall Time                  |                                    |
| 2V                                        | 1000ns (Max)                       |
| 4.5V                                      | 500ns (Max)                        |
| 6V                                        | 400ns (Max)                        |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |      |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|------------------------------------|---------------------|---------------------|------|------|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP  | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                    |                     |                     |      |      |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                   | 1.5  | -    | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                    |                     | 4.5                 | 3.15 | -    | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                    |                     | 6                   | 4.2  | -    | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                   | -    | -    | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                    |                     | 4.5                 | -    | -    | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                    |                     | 6                   | -    | -    | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -    | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                    | -0.02               | 4.5                 | 4.4  | -    | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                    | -0.02               | 6                   | 5.9  | -    | -    | 5.9           | -    | 5.9            | -    | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| -4                                      |                 |                                    | 4.5                 | 3.98                | -    | -    | 3.84 | -             | 3.7  | -              | V    |       |
| -5.2                                    |                 |                                    | 6                   | 5.48                | -    | -    | 5.34 | -             | 5.2  | -              | V    |       |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| 4                                       |                 |                                    | 4.5                 | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| 5.2                                     |                 |                                    | 6                   | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| Low Level Output Voltage<br>TTL Loads   |                 |                                    |                     |                     |      |      |      |               |      |                |      |       |

# **CD54HC251, CD74HC251, CD54HCT251, CD74HCT251**

## **DC Electrical Specifications (Continued)**

| PARAMETER                                                      | SYMBOL                    | TEST CONDITIONS                    |                                         | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------------|---------------------------|------------------------------------|-----------------------------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|                                                                |                           | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA)                     |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| Input Leakage Current                                          | I <sub>I</sub>            | V <sub>CC</sub> or GND             | -                                       | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | 0                                       | 6                   | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Three-State Leakage Current                                    | -                         | V <sub>IL</sub> or V <sub>IH</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND | 6                   | -    | -   | ±0.5 | -             | ±5.0 | -              | ±10 | μA    |
| <b>HCT TYPES</b>                                               |                           |                                    |                                         |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>           | -                                  | -                                       | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage                                        | V <sub>IL</sub>           | -                                  | -                                       | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | -0.02                                   | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                           |                                    | -4                                      | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                                    | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                           |                                    | 4                                       | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current                                          | I <sub>I</sub>            | V <sub>CC</sub> and GND            | 0                                       | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | 0                                       | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Three-State Leakage Current                                    | -                         | V <sub>IL</sub> or V <sub>IH</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND | 6                   | -    | -   | ±0.5 | -             | ±5.0 | -              | ±10 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2) | V <sub>CC</sub> -2.1               | -                                       | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

## **HCT Input Loading Table**

| INPUT      | UNIT LOADS |
|------------|------------|
| S0, S1, S2 | 0.55       |
| I0 - I7    | 0.5        |
| OE         | 2.65       |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

# CD54HC251, CD74HC251, CD54HCT251, CD74HCT251

## Switching Specifications Input $t_r$ , $t_f$ = 6ns

| PARAMETER                                  | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                            |                                     |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                                   |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay<br>Select to Outputs     | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 245 | -             | 305 | -              | 370 | ns    |
|                                            |                                     |                       | 4.5                 | -    | -   | 49  | -             | 61  | -              | 74  | ns    |
|                                            |                                     | C <sub>L</sub> =15pF  | 5                   | -    | 21  | -   | -             | -   | -              | -   | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 42  | -             | 52  | -              | 63  | ns    |
| Data to Outputs                            | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 175 | -             | 220 | -              | 265 | ns    |
|                                            |                                     |                       | 4.5                 | -    | -   | 35  | -             | 44  | -              | 53  | ns    |
|                                            |                                     | C <sub>L</sub> =15pF  | 5                   | -    | 12  | -   | -             | -   | -              | -   | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 30  | -             | 37  | -              | 45  | ns    |
| Enable to High Z and Enable from High Z    | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 140 | -             | 175 | -              | 210 | ns    |
|                                            |                                     |                       | 4.5                 | -    | -   | 28  | -             | 35  | -              | 42  | ns    |
|                                            |                                     | C <sub>L</sub> =15pF  | 5                   | -    | 11  | -   | -             | -   | -              | -   | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 24  | -             | 30  | -              | 36  | ns    |
| Output Transition Time                     | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|                                            |                                     |                       | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                            |                                     |                       | 6                   | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Input Capacitance                          | C <sub>IN</sub>                     | -                     | -                   | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Three-State Output Capacitance             | CO                                  | -                     | -                   | -    | -   | 15  | -             | 15  | -              | 15  | pF    |
| Power Dissipation Capacitance (Notes 3, 4) | C <sub>PD</sub>                     | -                     | 5                   | -    | 60  | -   | -             | -   | -              | -   | pF    |
| HCT TYPES                                  |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay<br>Select to Outputs     | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 42  | -             | 53  | -              | 63  | ns    |
|                                            |                                     | C <sub>L</sub> =15pF  | 5                   | -    | 18  | -   | -             | -   | -              | -   | ns    |
|                                            |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Data to Outputs                            | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 35  | -             | 44  | -              | 53  | ns    |
|                                            |                                     | C <sub>L</sub> =15pF  | 5                   | -    | 12  | -   | -             | -   | -              | -   | ns    |
| Enable to High Z and Enable from High Z    | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    |     | 30  | -             | 38  | -              | 45  | ns    |
|                                            |                                     | C <sub>L</sub> =15pF  | 5                   | -    | 12  | -   | -             | -   | -              | -   | ns    |
| Output Transition Time                     | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
| Input Capacitance                          | C <sub>IN</sub>                     | -                     | -                   | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance (Notes 3, 4) | C <sub>PD</sub>                     | -                     | 5                   |      | 60  | -   | -             | -   | -              | -   | pF    |

### NOTES:

- $C_{PD}$  is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## Test Circuits and Waveforms

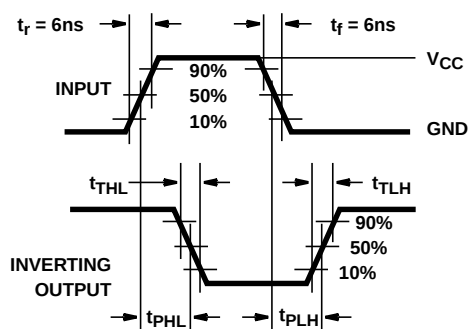


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

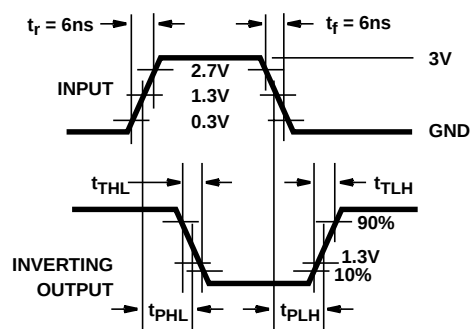


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

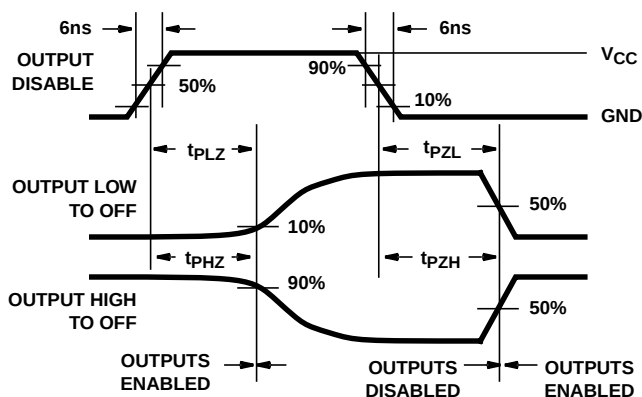


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

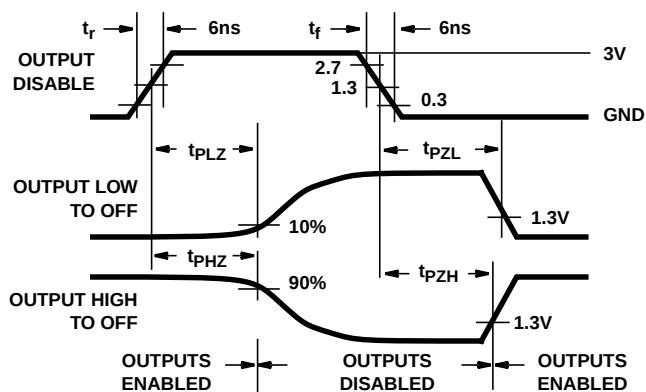
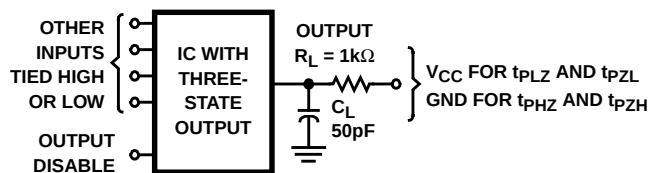


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



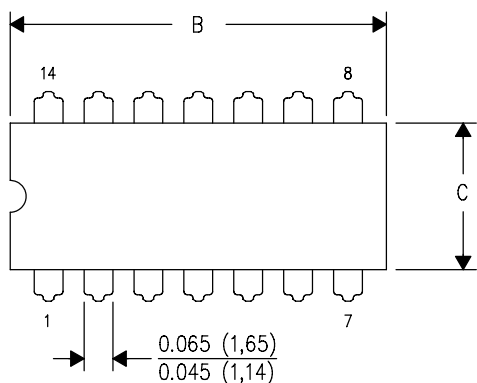
NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZH}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

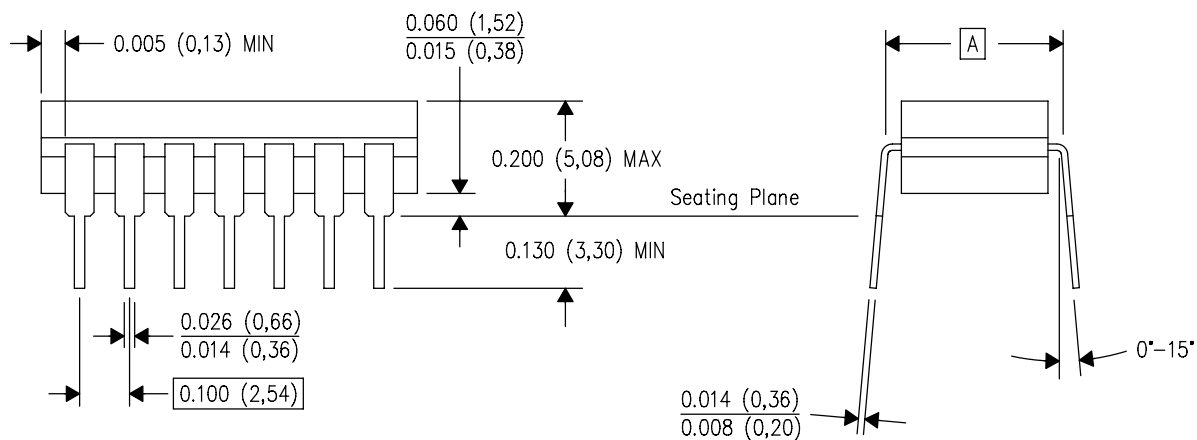
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14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



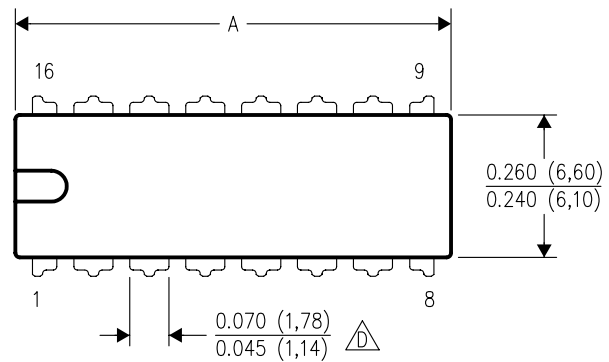
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

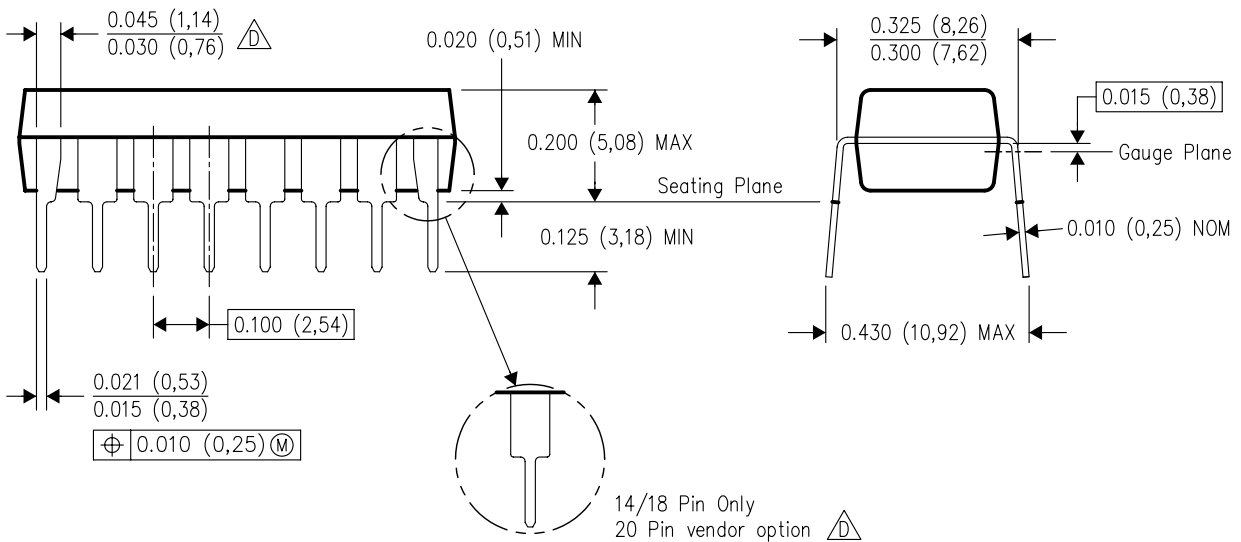
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |

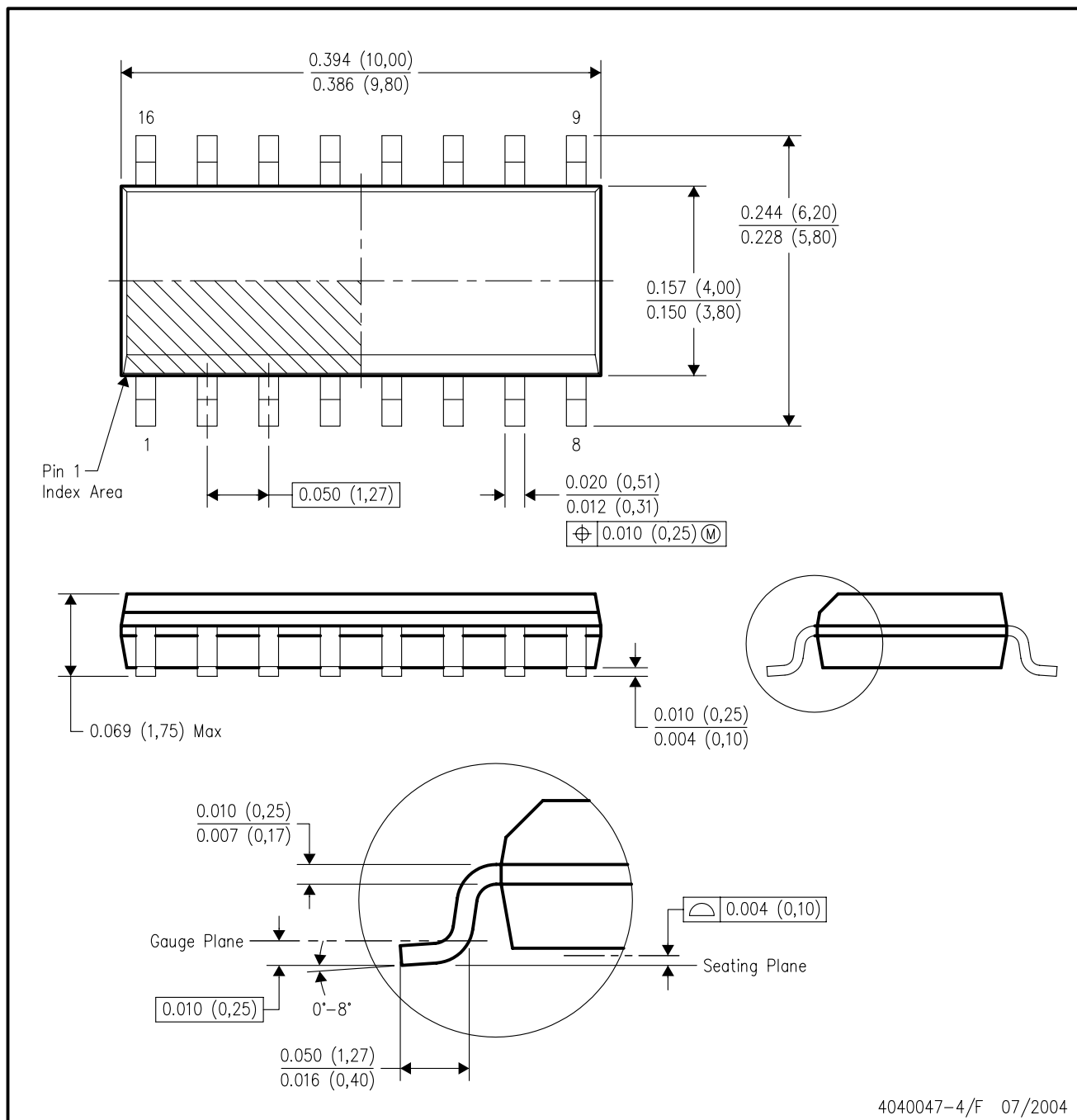


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AC.

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