TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS155C

October 1997 - Revised August 2003

CD54HC164, CD74HC164, CD54HCT164, CD74HCT164

High-Speed CMOS Logic 8-Bit Serial-In/Parallel-Out Shift Register

Features

- **Buffered Inputs**
- **Asynchronous Master Reset**
- **Typical f_{MAX} = 60MHz at V_{CC} = 5V, C_L = 15pF, $T_A = 25^oC$**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The ’HC164 and ’HCT164 are 8-bit serial-in parallel-out shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CP). A LOW on the Master Reset ($\overline{MR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided, either one can be used as a Data Enable control.

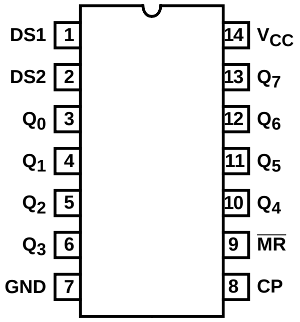
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC164F3A	-55 to 125	14 Ld CERDIP
CD54HCT164F3A	-55 to 125	14 Ld CERDIP
CD74HC164E	-55 to 125	14 Ld PDIP
CD74HC164M	-55 to 125	14 Ld SOIC
CD74HC164MT	-55 to 125	14 Ld SOIC
CD74HC164M96	-55 to 125	14 Ld SOIC
CD74HCT164E	-55 to 125	14 Ld PDIP
CD74HCT164M	-55 to 125	14 Ld SOIC
CD74HCT164MT	-55 to 125	14 Ld SOIC
CD74HCT164M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

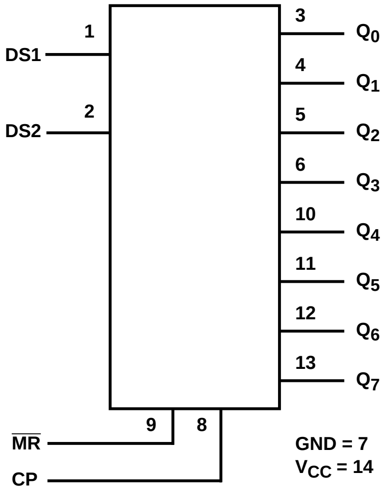
Pinout

CD54HC164, CD54HCT164
(CERDIP)
CD74HC164, CD74HCT164
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1	DS2	Q_0	Q_1 - Q_7
RESET (CLEAR)	**L**	**X**	**X**	**X**	**L**	**L - L**
Shift	H	↑	l	l	L	q_0 - q_6
	H	↑	l	h	L	q_0 - q_6
	H	↑	h	l	L	q_0 - q_6
	H	↑	h	h	H	q_0 - q_6

H= High Voltage Level.
h= High Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition.
l= Low Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition.
L= Low Voltage Level.
X= Don’t Care.
↑= Transition from Low to High Level.
q_n= Lower Case Letters Indicate The State Of the Reference Input Clock Transition.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ . . . . ±20mA
DC Output Diode Current, I_{OK}
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ . . . . ±25mA
DC V_{CC} or Ground Current, $I_{CC\text{ or }}I_{GND}$ . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . -55^{o}C to 125^{o}C
Supply Voltage Range, V_{CC}
HC Types . . . . .2V to 6V
HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
E (PDIP) Package	80
M (SOIC) Package	86

Maximum Junction Temperature . . . . 150^{o}C
Maximum Storage Temperature Range . . . .-65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . 300^{o}C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TEST CONDITIONS			25^{o}C			-40^{o}C TO 85^{o}C		-55^{o}C TO 125^{o}C		
PARAMETER	**SYMBOL**	**V_I (V)**	**I_O (mA)**	**V_{CC} (V)**	**MIN**	**TYP**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

		TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	V_I (V)	I_O (mA)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
Date Shift-In (1, 2)	0.3
$\overline{MR}$	0.9
Clock	0.7

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

Prerequisite For Switching Function

			25°C		-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	V_{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES									
Maximum Clock Frequency	f_{MAX}	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
$\overline{MR}$ Pulse Width	t_W	2	60	-	75	-	90	-	ns
		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns

Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	25^{o}C		-40^{o}C TO 85^{o}C		-55^{o}C TO 125^{o}C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
CP Pulse Width	t_W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Set-up Time	t_{SU}	2	60	-	75	-	90	-	ns
		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns
Hold Time	t_H	2	4	-	4	-	4	-	ns
		4.5	4	-	4	-	4	-	ns
		6	4	-	4	-	4	-	ns
$\overline{MR}$ to Clock, Removal Time	t_{REM}	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
HCT TYPES									
Maximum Clock Frequency	f_{MAX}	4.5	27	-	22	-	18	-	MHz
$\overline{MR}$ Pulse Width	t_w	6	18	-	23	-	27	-	ns
CP Pulse Width	t_w	4.5	18	-	23	-	27	-	ns
Set-up Time	t_{SU}	6	12	-	15	-	18	-	ns
Hold Time	t_H	4.5	4	-	4	-	4	-	ns
$\overline{MR}$ to Clock, Removal Time	t_{REM}	6	16	-	20	-	24	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25^{o}C		-40^{o}C TO 85^{o}C	-55^{o}C TO 125^{o}C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, CP to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	170	212	255	ns
			4.5	-	34	43	51	ns
		C_L = 15pF	5	14	-	-	-	ns
		C_L = 50pF	6	-	29	36	43	ns
$\overline{MR}$ to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	140	175	210	ns
			4.5	-	28	35	42	ns
		C_L = 15pF	5	11	-	-	-	ns
		C_L = 50pF	6	-	24	30	36	ns
Output Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	2	-	75	-	110	ns
			4.5	-	15	-	22	ns
			6	-	13	-	19	ns
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	5	60	-	-	-	MHz
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25^{o}C		-40^{o}C TO 85^{o}C	-55^{o}C TO 125^{o}C	UNITS
				TYP	MAX	MAX	MAX	
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	47	-	-	-	pF
HCT TYPES								
Propagation Delay, CP to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	36	45	54	ns
		C_L = 15pF	5	15	-	-	-	ns
$\overline{MR}$ to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	38	46	57	ns
		C_L = 15pF	5	16	-	-	-	ns
Output Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	15	19	22	ns
Input Capacitance	C_{IN}	-	-	-	-	-	-	pF
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	-	54	-	-	-	MHz
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	49	10	10	10	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per device.
4. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

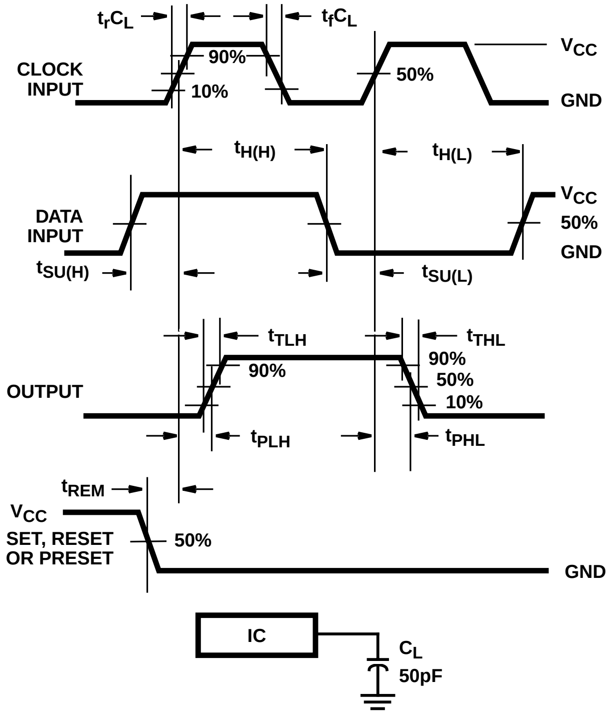


FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

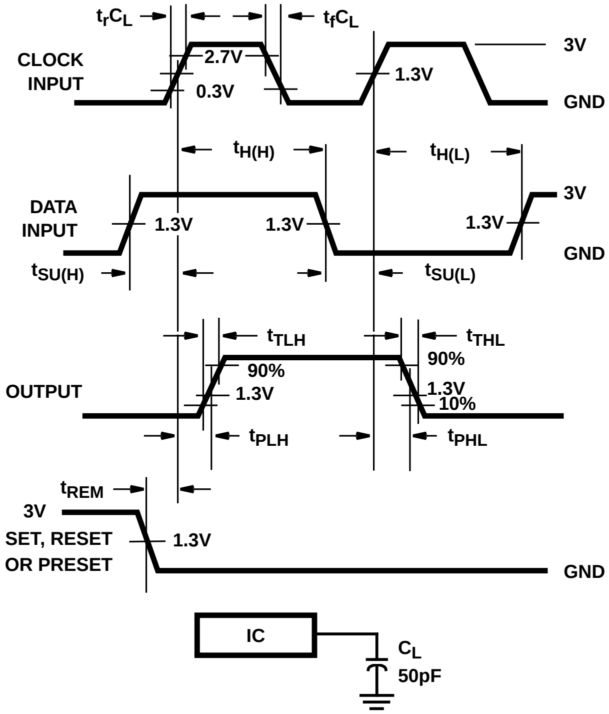


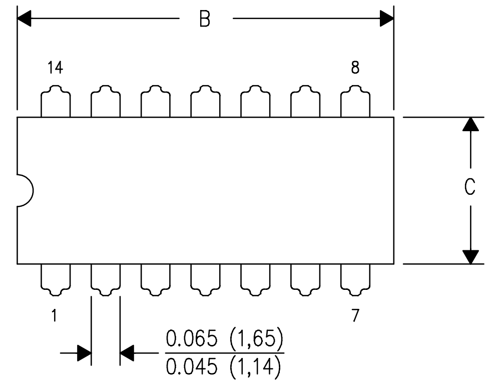
FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

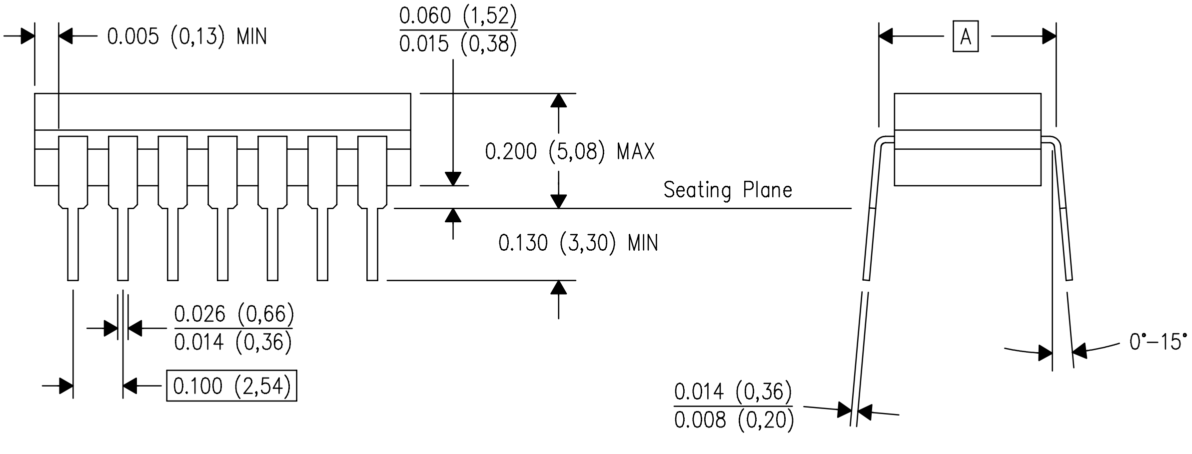
J (R−GDIP−T**)

CERAMIC DUAL IN−LINE PACKAGE

14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



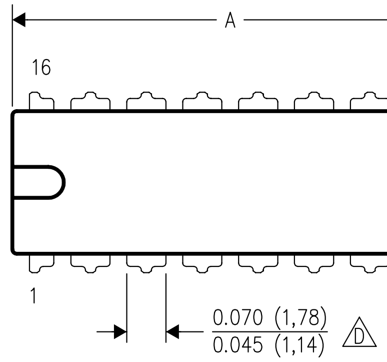


4040083/F 03/03

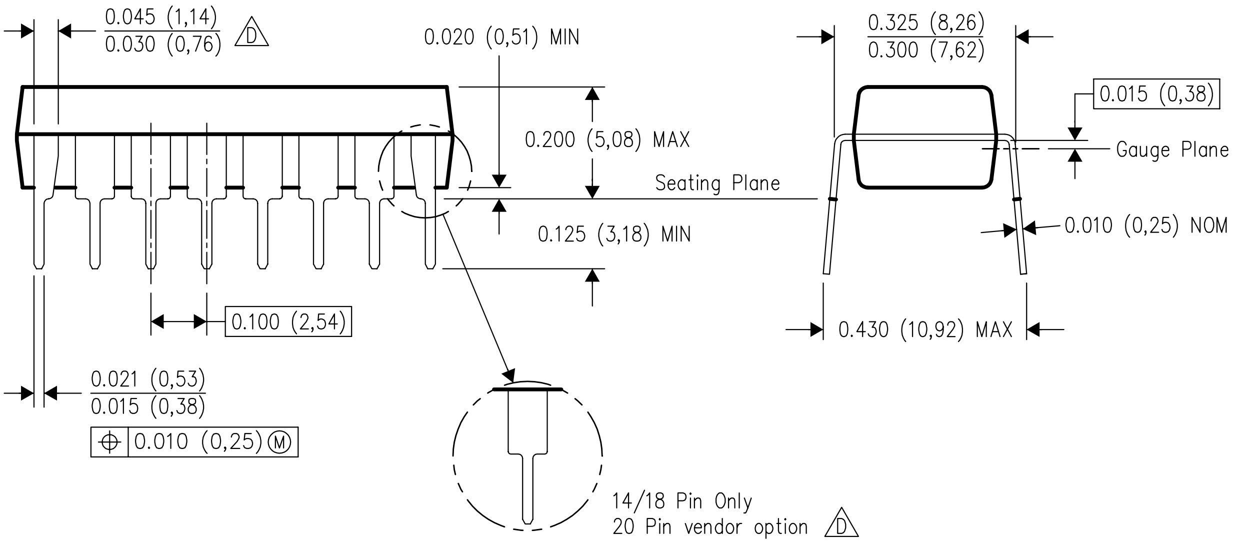
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



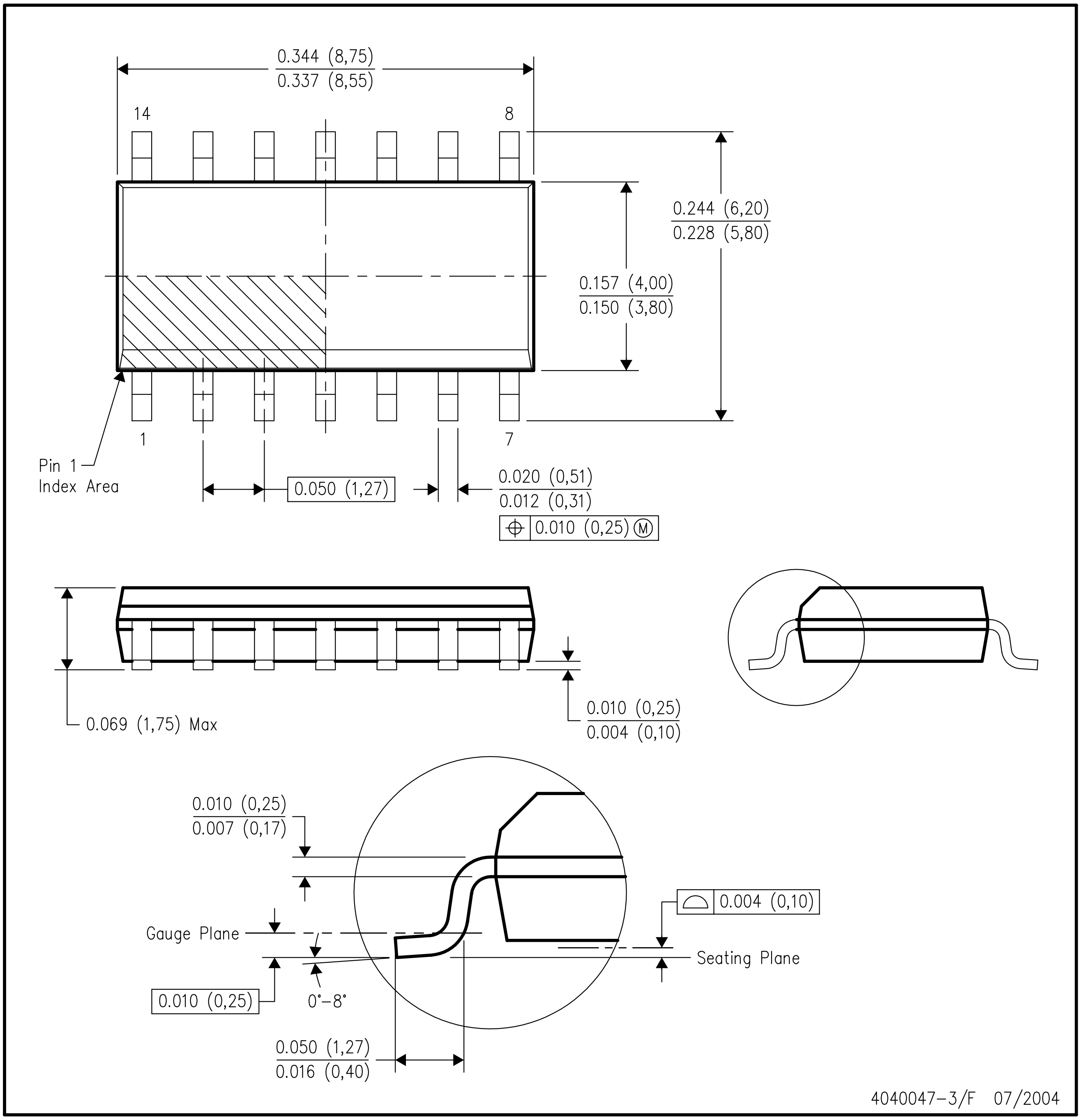
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
△D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AB.

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