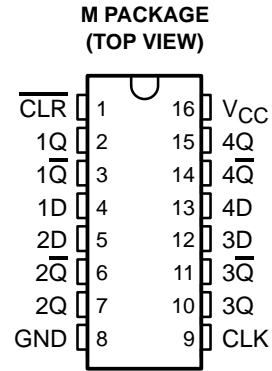


# CD74AC175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Buffered Inputs
- Contains Four Flip-Flops With Double-Rail Outputs
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- $\pm 24$ -mA Output Drive Current
  - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators



## description/ordering information

This positive-edge-triggered D-type flip-flop has a direct clear ( $\overline{\text{CLR}}$ ) input. The CD74AC175 features complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

## ORDERING INFORMATION

| $T_A$          | PACKAGE† |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------|---------------|-----------------------|------------------|
| –55°C to 125°C | SOIC – M | Tube          | CD74AC175M            | AC175M           |
|                |          | Tape and reel | CD74AC175M96          |                  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each flip-flop)

| INPUTS                  |     |   | OUTPUTS |                       |
|-------------------------|-----|---|---------|-----------------------|
| $\overline{\text{CLR}}$ | CLK | D | Q       | $\overline{\text{Q}}$ |
| L                       | X   | X | L       | H                     |
| H                       | ↑   | H | H       | L                     |
| H                       | ↑   | L | L       | H                     |
| H                       | L   | X | $Q_0$   | $\overline{Q_0}$      |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

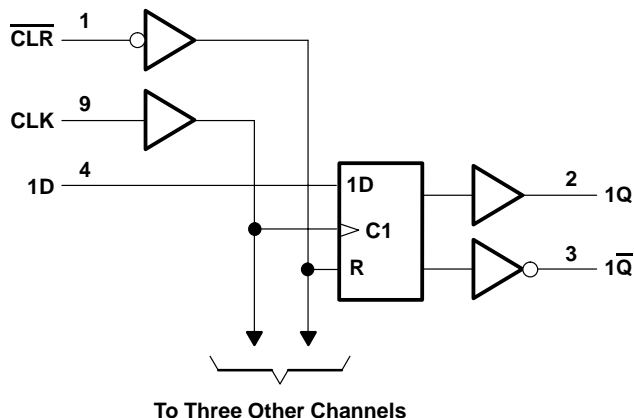
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# CD74AC175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |       |                |
|---|-------|----------------|
| Supply voltage range, $V_{CC}$  | ..... | -0.5 V to 6 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ V or $V_I > V_{CC}$ ) (see Note 1)  | ..... | $\pm 20$ mA    |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ V or $V_O > V_{CC}$ ) (see Note 1) | ..... | $\pm 50$ mA    |
| Continuous output current, $I_O$ ( $V_O > 0$ V or $V_O < V_{CC}$ )            | ..... | $\pm 50$ mA    |
| Continuous current through $V_{CC}$ or GND                                    | ..... | $\pm 200$ mA   |
| Package thermal impedance, $\theta_{JA}$ (see Note 2)                         | ..... | 73°C/W         |
| Storage temperature range, $T_{stg}$  | ..... | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

|                     |                                    | $T_A = 25^\circ\text{C}$  |          | $-55^\circ\text{C to } 125^\circ\text{C}$ |          | $-40^\circ\text{C to } 85^\circ\text{C}$ |          | UNIT |
|---------------------|------------------------------------|---------------------------|----------|---|----------|--|----------|------|
|                     |                                    | MIN                       | MAX      | MIN                                       | MAX      | MIN                                      | MAX      |      |
| $V_{CC}$            | Supply voltage                     | 1.5                       | 5.5      | 1.5                                       | 5.5      | 1.5                                      | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 1.5$ V          |          | 1.2                                       |          | 1.2                                      |          | V    |
|                     |                                    | $V_{CC} = 3$ V            |          | 2.1                                       |          | 2.1                                      |          |      |
|                     |                                    | $V_{CC} = 5.5$ V          |          | 3.85                                      |          | 3.85                                     |          |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 1.5$ V          |          | 0.3                                       |          | 0.3                                      |          | V    |
|                     |                                    | $V_{CC} = 3$ V            |          | 0.9                                       |          | 0.9                                      |          |      |
|                     |                                    | $V_{CC} = 5.5$ V          |          | 1.65                                      |          | 1.65                                     |          |      |
| $V_I$               | Input voltage                      | 0                         | $V_{CC}$ | 0   | $V_{CC}$ | 0  | $V_{CC}$ | V    |
| $V_O$               | Output voltage                     | 0                         | $V_{CC}$ | 0   | $V_{CC}$ | 0  | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 4.5$ V to 5.5 V |          | -24                                       |          | -24                                      |          | mA   |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 4.5$ V to 5.5 V |          | 24  |          | 24                                       |          |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 1.5$ V to 3 V   |          | 50  |          | 50                                       |          | ns/V |
|                     |                                    | $V_{CC} = 3.6$ V to 5.5 V |          | 20  |          | 20                                       |          |      |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER       | TEST CONDITIONS   | V <sub>CC</sub>          | T <sub>A</sub> = 25°C |      | –55°C to 125°C |      | –40°C to 85°C |      | UNIT |
|-----------------|---|--------------------------|-----------------------|------|----------------|------|---------------|------|------|
|                 |   |                          | MIN                   | MAX  | MIN            | MAX  | MIN           | MAX  |      |
| V <sub>OH</sub> | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>         | I <sub>OH</sub> = –50 μA | 1.5 V                 | 1.4  | 1.4            | 1.4  |               |      | V    |
|                 |   |                          | 3 V                   | 2.9  | 2.9            | 2.9  |               |      |      |
|                 |   |                          | 4.5 V                 | 4.4  | 4.4            | 4.4  |               |      |      |
|                 |   | I <sub>OH</sub> = –4 mA  | 3 V                   | 2.58 | 2.4            | 2.48 |               |      |      |
|                 |   |                          | 4.5 V                 | 3.94 | 3.7            | 3.8  |               |      |      |
|                 |   |                          | 5.5 V                 |      | 3.85           |      |               |      |      |
| V <sub>OL</sub> | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>         | I <sub>OL</sub> = 50 μA  | 1.5 V                 |      | 0.1            | 0.1  |               | 0.1  | V    |
|                 |   |                          | 3 V                   |      | 0.1            | 0.1  |               | 0.1  |      |
|                 |   |                          | 4.5 V                 |      | 0.1            | 0.1  |               | 0.1  |      |
|                 |   | I <sub>OL</sub> = 12 mA  | 3 V                   |      | 0.36           | 0.5  |               | 0.44 |      |
|                 |   |                          | 4.5 V                 |      | 0.36           | 0.5  |               | 0.44 |      |
|                 |   | I <sub>OL</sub> = 50 mA† | 5.5 V                 |      |                | 1.65 |               |      |      |
|                 |   |                          | 5.5 V                 |      |                |      |               | 1.65 |      |
| I <sub>I</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5.5 V                    |                       | ±0.1 | ±1             | ±1   | μA            |      |      |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V                    |                       | 8    | 160            | 80   | μA            |      |      |
| C <sub>i</sub>  |   |                          |                       | 10   | 10             | 10   | pF            |      |      |

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 1.5 V (unless otherwise noted)**

|                    |                            | –55°C to 125°C      |     | –40°C to 85°C |     | UNIT |
|--------------------|----------------------------|---------------------|-----|---------------|-----|------|
|                    |                            | MIN                 | MAX | MIN           | MAX |      |
| f <sub>clock</sub> | Clock frequency            |                     | 8   |               | 9   | MHz  |
| t <sub>w</sub>     | Pulse duration             | CL <sub>R</sub> low | 50  |               | 44  | ns   |
|                    |                            | CLK high or low     | 63  |               | 55  |      |
| t <sub>su</sub>    | Setup time before CLK↑     | Data                | 2   |               | 2   | ns   |
| t <sub>h</sub>     | Hold time, data after CLK↑ |                     | 2   |               | 2   | ns   |
| t <sub>rec</sub>   | Recovery time, before CLK↑ | CL <sub>R</sub> ↑   | 1   |               | 1   | ns   |

**CD74AC175**  
**QUADRUPLE D-TYPE FLIP-FLOP**  
**WITH CLEAR**

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted)**

|             |                            | -55°C to 125°C  |     | -40°C to 85°C |     | UNIT |
|-------------|----------------------------|-----------------|-----|---------------|-----|------|
|             |                            | MIN             | MAX | MIN           | MAX |      |
| $f_{clock}$ | Clock frequency            | 71              |     | 81            |     | MHz  |
| $t_w$       | Pulse duration             | CLR low         |     | 5.6           | 4.9 | ns   |
|             |                            | CLK high or low |     | 7             | 6.1 |      |
| $t_{su}$    | Setup time before CLK↑     | Data            |     | 2             | 2   | ns   |
| $t_h$       | Hold time, data after CLK↑ |                 |     | 2             | 2   | ns   |
| $t_{rec}$   | Recovery time, before CLK↑ | CLR↑            |     | 1             | 1   | ns   |

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted)**

|             |                            | -55°C to 125°C  |     | -40°C to 85°C |     | UNIT |
|-------------|----------------------------|-----------------|-----|---------------|-----|------|
|             |                            | MIN             | MAX | MIN           | MAX |      |
| $f_{clock}$ | Clock frequency            | 100             |     | 114           |     | MHz  |
| $t_w$       | Pulse duration             | CLR low         |     | 4             | 3.5 | ns   |
|             |                            | CLK high or low |     | 5             | 4.4 |      |
| $t_{su}$    | Setup time before CLK↑     | Data            |     | 2             | 2   | ns   |
| $t_h$       | Hold time, data after CLK↑ |                 |     | 2             | 2   | ns   |
| $t_{rec}$   | Recovery time, before CLK↑ | CLR↑            |     | 1             | 1   | ns   |

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 1.5 V, C_L = 50 pF$  (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C |     | -40°C to 85°C |     | UNIT |
|-----------|--------------|-------------|----------------|-----|---------------|-----|------|
|           |              |             | MIN            | MAX | MIN           | MAX |      |
| $f_{max}$ |              |             | 8              |     | 9             |     | MHz  |
| $t_{PLH}$ | CLK          | Any Q       | 153            |     | 139           |     | ns   |
| $t_{PHL}$ |              |             | 153            |     | 139           |     |      |
| $t_{PLH}$ | CLR          | Any Q       | 153            |     | 139           |     | ns   |
| $t_{PHL}$ |              |             | 153            |     | 139           |     |      |

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V, C_L = 50 pF$  (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C |      | -40°C to 85°C |      | UNIT |
|-----------|--------------|-------------|----------------|------|---------------|------|------|
|           |              |             | MIN            | MAX  | MIN           | MAX  |      |
| $f_{max}$ |              |             | 71             |      | 81            |      | MHz  |
| $t_{PLH}$ | CLK          | Any Q       | 4.3            | 17.1 | 4.4           | 15.5 | ns   |
| $t_{PHL}$ |              |             | 4.3            | 17.1 | 4.4           | 15.5 |      |
| $t_{PLH}$ | CLR          | Any Q       | 4.3            | 17.1 | 4.4           | 15.5 | ns   |
| $t_{PHL}$ |              |             | 4.3            | 17.1 | 4.4           | 15.5 |      |



switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT)         | TO<br>(OUTPUT) | -55°C to<br>125°C |      | -40°C to<br>85°C |      | UNIT |
|-----------|-------------------------|----------------|-------------------|------|------------------|------|------|
|           |                         |                | MIN               | MAX  | MIN              | MAX  |      |
| $f_{max}$ |                         |                | 100               |      | 114              |      | MHz  |
| $t_{PLH}$ | CLK                     | Any Q          | 3.1               | 12.2 | 3.2              | 11.1 | ns   |
| $t_{PHL}$ |                         |                | 3.1               | 12.2 | 3.2              | 11.1 |      |
| $t_{PLH}$ | $\overline{\text{CLR}}$ | Any Q          | 3.1               | 12.2 | 3.2              | 11.1 | ns   |
| $t_{PHL}$ |                         |                | 3.1               | 12.2 | 3.2              | 11.1 |      |

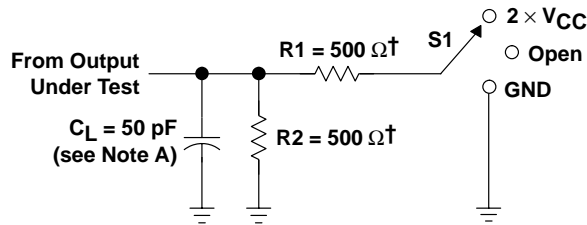
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TYP | UNIT |
|-----------|-------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | 55  | pF   |

# CD74AC175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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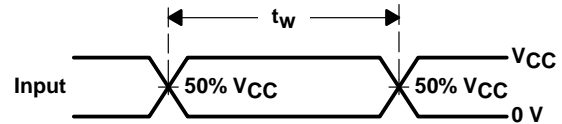
## PARAMETER MEASUREMENT INFORMATION



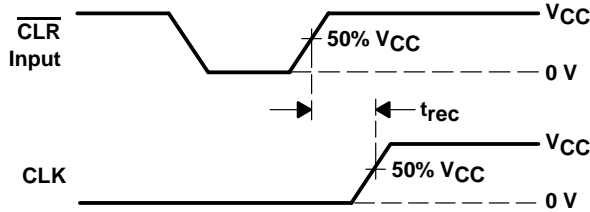
† When  $V_{CC} = 1.5 \text{ V}$ ,  $R1 = R2 = 1 \text{ k}\Omega$

LOAD CIRCUIT

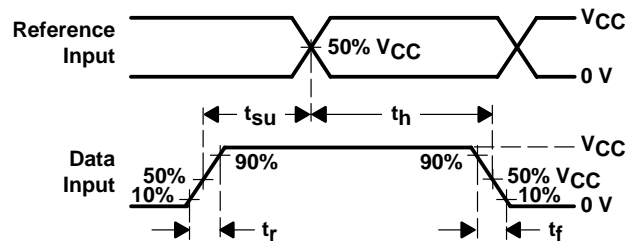
| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |



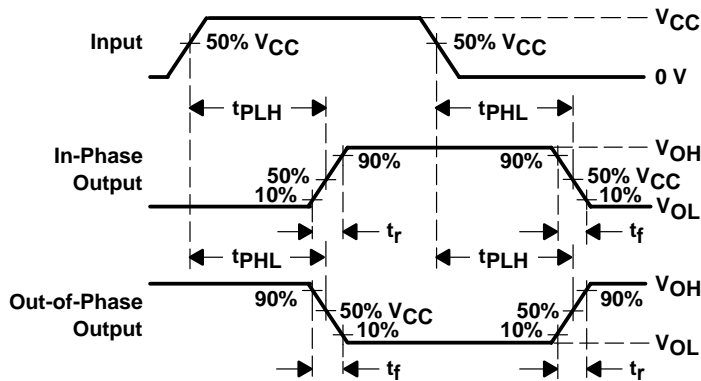
VOLTAGE WAVEFORMS  
PULSE DURATION



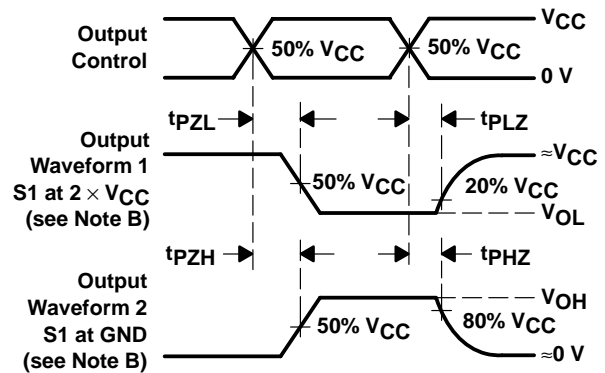
VOLTAGE WAVEFORMS  
RECOVERY TIME



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS  
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
  - For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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| Telephony          | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
| Video & Imaging    | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
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**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD74AC175M       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74AC175M96     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74AC175M96E4   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74AC175M96G4   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74AC175ME4     | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74AC175MG4     | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74AC175NSR     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74AC175NSRE4   | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74AC175NSRG4   | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



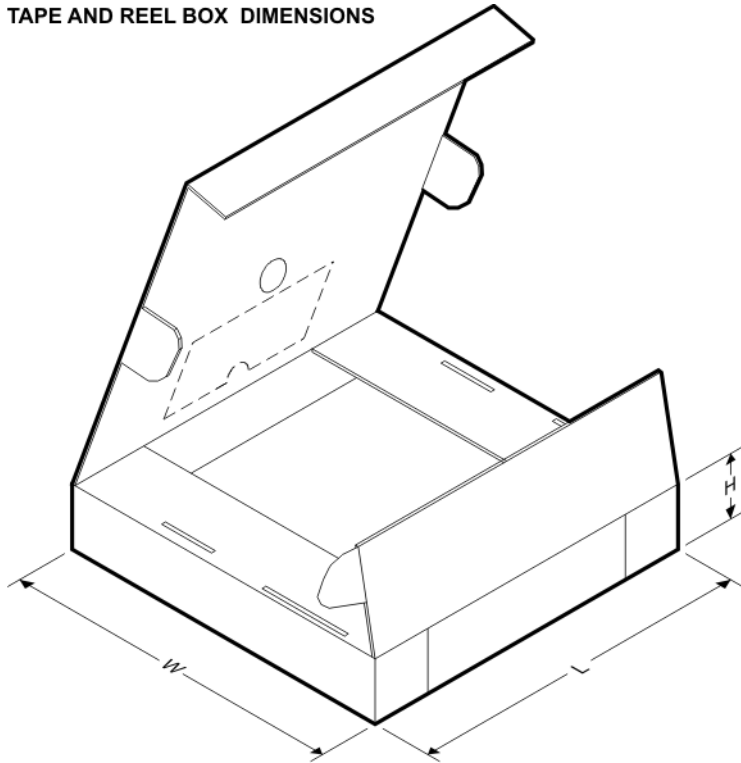
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC175M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74AC175NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74AC175M96 | SOIC         | D               | 16   | 2500 | 342.9       | 345.9      | 28.6        |
| CD74AC175NSR | SO           | NS              | 16   | 2000 | 346.0       | 346.0      | 33.0        |

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

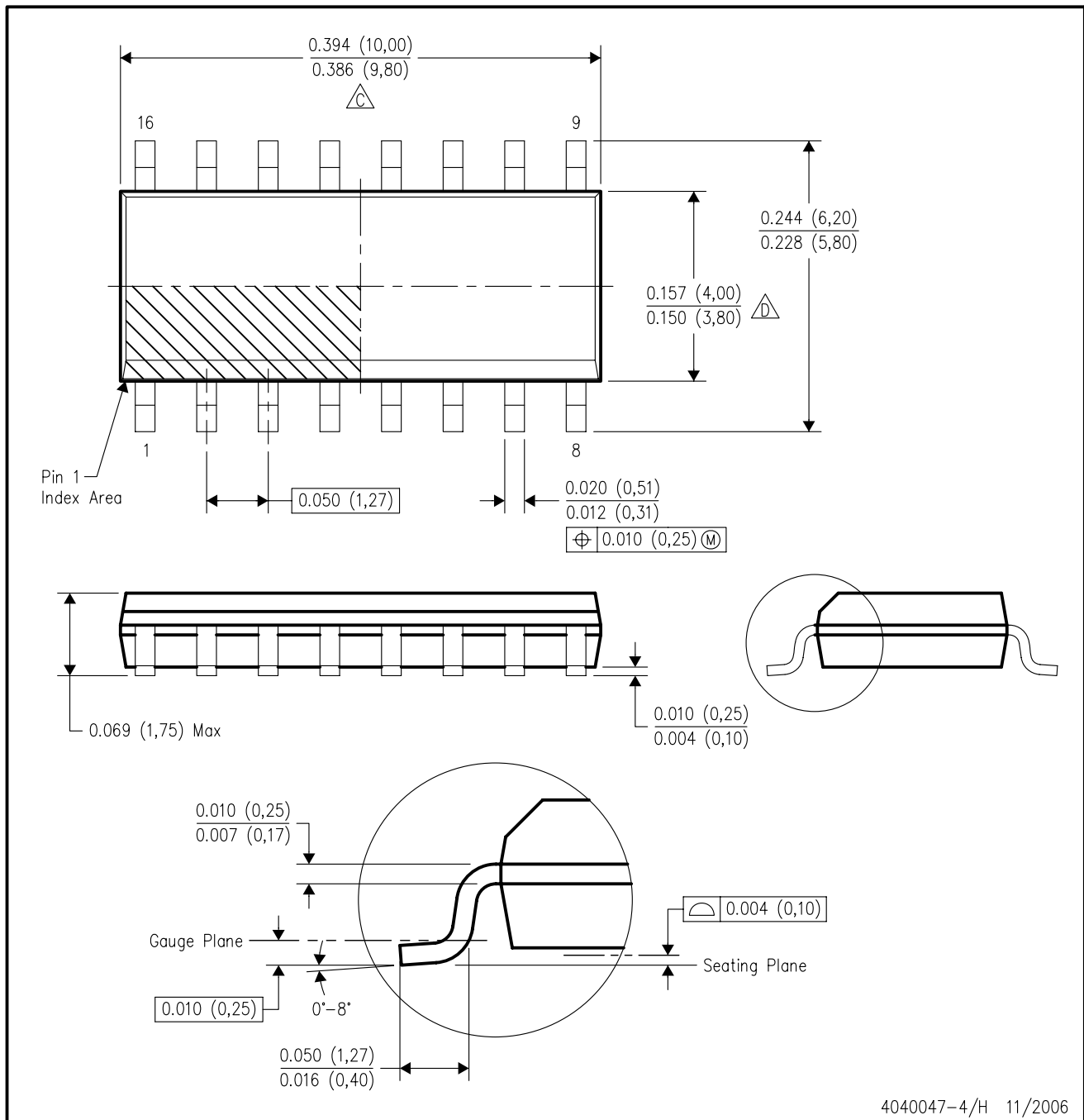
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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