

CD4060B Types

CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

High-Voltage Types (20-Volt Rating)

■ CD4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_1 (and ϕ_0). All inputs and outputs are fully buffered. Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

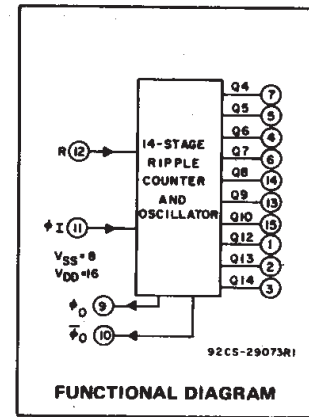
The CD4060B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- 12 MHz clock rate at 15 V
- Common reset
- Fully static operation
- Buffered inputs and outputs
- Schmitt trigger input-pulse line
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for description of "B" Series CMOS Devices"

Oscillator Features:

- All active components on chip
- RC or crystal oscillator configuration
- RC oscillator frequency of 690 kHz min. at 15 V



Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

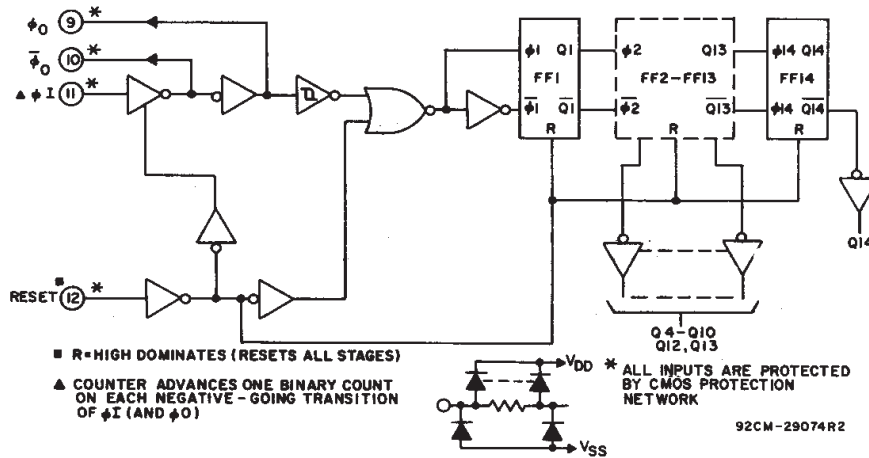


Fig. 1 – Logic diagram.

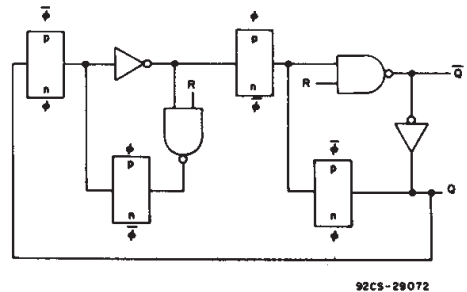


Fig. 2 – Detail of typical flip-flop stage.

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|---|
| DC SUPPLY-VOLTAGE RANGE, (V_{DD}) | -0.5V to +20V |
| Voltages referenced to V_{SS} Terminal | |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to $V_{DD} + 0.5V$ |
| DC INPUT CURRENT, ANY ONE INPUT | $\pm 10\text{mA}$ |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ | 500mW |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T_A) | -55°C to $+125^\circ\text{C}$ |
| STORAGE TEMPERATURE RANGE (T_{stg}) | -65°C to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{mm}$) from case for 10s max | $+265^\circ\text{C}$ |

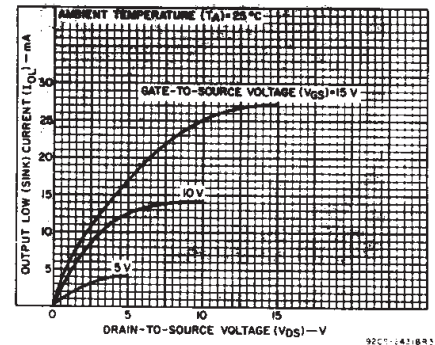


Fig. 3 – Typical n-channel output low (sink) current characteristics.

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STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | — | 0,5 | 5 | 5 | 5 | 150 | 150 | — | 0,04 | 5 | μA |
| | — | 0,10 | 10 | 10 | 10 | 300 | 300 | — | 0,04 | 10 | |
| | — | 0,15 | 15 | 20 | 20 | 600 | 600 | — | 0,04 | 20 | |
| | — | 0,20 | 20 | 100 | 100 | 3000 | 3000 | — | 0,08 | 100 | |
| Output Low (Sink) Current*, I _{OL} Min. | 0,4 | 0,5 | 5 | 0,64 | 0,61 | 0,42 | 0,36 | 0,51 | 1 | — | mA |
| | 0,5 | 0,10 | 10 | 1,6 | 1,5 | 1,1 | 0,9 | 1,3 | 2,6 | — | |
| | 1,5 | 0,15 | 15 | 4,2 | 4 | 2,8 | 2,4 | 3,4 | 6,8 | — | |
| Output High (Source) Current*, I _{OH} Min. | 4,6 | 0,5 | 5 | -0,64 | -0,61 | -0,42 | -0,36 | -0,51 | -1 | — | mA |
| | 2,5 | 0,5 | 5 | -2 | -1,8 | -1,3 | -1,15 | -1,6 | -3,2 | — | |
| | 9,5 | 0,10 | 10 | -1,6 | -1,5 | -1,1 | -0,9 | -1,3 | -2,6 | — | |
| | 13,5 | 0,15 | 15 | -4,2 | -4 | -2,8 | -2,4 | -3,4 | -6,8 | — | |
| Output Voltage: Low-Level, V _{OL} Max. | — | 0,5 | 5 | 0,05 | | | | — | 0 | 0,05 | V |
| | — | 0,10 | 10 | 0,05 | | | | — | 0 | 0,05 | |
| | — | 0,15 | 15 | 0,05 | | | | — | 0 | 0,05 | |
| Output Voltage: High-Level, V _{OH} Min. | — | 0,5 | 5 | 4,95 | | | | 4,95 | 5 | — | V |
| | — | 0,10 | 10 | 9,95 | | | | 9,95 | 10 | — | |
| | — | 0,15 | 15 | 14,95 | | | | 14,95 | 15 | — | |
| Input Low Voltage V _{IL} Max. | 0,5, 4,5 | — | 5 | 1,5 | | | | — | — | 1,5 | V |
| | 1,9 | — | 10 | 3 | | | | — | — | 3 | |
| | 1,5, 13,5 | — | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, V _{IH} Min. | 0,5, 4,5 | — | 5 | 3,5 | | | | 3,5 | — | — | V |
| | 1,9 | — | 10 | 7 | | | | 7 | — | — | |
| | 1,5, 13,5 | — | 15 | 11 | | | | 11 | — | — | |
| Input Current I _{IN} Max. | — | 0,18 | 18 | ±0,1 | ±0,1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0,1 | μA |

* Data not applicable to terminal 9 or 10.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

| CHARACTERISTIC | V _{DD} | LIMITS | | UNITS |
|--|-----------------|-----------|------|-------|
| | | MIN. | MAX. | |
| Supply-Voltage Range (For T _A = Full Package Temperature Range) | — | 3 | 18 | V |
| Input-Pulse Width, t _W (f = 100 kHz) | 5 | 100 | — | ns |
| | 10 | 40 | — | |
| | 15 | 30 | — | |
| Input-Pulse Rise Time and Fall Time, t _{rφ} , t _{fφ} | 5 | Unlimited | | |
| | 10 | Unlimited | | |
| | 15 | Unlimited | | |
| Input-Pulse Frequency, f _{φI} (External pulse source) | 5 | — | 3,5 | MHz |
| | 10 | — | 8 | |
| | 15 | — | 12 | |
| Reset Pulse Width, t _W | 5 | 120 | — | ns |
| | 10 | 60 | — | |
| | 15 | 40 | — | |

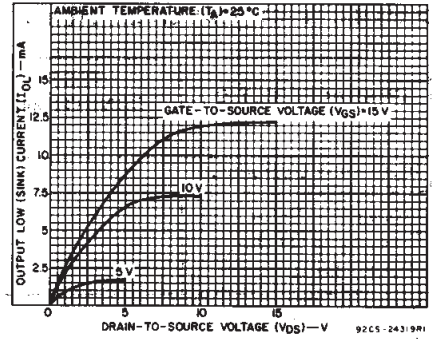


Fig. 4 - Minimum n-channel output low (sink) current characteristics.

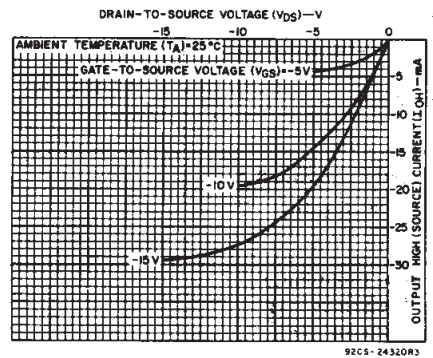


Fig. 5 - Typical p-channel output high (source) current characteristics.

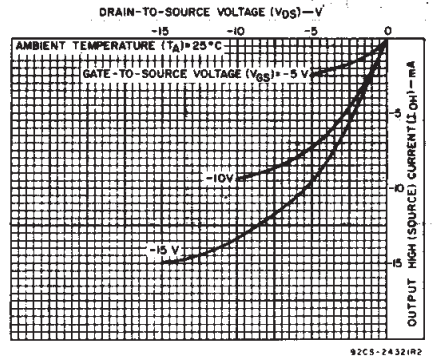


Fig. 6 - Minimum p-channel output high (source) current characteristics.

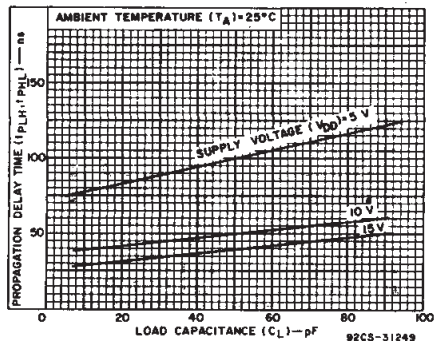


Fig. 7 - Typical propagation delay time (Q_n to Q_{n+1}) as a function of load capacitance.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS | |
|--|----------------------|---------------------|-----------|------|-------|------|
| | | V _{DD} (V) | MIN. | TYP. | | MAX. |
| Input-Pulse Operation | | | | | | |
| Propagation Delay Time, ϕ_I to Q4 Out; t_{PHL}, t_{PLH} | | 5 | — | 370 | 740 | ns |
| | | 10 | — | 150 | 300 | |
| | | 15 | — | 100 | 200 | |
| Propagation Delay Time, Q_n to Q_{n+1} ; t_{PHL}, t_{PLH} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Transition Time, t_{THL}, t_{TLH} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Min. Input-Pulse Width, t_W | $f = 100\text{ kHz}$ | 5 | — | 50 | 100 | ns |
| | | 10 | — | 20 | 40 | |
| | | 15 | — | 15 | 30 | |
| Input-Pulse Rise & Fall Time, $t_{r\phi}, t_{f\phi}$ | | 5 | Unlimited | | | |
| | | 10 | | | | |
| | | 15 | | | | |
| Max. Input-Pulse Frequency, $f_{\phi I}$ (External pulse source) | | 5 | 3.5 | 7 | — | MHz |
| | | 10 | 8 | 16 | — | |
| | | 15 | 12 | 24 | — | |
| Input Capacitance, C_I | Any Input | | — | 5 | 7.5 | pF |
| Reset Operation | | | | | | |
| Propagation Delay Time, t_{PHL} | | 5 | — | 180 | 360 | ns |
| | | 10 | — | 80 | 160 | |
| | | 15 | — | 50 | 100 | |
| Minimum Reset Pulse Width, t_W | | 5 | — | 60 | 120 | ns |
| | | 10 | — | 30 | 60 | |
| | | 15 | — | 20 | 40 | |

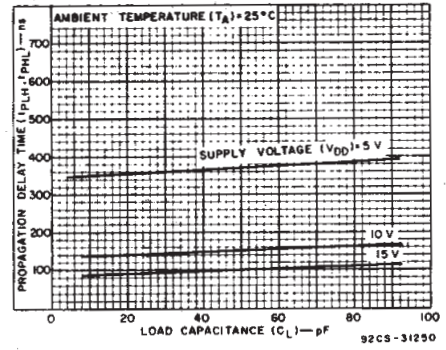


Fig. 8 - Typical propagation delay time (ϕ_I to Q_4 Output) as a function of load capacitance.

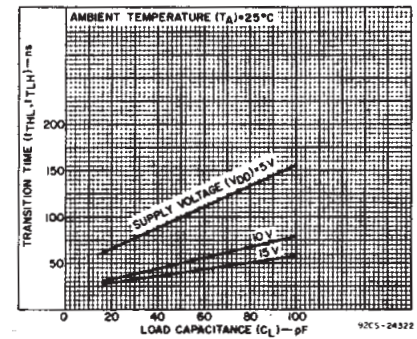


Fig. 9 - Typical transition time as a function of load capacitance.

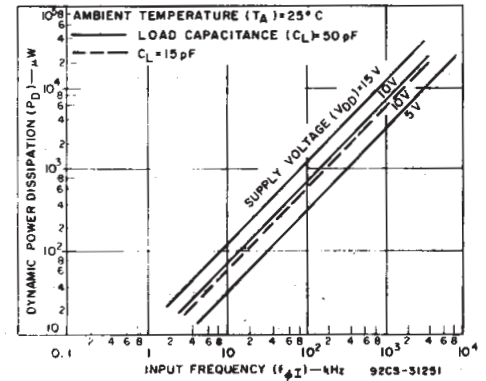


Fig. 10 - Typical dynamic power dissipation as a function of input frequency.

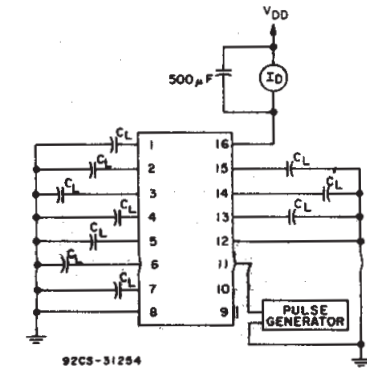


Fig. 11 - Dynamic power dissipation test circuit.

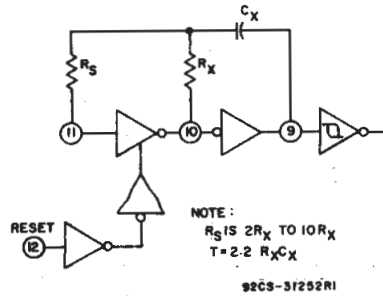


Fig. 12 - Typical RC circuit.

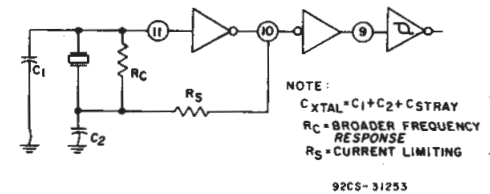


Fig. 13 - Typical crystal circuit.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$ [cont'd]

| CHARACTERISTIC | TEST CONDITIONS | VDD (V) | LIMITS | | | UNITS | |
|--|---|--------------------------|--------|---------------|-------|---------------|----|
| | | | Min. | Typ. | Max. | | |
| RC Operation | | | | | | | |
| Variation of Frequency (Unit-to-Unit) | $C_X = 200 \text{ pF}$, $R_S = 560 \text{ k}\Omega$, $R_X = 50 \text{ k}\Omega$ | 5 | — | $23 \pm 10\%$ | — | kHz | |
| | | 10 | — | $24 \pm 10\%$ | — | | |
| | | 15 | — | $25 \pm 10\%$ | — | | |
| Variation of Frequency with voltage change (Same Unit) | $C_X = 200 \text{ pF}$, $R_S = 560 \text{ k}\Omega$, $R_X = 50 \text{ k}\Omega$ | 5V to 10 V 10V to 15V | — | 1.5 0.5 | — | M Ω | |
| R_X max. | $C_X = 10 \mu\text{F}$ $= 50 \mu\text{F}$ $= 10 \mu\text{F}$ | 5 | — | — | 20 | | |
| | | 10 | — | — | 20 | | |
| | | 15 | — | — | 10 | | |
| C_X max. | $R_X = 500 \text{ k}\Omega$ $= 300 \text{ k}\Omega$ $= 300 \text{ k}\Omega$ | 5 | — | — | 1000 | μF | |
| | | 10 | — | — | 50 | | |
| | | 15 | — | — | 50 | | |
| Maximum Oscillator Frequency* | $R_X = 5 \text{ k}\Omega$ $R_S = 30 \text{ k}\Omega$ $C_X = 15 \text{ pF}$ | 10 | 530 | 650 | 810 | kHz | |
| | | 15 | 690 | 800 | 940 | | |
| Drive Current at Pin 9 (For Oscillator Design) | I_{OL} | $V_O = 0.4 \text{ V}$ | 5 | 0.16 | 0.35 | — | mA |
| | | $= 0.5 \text{ V}$ | 10 | 0.42 | 0.8 | — | |
| | | $= 1.5 \text{ V}$ | 15 | 1 | 2 | — | |
| | I_{OH} | $V_O = 4.6 \text{ V}$ | 5 | -0.16 | -0.35 | — | |
| | | $= 9.5 \text{ V}$ | 10 | -0.42 | -0.8 | — | |
| | | $= 13.5 \text{ V}$ | 15 | -1 | -2 | — | |

*RC oscillator applications are not recommended at supply voltages below 7 V for $R_X < 50 \text{ k}\Omega$.

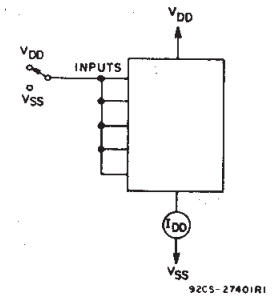


Fig. 14 – Quiescent device current.

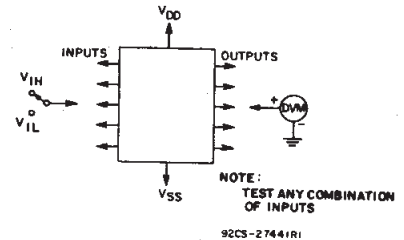


Fig. 15 – Input voltage.

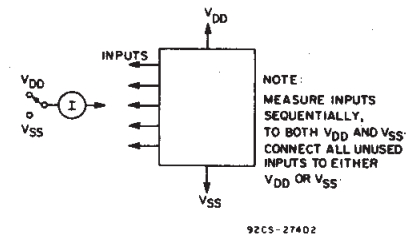
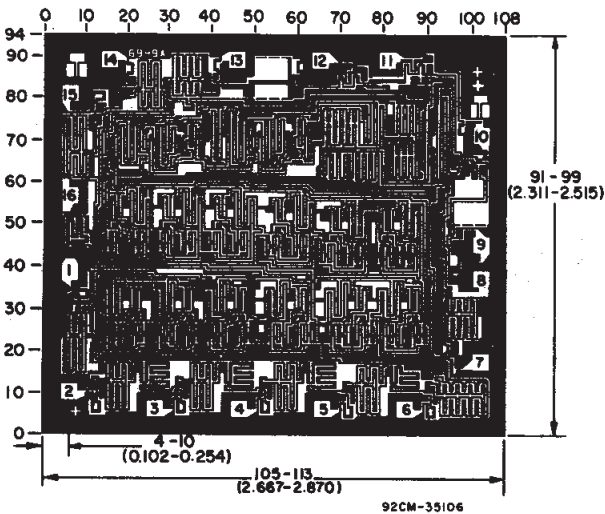


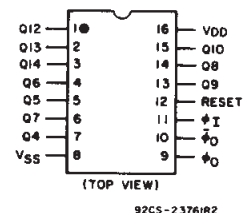
Fig. 16 – Input current.

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Chip dimensions and pad layout for CD4060B

TERMINAL DIAGRAM



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4060BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4060BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4060BF | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4060BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4060BM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BM96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BM96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BM96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BMG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BMT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BMTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BMTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4060BPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4060BM96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4060BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4060BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4060BM96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD4060BNSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| CD4060BPWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



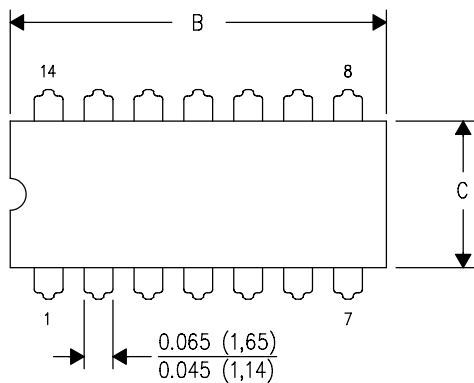
4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

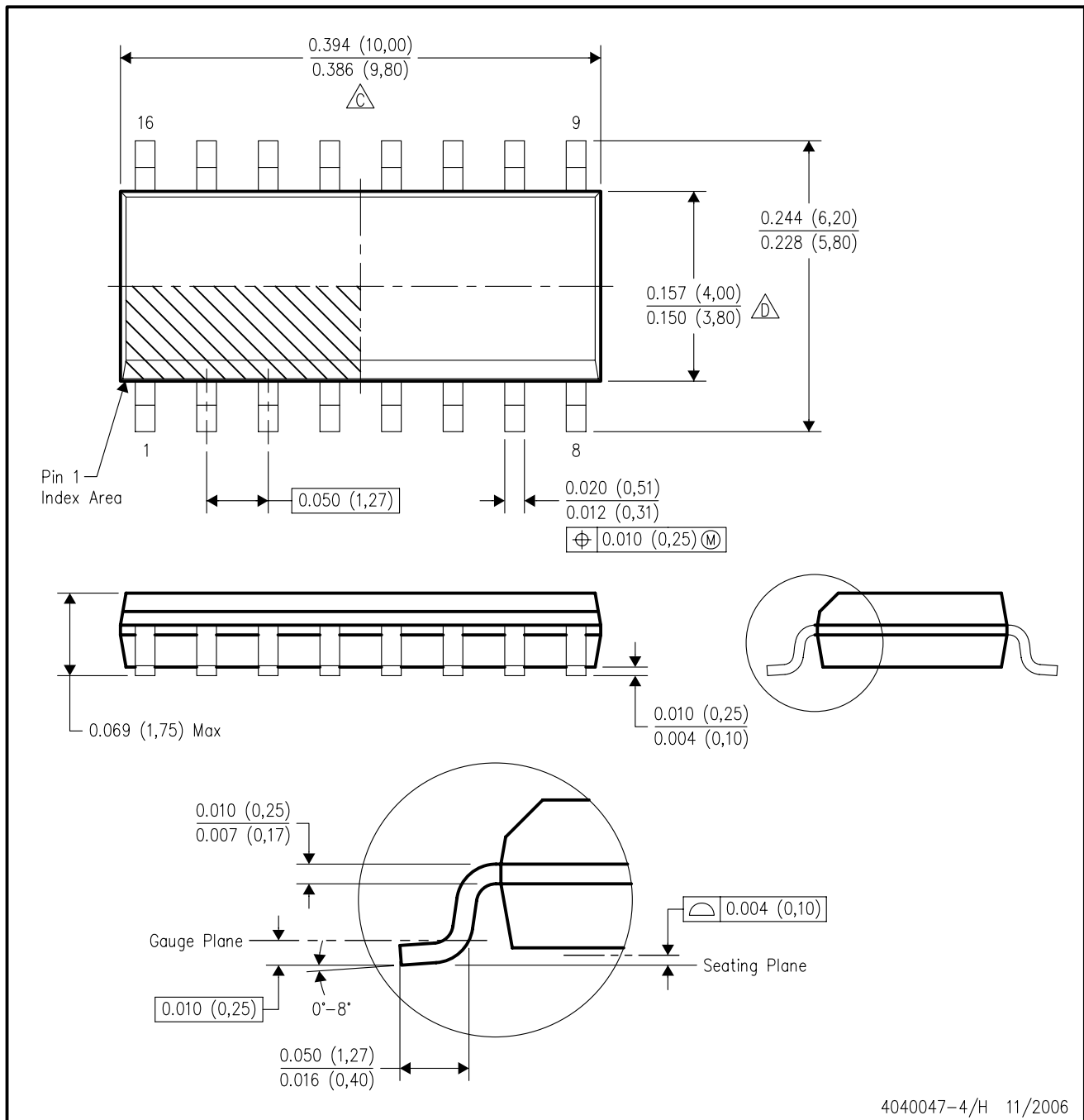


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

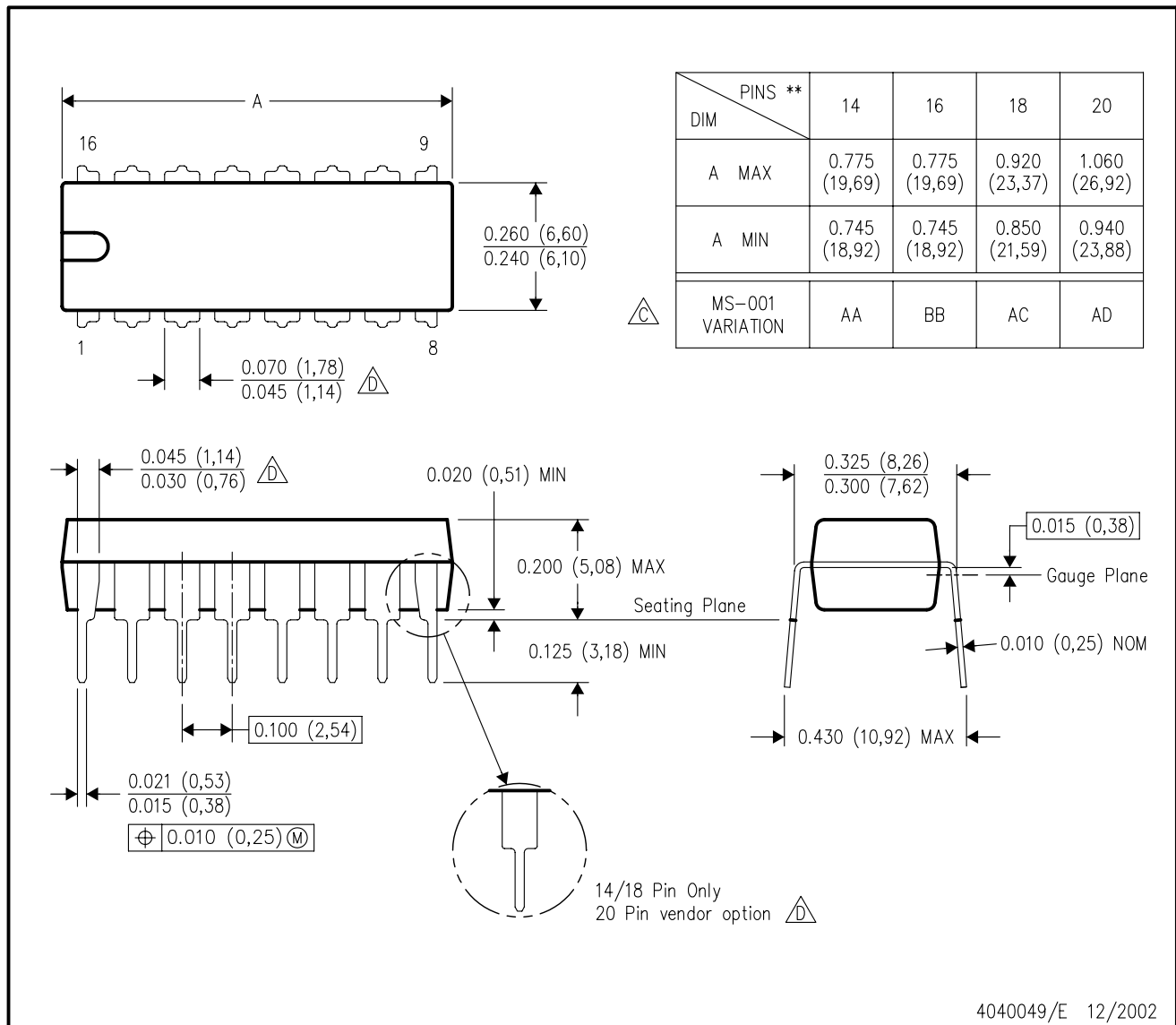


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.