Programmable Gamma-Voltage Generator and High Slew Rate V_{COM} with Integrated Two-Bank Memory

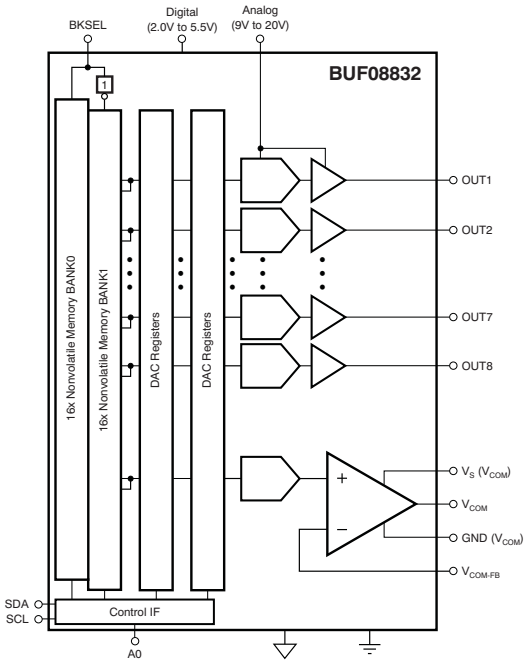
Check for Samples: BUF08832

FEATURES

- **10-BIT RESOLUTION**
- **8-CHANNEL P-GAMMA**
- **1-CHANNEL P-V_{COM}**
- **HIGH SLEW RATE V_{COM}: 45V/µs**
- **16x REWRITABLE NONVOLATILE MEMORY**
- **TWO INDEPENDENT PIN-SELECTABLE MEMORY BANKS**
- **RAIL-TO-RAIL OUTPUT**
  - **300mV Min Swing-to-Rail (10mA)**
  - **> 300mA Max I_{OUT}**
- **LOW SUPPLY CURRENT**
- **SUPPLY VOLTAGE: 9V to 20V**
- **DIGITAL SUPPLY: 2V to 5.5V**
- **TWO-WIRE INTERFACE: Supports 400kHz and 3.4MHz**

APPLICATIONS

- **TFT-LCD REFERENCE DRIVERS**



DESCRIPTION

The BUF08832 offers eight programmable gamma channels and one programmable V_{COM} channel.

The final gamma and V_{COM} values can be stored in the on-chip, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF08832 supports up to 16 write operations to the on-chip memory.

The BUF08832 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate switching between gamma curves.

All gamma and V_{COM} channels offer a rail-to-rail output that typically swings to within 150mV of either supply rail with a 10mA load. All channels are programmed using a Two-Wire interface that supports standard operations up to 400kHz and high-speed data transfers up to 3.4MHz.

The BUF08832 is manufactured using Texas Instruments' proprietary, state-of-the-art, high-voltage CMOS process. This process offers very dense logic and high supply voltage operation of up to 20V. The BUF08832 is offered in a HTSSOP-20 PowerPAD™ package, and is specified from –40°C to +85°C.

RELATED PRODUCTS

FEATURES	PRODUCT
22-Channel Gamma Correction Buffer	BUF22821
16-Channel Gamma Correction Buffer	BUF16821
12-Channel Gamma Correction Buffer	BUF12800
18-/20-Channel Programmable Buffer, 10-Bit, V_{COM}	BUF20800
18-/20-Channel Programmable Buffer with Memory	BUF20820
Programmable V_{COM} Driver	BUF01900
18V Supply, Traditional Gamma Buffers	BUF11704
22V Supply, Traditional Gamma Buffers	BUF11705

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING
BUF08832	HTSSOP-20	PWP	BUF08832

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER			BUF08832	UNIT
Supply Voltage		V_S	+22	V
Supply Voltage		V_{SD}	+6	V
Digital Input Pins, SCL, SDA, AO, BKSEL: Voltage			–0.5 to +6	V
Digital Input Pins, SCL, SDA, AO, BKSEL: Current			±10	mA
Output Pins, OUT1 through OUT16, $V_{COM}1$ and $V_{COM}2$(2)			(V–) – 0.5 to (V+) + 0.5	V
Output Short-Circuit(3)			Continuous	
Ambient Operating Temperature			–40 to +95	°C
Ambient Storage Temperature			–65 to +150	°C
Junction Temperature		T_J	+125	°C
ESD Rating	Human Body Model	HBM	4000	V
	Charged Device Model	CDM	1000	V
	Machine Model	MM	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) See the *Output Protection* section.
(3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS

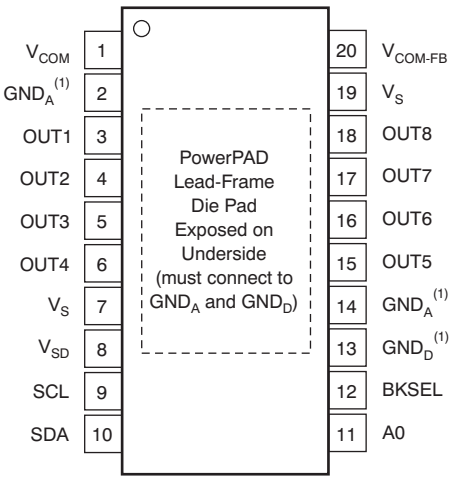
Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**
At T_A = +25°C, V_S = +18V, V_{SD} = +2V, and C_L = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF08832 MIN	BUF08832 TYP	BUF08832 MAX	UNIT
ANALOG GAMMA BUFFER CHANNELS						
Reset Value		Code 512		9		V
OUT 1, 8 Output Swing: High		**Code = 1023, Sourcing 10mA**	**17.7**	**17.85**		**V**
OUT 1, 8 Output Swing: Low		**Code = 0, Sinking 10mA**		**0.07**	**0.3**	**V**
OUT 2-7 Output Swing: High		**Code = 1023, Sourcing 10mA**	**17.5**	**17.85**		**V**
OUT 2-7 Output Swing: Low		**Code = 0, Sinking 10mA**		**0.07**	**0.5**	**V**
V_{COM} Output Swing: High(1)		**Sourcing/Sinking 400mA, G = 2**	**14**	**15.3**		**V**
V_{COM} Output Swing: Low(1)		**Sourcing/Sinking 400mA, G = 2**		**3.8**	**5**	**V**
V_{COM} Slew Rate(2)		R_{LOAD} = 60Ω, C_{LOAD} = 100pF		45		V/µs
Continuous Output Current		Note (3)		30		mA
Output Accuracy(4)		V_{COM}, codes 0 - 960; OUT 1 - 8, codes 0 - 1023		±20	±50	mV
vs Temperature		**Code 512**		**±25**		**µV/°C**
Integral Nonlinearity(4)	INL			0.3		LSB
Differential Nonlinearity(4)	DNL			0.3		LSB
Load Regulation, 10mA	REG	Code 512 or V_{CC}/2, I_{OUT} = +5mA to –5mA Step		0.5	1.5	mV/mA
OTP MEMORY						
Number of OTP Write Cycles					16	Cycles
Memory Retention				100		Years
ANALOG POWER SUPPLY						
Operating Range			9		20	V
Total Analog Supply Current	I_S	Outputs at Reset Values, No Load		8.5	11	mA
Over Temperature					**11**	**mA**
DIGITAL						
Logic 1 Input Voltage	V_{IH}		0.7 × V_{SD}			V
Logic 0 Input Voltage	V_{IL}				0.3 × V_{SD}	V
Logic 0 Output Voltage	V_{OL}	I_{SINK} = 3mA		0.15	0.4	V
Input Leakage				±0.01	±10	µA
Clock Frequency	**f_{CLK}**	**Standard/Fast Mode**			**400**	**kHz**
		High-Speed Mode			**3.4**	**MHz**
DIGITAL POWER SUPPLY						
Operating Range	V_{SD}		2.0		5.5	V
Digital Supply Current(3)	I_{SD}	Outputs at Reset Values, No Load, Two-Wire Bus Inactive		115	180	µA
Over Temperature				**115**		**µA**
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range		Junction Temperature < +125°C	–40		+95	°C
Storage Range			–65		+150	°C
Thermal Resistance(3)	θ_{JA}					
HTSSOP-20		See Note (5)		40		°C/W

(1) The BUF08832 V_{COM} DAC limits can be programmed. These default limits apply if the device is not programmed. See the Programmable V_{COM} Limit Section.
(2) See Figure 12, *Large-Signal Step Response, V_{COM}*.
(3) Observe maximum power dissipation.
(4) The V_{COM} output voltage is limited to codes 0 through 960; see Figure 3. This limitation is for V_{COM} only and does not affect DAC OUT, 1 through 8.
(5) Thermal pad attached to printed circuit board (PCB), 0lfm airflow, and 76mm × 76mm copper area.

PIN CONFIGURATION

PWP PACKAGE
HTSSOP-20
(TOP VIEW)



NOTE: (1) GND_A and GND_D must be connected together.

PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	V_{COM}	V_{COM}
2	GND_A	Analog ground; must be connected to digital ground (GND_D).
3	OUT1	DAC output 1
4	OUT2	DAC output 2
5	OUT3	DAC output 3
6	OUT4	DAC output 4
7	V_S	V_S connected to analog supply
8	V_{SD}	Digital supply; connect to logic supply
9	SCL	Serial clock input; open-drain, connect to pull-up resistor.
10	SDA	Serial data I/O; open-drain, connect to pull-up resistor.
11	A0	A0 address pin for Two-Wire address; connect to either logic 1 or logic 0. See Table 1.
12	BKSEL	Selects memory bank 0 or 1; connect to either logic 1 to select bank 1 or logic 0 to select bank 0.
13	GND_D	Digital ground; must be connected to analog ground at the BUF08832.
14	GND_A	Analog ground; must be connected to digital ground (GND_D).
15	OUT5	DAC output 5
16	OUT6	DAC output 6
17	OUT7	DAC output 7
18	OUT8	DAC output 8
19	V_S	V_S connected to analog supply
20	V_{COM-FB}	V_{COM} feedback

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +18V, V_{SD} = +2V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

OUTPUT VOLTAGE vs OUTPUT CURRENT (V_{COM})

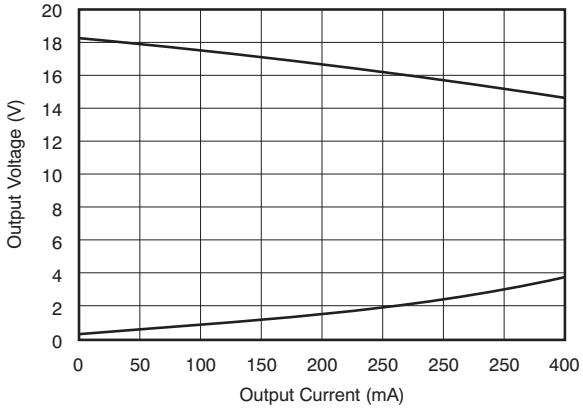


Figure 1.

OUTPUT VOLTAGE vs OUTPUT CURRENT (Channels 1–8)

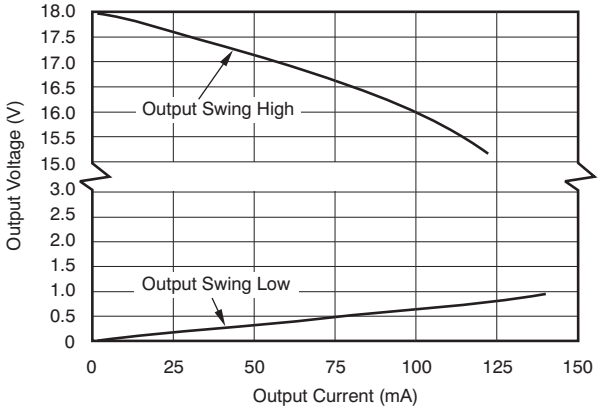


Figure 2.

V_{COM} OUTPUT VOLTAGE vs CODE

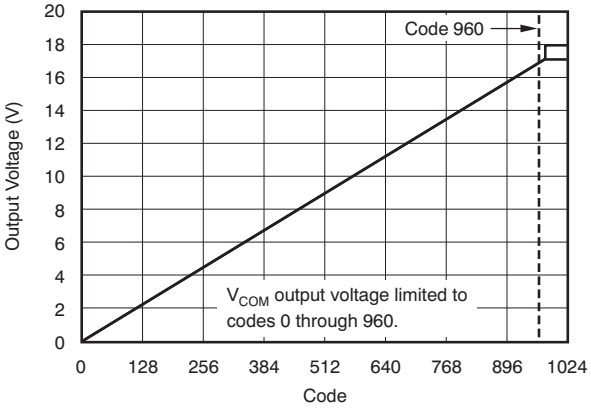


Figure 3.

ANALOG SUPPLY CURRENT HISTOGRAM

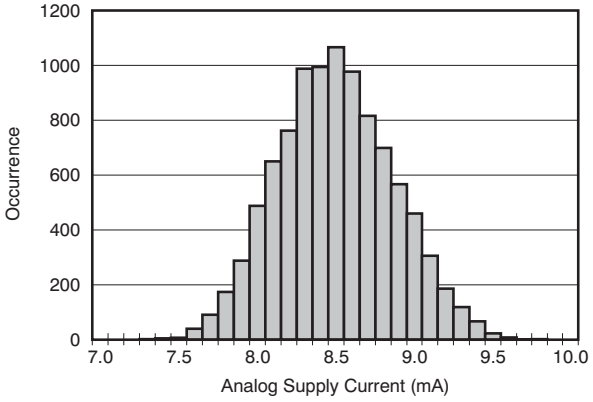


Figure 4.

ANALOG SUPPLY CURRENT vs TEMPERATURE

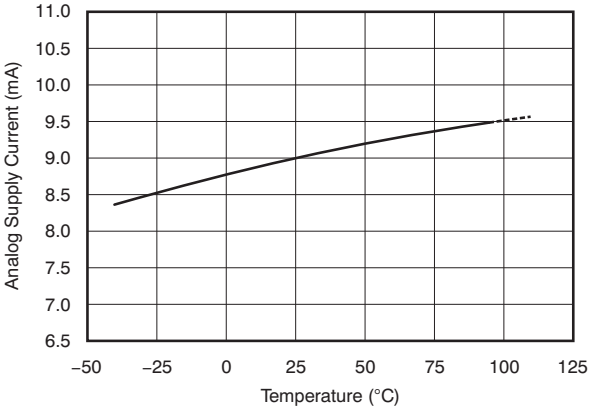


Figure 5.

OUTPUT VOLTAGE vs TEMPERATURE

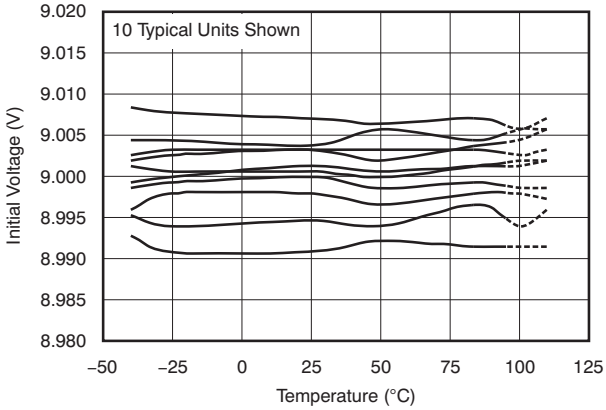


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +18V, V_{SD} = +2V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

DIGITAL SUPPLY CURRENT vs TEMPERATURE

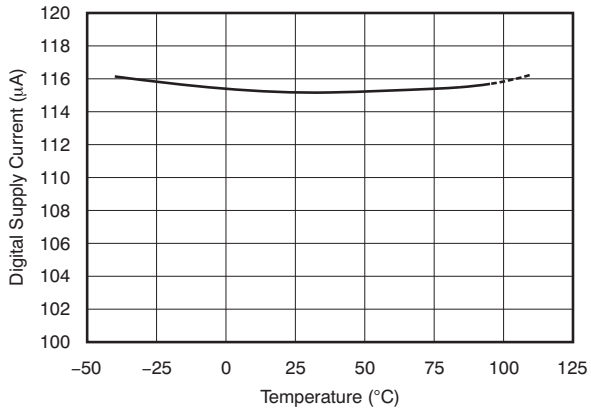


Figure 7.

DIFFERENTIAL LINEARITY ERROR

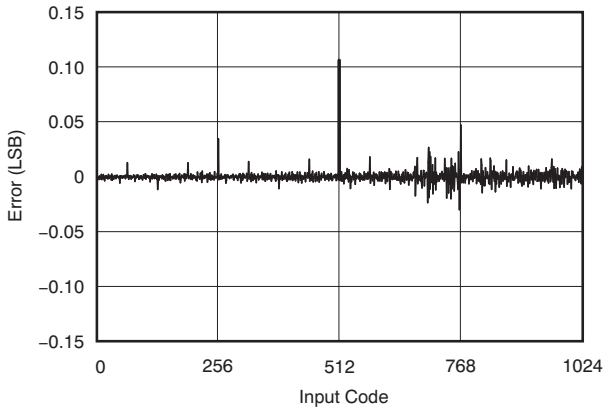


Figure 8.

INTEGRAL LINEARITY ERROR

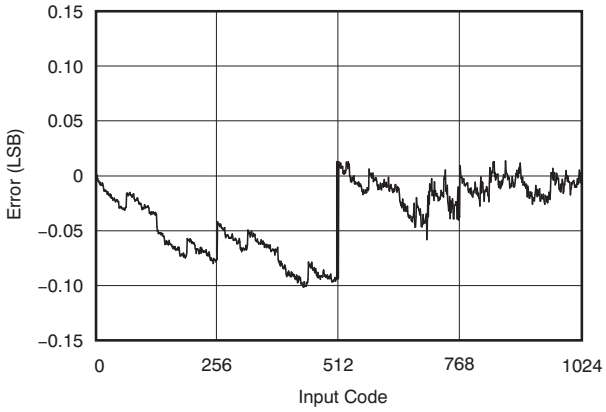


Figure 9.

BKSEL SWITCHING TIME DELAY

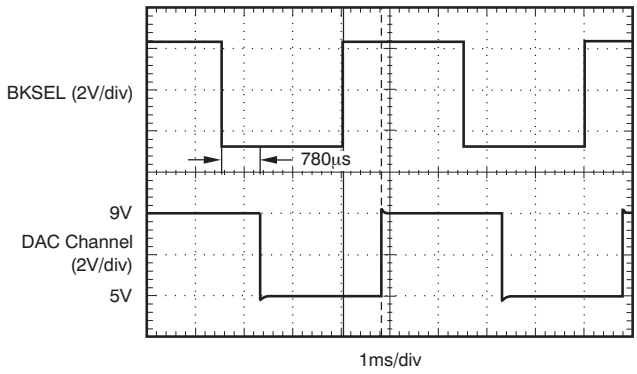


Figure 10.

LARGE-SIGNAL STEP RESPONSE

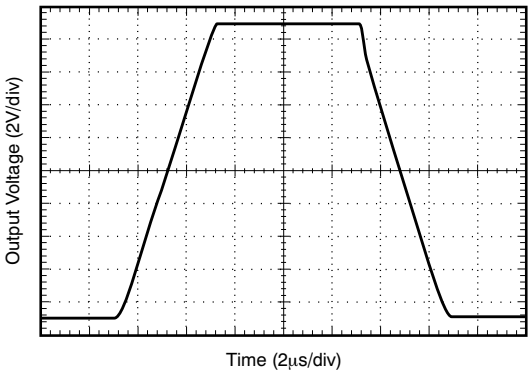


Figure 11.

LARGE-SIGNAL STEP RESPONSE, V_{COM}

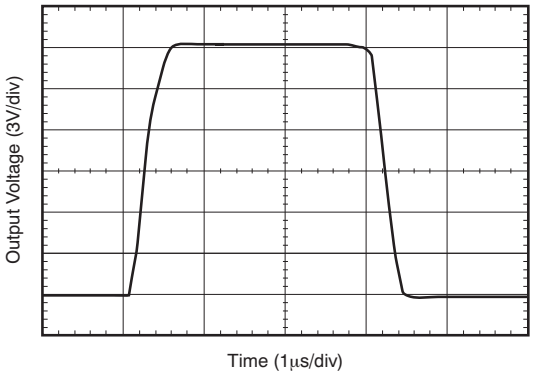


Figure 12.

APPLICATION INFORMATION

GENERAL

The BUF08832 programmable voltage reference allows fast and easy adjustment of eight programmable gamma reference outputs and a V_{COM} output, each with 10-bit resolution. The BUF08832 is programmed through a high-speed, Two-Wire interface. The final gamma and V_{COM} values can be stored in the onboard, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF08832 supports up to 16 write operations to the onboard memory. The BUF08832 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate dynamic switching between gamma curves.

The BUF08832 can be powered using an analog supply voltage from 9V to 20V, and a digital supply from 2V to 5.5V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time. See Figure 13 and Figure 14 for typical configurations of the BUF08832.

TWO-WIRE BUS OVERVIEW

The BUF08832 communicates over an industry-standard, two-wire interface to receive data in slave mode. This model uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The BUF08832 can act only as a slave device; therefore, it never drives SCL. SCL is an input only for the BUF08832.

ADDRESSING THE BUF08832

The address of the BUF08832 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is LOW, the device acknowledges on address 74h (1110100). If the A0 pin is HIGH, the device acknowledges on address 75h (1110101). Table 1 shows the A0 pin settings and BUF08832 address options.

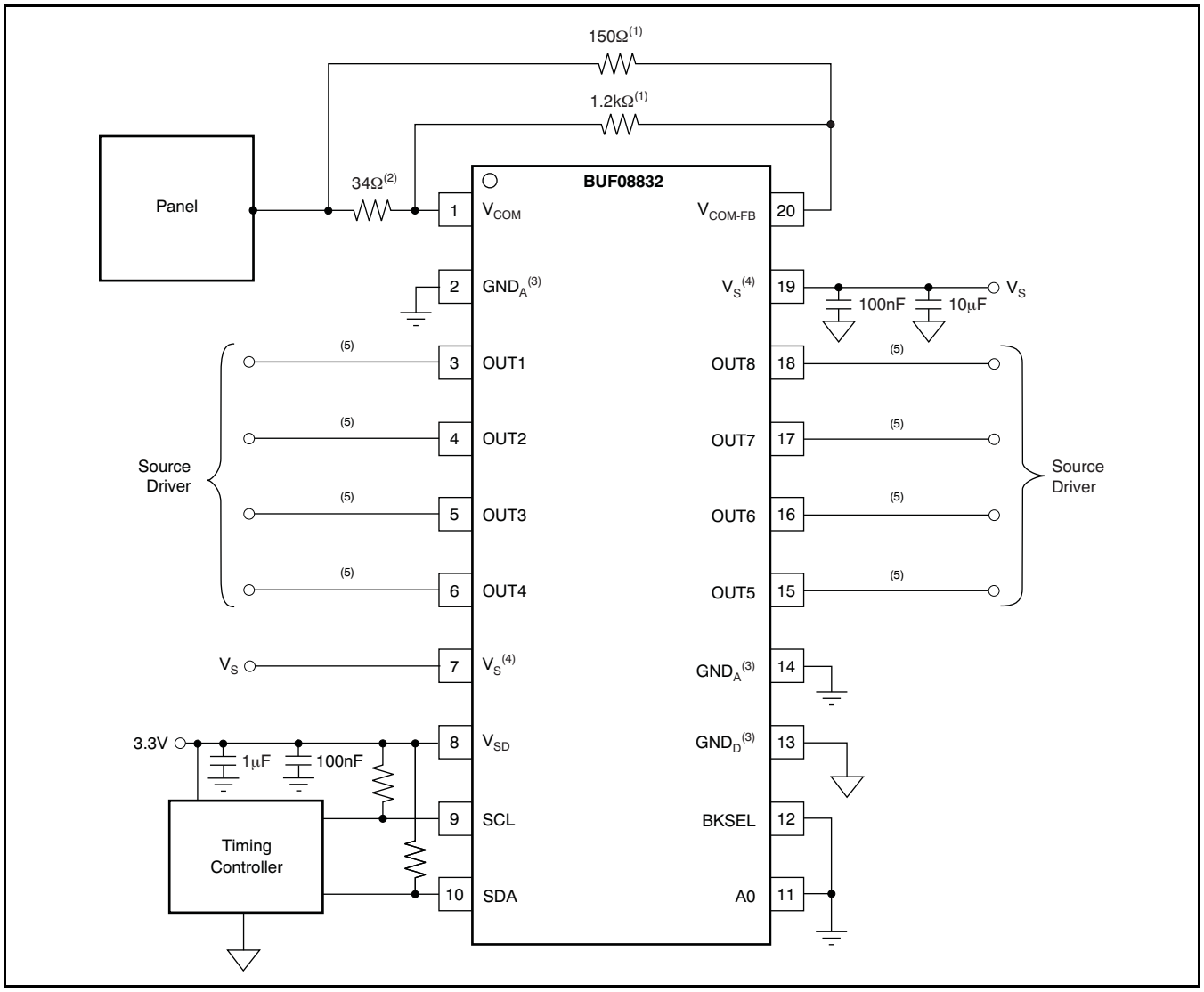
Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick Reference of BUF08832 Addresses

DEVICE/COMPONENT BUF08832 ADDRESS	ADDRESS
A0 pin is LOW (device acknowledges on address 74h)	1110100
A0 pin is HIGH (device acknowledges on address 75h)	1110101

Table 2. Quick Reference of Command Codes

COMMAND	CODE
General-Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.



(1) Values must be selected for the panel used.

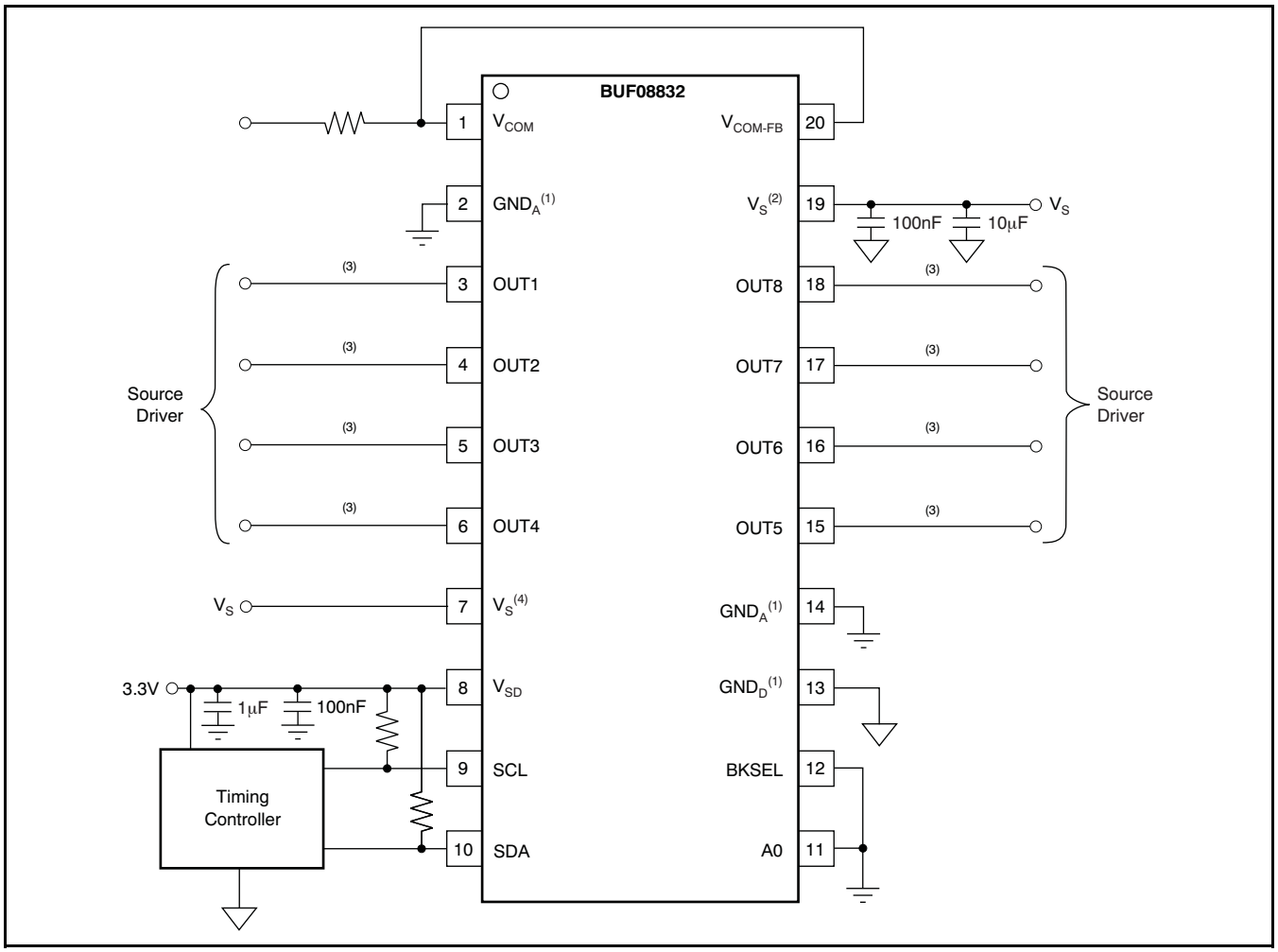
(2) Values must be selected for good phase margin when driving large capacitive loads.

(3) GND_A and GND_D must be connected together.

(4) Pins 7 and 19 are V_S. The one set of capacitors shown on pin 19 are common to both pins.

(5) RC combination for the OUT pins is not recommended; see the *Output Protection* section.

Figure 13. Typical Application Configuration (V_{COM} with Feedback)



(1) GND_A and GND_D must be connected together.

(2) Pins 7 and 19 are V_S. The one set of capacitors shown on pin 19 are common to both pins.

(3) RC combination for the OUT pins is not recommended; see the *Output Protection* section.

Figure 14. Typical Application Configuration (V_{COM} without Feedback)

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF08832 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001 xxx, with SCL ≤ 400kHz, following the START condition; where *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. Table 2 provides a reference for the High-speed mode command code. (Note that this configuration is different from normal address bytes—the low bit does not indicate read/write status.) The BUF08832 responds to the High-speed command regardless of the value of these last three bits. The BUF08832 does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. Upon receiving a master code, the BUF08832 switches on its Hs mode filters, and communicates at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF08832 switches out of Hs mode with the next STOP condition.

GENERAL-CALL RESET AND POWER-UP

The BUF08832 responds to a General-Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (*0000 0110*). The BUF08832 acknowledges both bytes. Table 2 provides a reference for the General-Call Reset command code. Upon receiving a General-Call Reset, the BUF08832 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General-Call address byte of 00h (*0000 0000*), but does not acknowledge any General-Call data bytes other than 06h (*0000 0110*).

When the BUF08832 powers up, it automatically performs a reset. As part of the reset, the BUF08832 is configured for all outputs to change to the last programmed nonvolatile memory values, or *1000000000* if the nonvolatile memory values have not been programmed.

OUTPUT VOLTAGE

Buffer output values are determined by the analog supply voltage (V_S) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = V_S \times \left(\frac{CODE_{10}}{1024} \right) \quad (1)$$

The BUF08832 outputs are capable of a full-scale voltage output change in typically 5µs; no intermediate steps are required.

UPDATING THE DAC OUTPUT VOLTAGES

Because the BUF08832 features a double-buffered register structure, updating the digital-to-analog converter (DAC) and/or the V_{COM} **register** is not the same as updating the DAC and/or V_{COM} **output voltage**. There are two methods for updating the DAC/V_{COM} output voltages.

Method 1: Method 1 is used when it is desirable to have the DAC/V_{COM} output voltage change immediately after writing to a DAC register. For each write transaction, the master sets data bit 15 to a '1'. The DAC/V_{COM} output voltage update occurs after receiving the 16th data bit for the currently-written register.

Method 2: Method 2 is used when it is desirable to have all DAC/V_{COM} output voltages change at the same time. First, the master writes to the desired DAC/V_{COM} channels with data bit 15 a '0'. Then, when writing the last desired DAC/V_{COM} channel, the master sets data bit 15 to a '1'. All DAC/V_{COM} channels are updated at the same time after receiving the 16th data bit.

NONVOLATILE MEMORY

BKSEL Pin

The BUF08832 has 16x rewrite capability of the nonvolatile memory. Additionally, the BUF08832 has the ability to store two distinct gamma curves in two different nonvolatile memory banks, each of which has 16x rewrite capability. One of the two available banks is selected using the external input pin, BKSEL. When this pin is low, BANK0 is selected; when this pin is high, BANK1 is selected.

When the BKSEL pin changes state, the BUF08832 acquires the last programmed DAC/V_{COM} values from the nonvolatile memory associated with this newly chosen bank. At power-up, the state of the BKSEL pin determines which memory bank is selected.

The I^2C master also has the ability to update (acquire) the DAC registers with the last programmed nonvolatile memory values using software control. The bank to be acquired depends on the state of BKSEL.

General Acquire Command

A general acquire command is used to update all registers and DAC/V_{COM} outputs to the last programmed values stored in nonvolatile memory. A single-channel acquire command updates only the register and DAC/V_{COM} output of the DAC/V_{COM} corresponding to the DAC/V_{COM} address used in the single-channel acquire command.

These are the steps of the sequence to initiate a general channel acquire:

1. Be sure BKSEL is in its desired state and has been stable for at least 1ms.
2. Send a START condition on the bus.
3. Send the appropriate device address (based on A0) and the read/write bit = LOW. The BUF08832 acknowledges this byte.
4. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 1 and D6 = 0. Bits D5-D0 are any valid DAC/V_{COM} address. Although the BUF08832 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
   – 000000 through 000111
   – 010010
   It returns *0000* for reads from 001000 through 010001, and 010011 through 010111. See Table 4 for valid DAC/V_{COM} addresses.
5. Send a STOP condition on the bus.

Approximately 750µs (±80µs) after issuing this command, all DAC/V_{COM} registers and DAC/V_{COM} output voltages change to the respective, appropriate nonvolatile memory values.

Single-Channel Acquire Command

These are the steps to initiate a single-channel acquire:

1. Be sure BKSEL is in its desired state and has been stable for at least 1ms.
2. Send a START condition on the bus.
3. Send the device address (based on A0) and read/write bit = LOW. The BUF08832 acknowledges this byte.
4. Send a DAC/V_{COM} pointer address byte using the DAC/V_{COM} address corresponding to the output and register to update with the OTP memory value. Set bit D7 = 0 and D6 = 1. Bits D5-D0 are the DAC/V_{COM} address. Although the BUF08832 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
   – 000000 through 000111
   – 010010
   It returns *0000* reads from 001000 through 010001, and 010011 through 010111. See Table 4 for valid DAC/V_{COM} addresses.
5. Send a STOP condition on the bus.

Approximately 36µs (±4µs) after issuing this command, the specified DAC/V_{COM} register and DAC/V_{COM} output voltage change to the appropriate memory value.

MaxBank

The BUF08832 can provide the user with the number of times the nonvolatile memory of a particular DAC/V_{COM} channel nonvolatile memory has been written to for the current memory bank. This information is provided by reading the register at pointer address 111111.

There are two ways to update the MaxBank register:

1. After initiating a single acquire command, the BUF08832 updates the MaxBank register with a code corresponding to how many times that particular channel memory has been written to.
2. Following a general acquire command, the BUF08832 updates the MaxBank register with a code corresponding to the maximum number of times the most used channel (OUT1-8 and V_{COM}s) has been written to.

MaxBank is a read-only register and is only updated by performing a general- or single-channel acquire.

Table 3 shows the relationship between the number of times the nonvolatile memory has been programmed and the corresponding state of the MaxBank Register.

Table 3. MaxBank Details

NUMBER OF TIMES WRITTEN TO	RETURNS CODE
0	0000
1	0000
2	0001
3	0010
4	0011
5	0100
6	0101
7	0110
8	0111
9	1000
10	1001
11	1010
12	1011
13	1100
14	1101
15	1110
16	1111

Parity Error Correction

The BUF08832 provides single-bit parity error correction for data stored in the nonvolatile memory to provide increased reliability of the nonvolatile memory. If a single bit of nonvolatile memory for a channel fails, the BUF08832 corrects for it and updates the appropriate DAC with the intended value when its memory is acquired.

If more than one bit of nonvolatile memory for a channel fails, the BUF08832 does not correct for it, and updates the appropriate DAC/V_{COM} with the default value of 1000000000.

DIE_ID AND DIE_REV REGISTERS

The user can verify the presence of the BUF08832 in the system by reading from address 111101. The BUF08832 returns *0010001010000000* when read at this address.

The user can also determine the die revision of the BUF08832 by reading from register 111100. BUF08832 returns *0000000000000000* when a RevA die is present. RevB would be designated by *0000000000000001* and so on.

READ/WRITE OPERATIONS

Read and write operations can be done for a single DAC/V_{COM} or for multiple DACs/V_{COM}. Writing to a DAC/V_{COM} register differs from writing to the nonvolatile memory. Bits D15–D14 of the most significant byte of data determines if data are written to the DAC/V_{COM} register or the nonvolatile memory.

Read/Write: DAC/V_{COM} Register (volatile memory)

The BUF08832 is able to read from a single DAC/V_{COM}, or multiple DACs/V_{COM}, or write to the register of a single DAC/V_{COM}, or multiple DACs/V_{COM} in a single communication transaction. DAC pointer addresses begin with 000000 (which corresponds to OUT1) through 000111 (which corresponds to OUT8). The V_{COM} address is 010010.

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH performs a read transaction.

Writing: DAC/V_{COM} Register (Volatile Memory)

To write to a single DAC/V_{COM} register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08832 acknowledges this byte.
3. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/V_{COM} address. Although the BUF08832 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
   - 000000 through 000111
   - 010010

   It returns *0000* for reads from 001000 through 010001, and 010011 through 010111. See Table 4 for valid DAC/V_{COM} addresses.
4. Send two bytes of data for the specified register. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are used, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP or START condition on the bus.

The BUF08832 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register is not updated. Updating the DAC/V_{COM} register is not the same as updating the DAC/V_{COM} output voltage; see the *Updating the DAC Output Voltages* section.

The process of updating multiple DAC/V_{COM} registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF08832 automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers have been updated or a STOP or START condition is sent.

To write to multiple DAC/V_{COM} registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08832 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever DAC/V_{COM} is the first in the sequence of DACs/V_{COM} to be updated. The BUF08832 begins with this DAC/V_{COM} and steps through subsequent DACs/V_{COM} in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15–D8, of which only bits D9 and D8 have meaning, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The first two bytes are for the DAC/V_{COM} addressed in the previous step. The DAC/V_{COM} register is automatically updated after receiving the second byte. The next two bytes are for the following DAC/V_{COM}. That DAC/V_{COM} register is updated after receiving the fourth byte. This process continues until the registers of all following DACs/V_{COM} have been updated. The BUF08832 continues to accept data for a total of 18 DACs; however, the two data sets following the 16th data set are meaningless. The 19th data set applies to V_{COM}. The 20th data set is meaningless. The write disable bit cannot be accessed using this method. It must be written to using *the write to a single DAC register* procedure.
5. Send a STOP or START condition on the bus.

The BUF08832 acknowledges each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data are updated.

Reading: DAC/V_{COM}/OTHER Register (Volatile Memory)

Reading a register returns the data stored in that DAC/V_{COM}/OTHER register.

To read a single DAC/V_{COM}/OTHER register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08832 acknowledges this byte.
3. Send the DAC/V_{COM}/OTHER pointer address byte. Set bit D7 = 0 and D6 = 0; bits D5–D0 are the DAC/V_{COM}/OTHER address. NOTE: The BUF08832 stores and returns data only from these addresses:
   - 000000 through 000111
   - 010010
   - 111100 through 111111

   It returns *0000* for reads from 001000 through 010001, and 010011 through 010111. See Table 4 for valid DAC/V_{COM}/OTHER addresses.
4. Send a START or STOP/START condition.
5. Send the correct device address and read/write bit = HIGH. The BUF08832 acknowledges this byte.
6. Receive two bytes of data. They are for the specified register. The most significant byte (bits D15–D8) is received first; next is the least significant byte (bits D7–D0). In the case of DAC/V_{COM} channels, bits D15–D10 have no meaning.
7. Acknowledge after receiving the first byte.
8. Send a STOP or START condition on the bus or do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not acknowledging.

To read multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08832 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever register is the first in the sequence of DACs/V_{COM} to be read. The BUF08832 begins with this DAC/V_{COM} and steps through subsequent DACs/V_{COM} in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send the correct device address and read/write bit = HIGH. The BUF08832 acknowledges this byte.
6. Receive two bytes of data. They are for the specified DAC/V_{COM}. The first received byte is the most significant byte (bits D15–D8; only bits D9 and D8 have meaning), next is the least significant byte (bits D7–D0).
7. Acknowledge after receiving each byte of data.
8. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge bit. The reading of registers DieID, DieRev, and MaxBank is not supported in this mode of operation (these values must be read using the single register read method).

Write: Nonvolatile Memory for the DAC Register

The BUF08832 is able to write to the nonvolatile memory of a single DAC/V_{COM} in a single communication transaction. In contrast to the BUF20820, writing to multiple nonvolatile memory words in a single transaction is not supported. Valid DAC/V_{COM} pointer addresses begin with 000000 (which corresponds to OUT1) through 000111 (which corresponds to OUT8). The V_{COM} address is 010010.

When programming the nonvolatile memory, the analog supply voltage must be between 9V and 20V. Write commands are performed by setting the read/write bit LOW.

To write to a single nonvolatile register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08832 acknowledges this byte. Although the BUF08832 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
   – 000000 through 000111
   – 010010

   It returns *0000* for reads from 001000 through 010001, and 010011 through 010111. See Table 4 for DAC/V_{COM} addresses.
3. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/V_{COM} address.
4. Send two bytes of data for the nonvolatile register of the specified DAC/V_{COM}. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are data bits, and bits D15–D14 must be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF08832 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified nonvolatile register is not updated. Writing a nonvolatile register also updates the DAC/V_{COM} register and output voltage.

The DAC/V_{COM} register and DAC/V_{COM} output voltage are updated immediately, while the programming of the nonvolatile memory takes up to 250µs. Once a nonvolatile register write command has been issued, no communication with the BUF08832 should take place for at least 250µs. Writing or reading over the serial interface while the nonvolatile memory is being written jeopardizes the integrity of the data being stored.

Read: Nonvolatile Memory for the DAC Register

To read the data present in nonvolatile register for a particular DAC/V_{COM} channel, the master must first issue a general acquire command, or a single acquire command with the appropriate DAC/V_{COM} channel chosen. This action updates both the DAC/V_{COM} register(s) and DAC/V_{COM} output voltage(s). The master may then read from the appropriate DAC/V_{COM} register as described earlier.

Programmable V_{COM} Limits

The BUF08832 V_{COM} output has a programmable HIGH limit and LOW limit. The implementation and interface of these limits are the same as with the DAC registers. These registers are written to and read back through the Two-Wire bus. Addresses for limiters are 1E and 1F for the HIGH limit and LOW limit, respectively. See Table 4 for register pointer addresses.

Upon power-up or general-call reset, the DAC registers (channels 1 though 8 and V_{COM}) are set to 200 (default) that corresponds to mid-scale output for a 10-bit DAC. The HIGH and LOW limit registers are set to 3FF and 000 respectively. Therefore, the limits are transparent if not programmed.

The BUF08832 uses double-buffered registers. The input of data is stored in the first layer. The input may be latched to the DAC output, depending upon application. The DACs update only when the second layer of latches are enabled.

The HIGH and LOW limits can be programmed to any desired value to limit the V_{COM} output. The limit can be programmed before or after programming the V_{COM} channel. Because the input of data is stored in the first layer of latches, the V_{COM} output is limited according to the following rule in either sequence:

1. If the V_{COM} OTP write is enabled, then the V_{COM} input is always stored in the OTP. Limit comparison happens only before the DAC output.
2. If the V_{COM} input is higher than the HIGH limit, then the HIGH limit is latched to the DAC output. Reading of the DAC register returns the HIGH limit.
3. If the V_{COM} input is lower than the LOW limit, then the LOW limit is latched to the DAC output. Reading of the DAC register returns the LOW limit.
4. If the V_{COM} input is in between the HIGH and LOW limit, then the programmed value is latched to DAC output. Reading of the DAC register returns the programmed value.
5. If the HIGH limit is lower than the LOW limit, then the BUF08832 ignores the limits and latches the programmed value to the DAC output. Reading of the DAC register returns the programmed value.

There are two banks of OTP associated with each of the two limit registers. OTP operations on these two addresses are valid, just like OTP for DAC registers.

Table 4. DAC Register Pointer Addresses

DAC REGISTER	POINTER ADDRESS
OUT1	000000
OUT2	000001
OUT3	000010
OUT4	000011
OUT5	000100
OUT6	000101
OUT7	000110
OUT8	000111
V_{COM}	010010
HIGH Limit	011110
LOW Limit	011111
OTHER REGISTER	**POINTER ADDRESS**
Die_Rev	111100
Die_ID	111101
MaxBank	111111

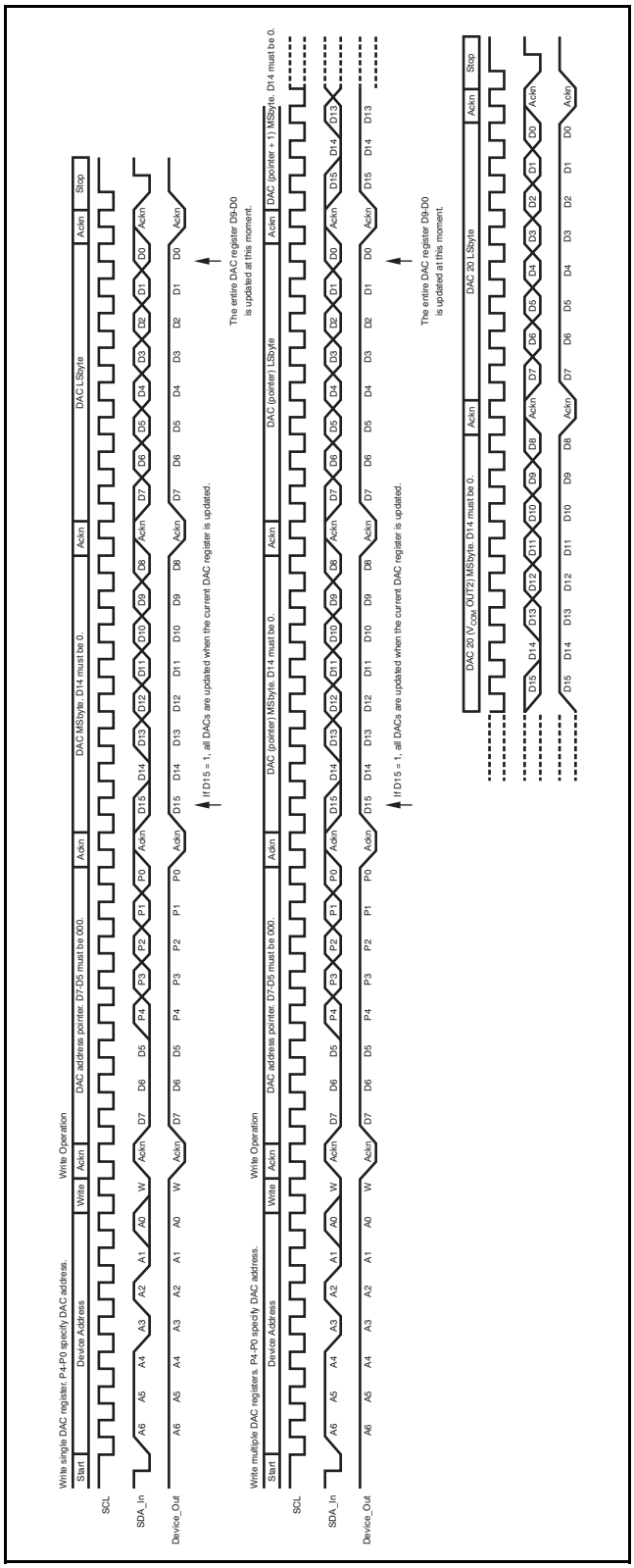


Figure 15. Write DAC Register Timing

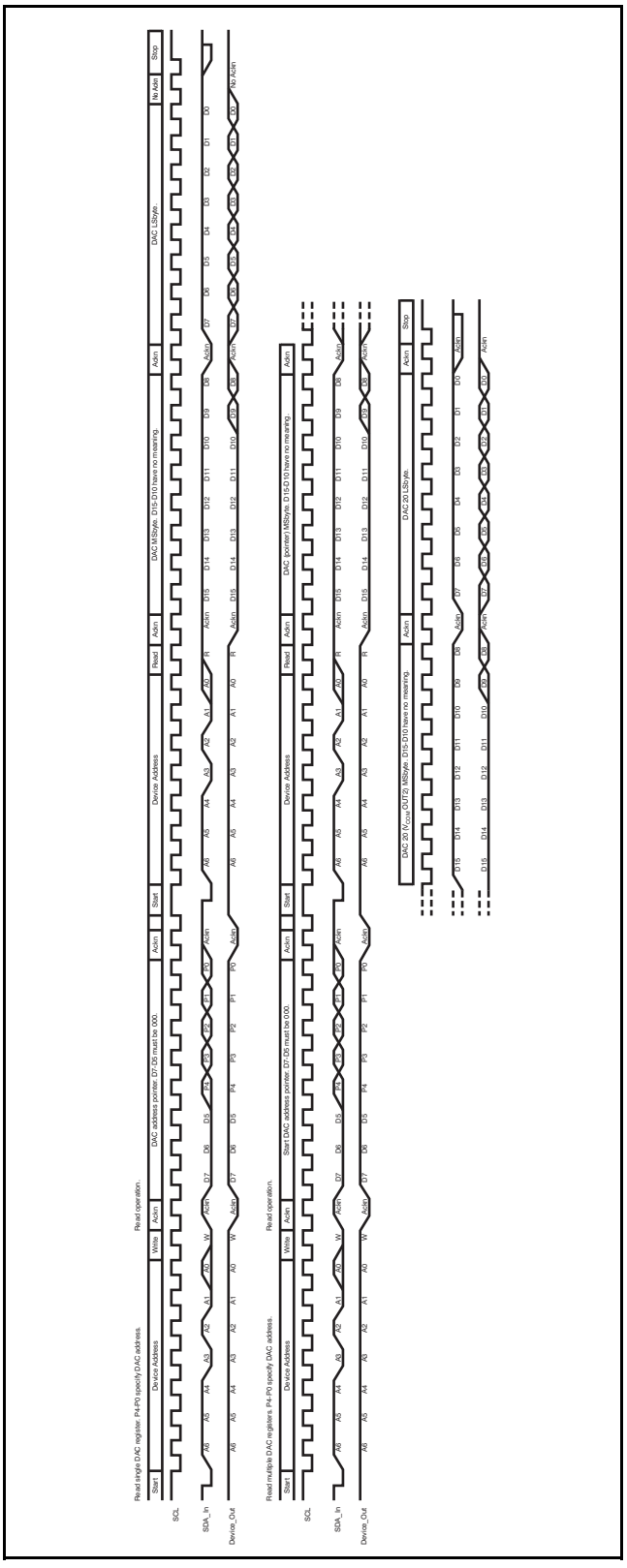


Figure 16. Read Register Timing

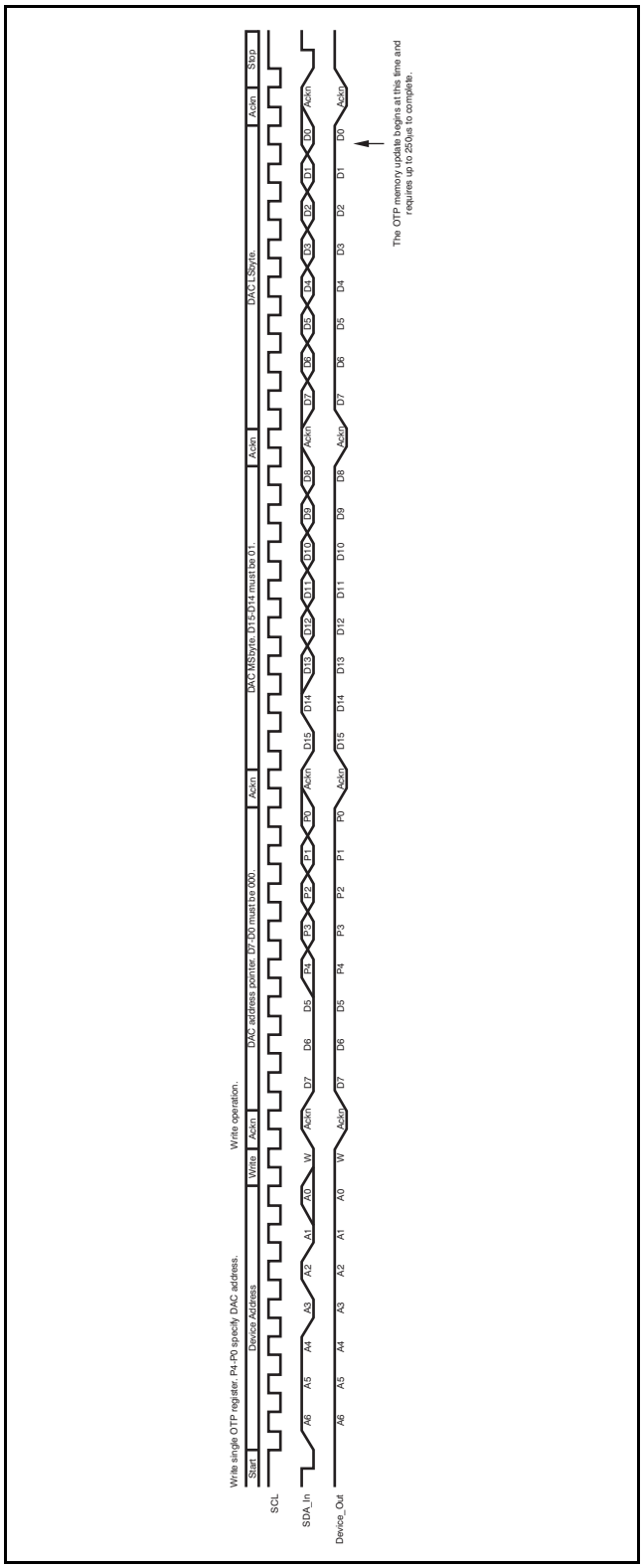


Figure 17. Write Nonvolatile Register Timing

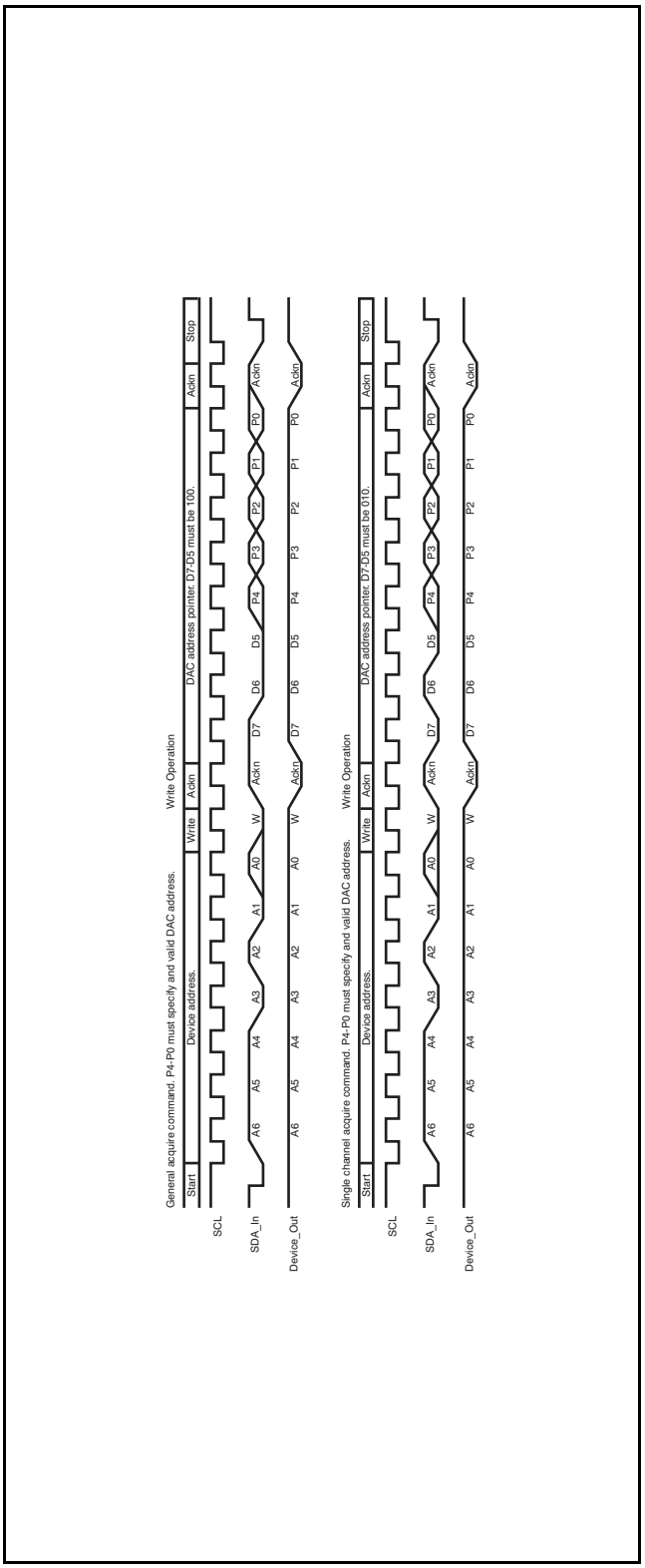


Figure 18. Acquire Operation Timing

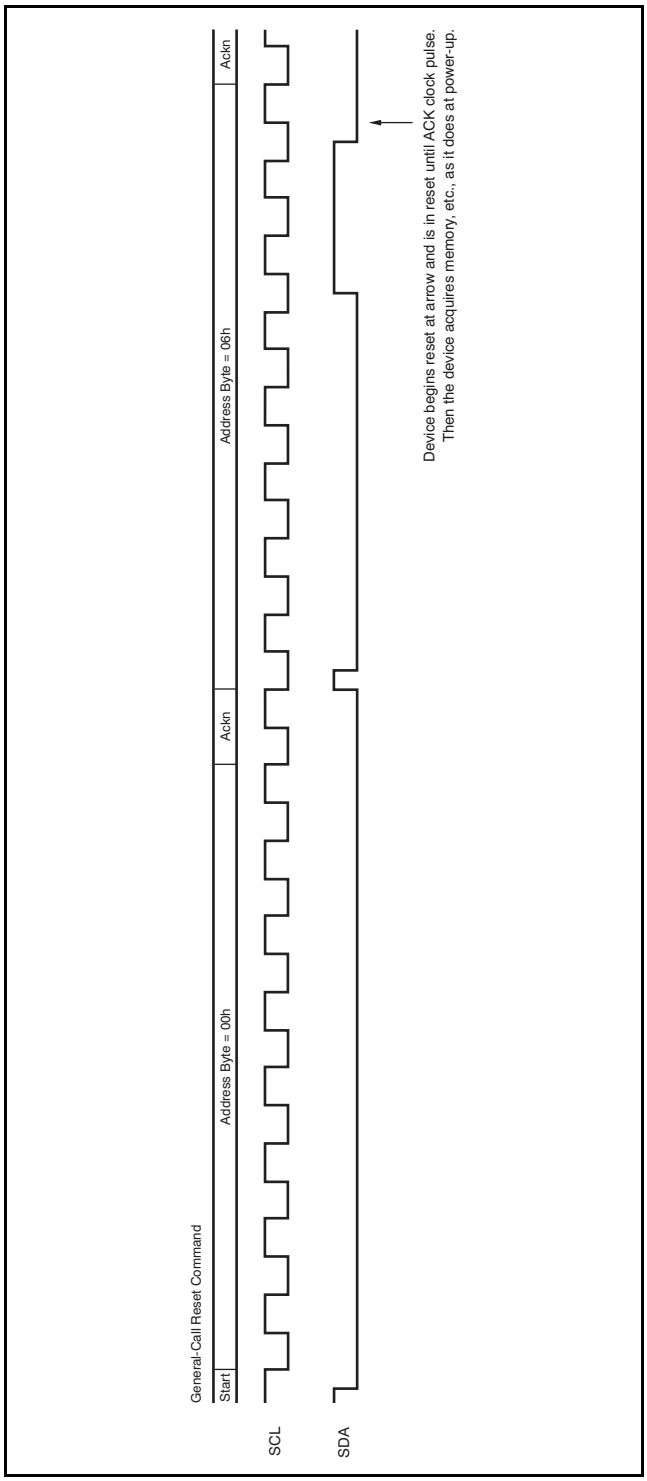


Figure 19. General-Call Reset Timing

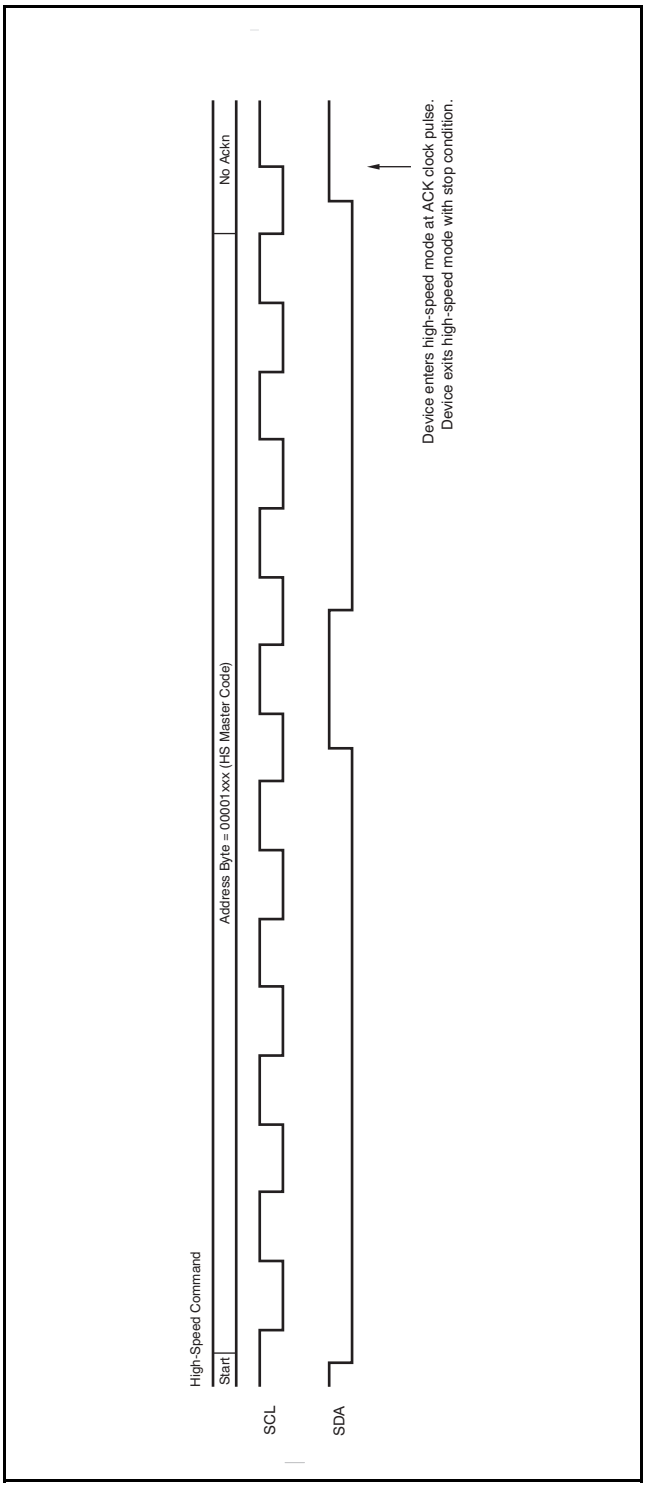


Figure 20. High-Speed Mode Timing

END-USER SELECTED GAMMA CONTROL

Because the BUF08832 has two banks of nonvolatile memory, it is well-suited for providing two levels of gamma control by using the BKSEL pin, as shown in Figure 21. When the state of the BKSEL pin changes, the BUF08832 updates all nine programmable buffer outputs simultaneously after 750µs (±80µs).

To update all nine programmable output voltages simultaneously via hardware, toggle the BKSEL pin to switch between Gamma Curve 0 (stored in Bank0) and Gamma Curve 1 (stored in Bank1).

All DAC/V_{COM} registers and output voltages are updated simultaneously after approximately 750µs.

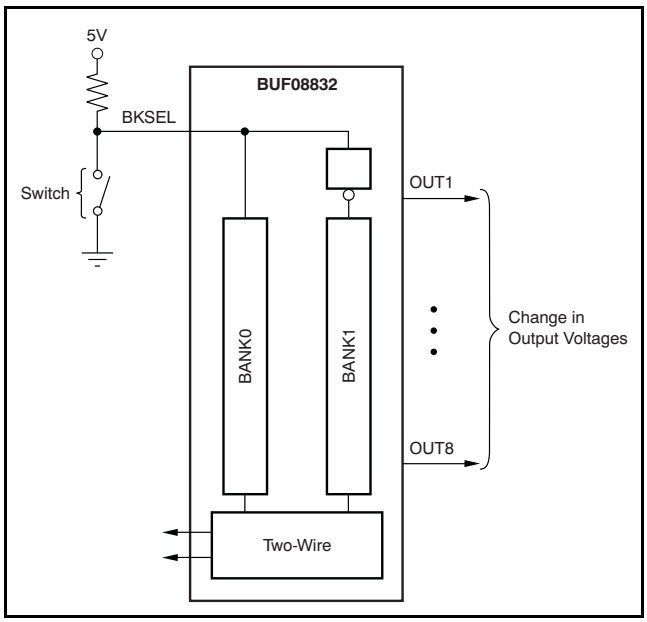


Figure 21. Gamma Control

DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD television applications. This technique typically requires switching gamma curves between frames. Using the BKSEL pin to switch between two gamma curves does not often provide good results because of the 750µs required to transfer the data from the nonvolatile memory to the DAC register. However, dynamic gamma control can still be accomplished by storing two gamma curves in an external EEPROM and writing directly to the DAC register (volatile).

The double register input structure saves programming time by allowing updated DAC values to be pre-stored into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC/V_{COM} output values remain unchanged—the display is unaffected. At the beginning or the end of a picture frame, the DAC/V_{COM} outputs (and therefore, the gamma voltages) can be quickly updated by writing a '1' in bit 15 of any DAC/V_{COM} register. For details on the operation of the double register input structure, see the *Updating the DAC Output Voltages* section.

To update all nine programmable output voltages simultaneously via software, perform the following actions:

STEP 1: Write to registers 1–9 with bit 15 always '0'.

STEP 2: Write any DAC/V_{COM} register a second time with identical data. Make sure that bit 15 is set to '1'. All DAC/V_{COM} channels are updated simultaneously after receiving the last bit of data.

OUTPUT PROTECTION

The BUF08832 output stages can safely source and sink the current levels indicated in Figure 1 and Figure 2. However, there are other modes where precautions must be taken to prevent to the output stages from being damaged by excessive current flow. The outputs (OUT1 through OUT8, and V_{COM}) include ESD protection diodes, as shown in Figure 22. Normally, these diodes do not conduct and are passive during typical device operation. Unusual operating conditions can occur where the diodes may conduct, potentially subjecting them to high, even damaging current levels. These conditions are most likely to occur when a voltage applied to an output exceeds (V_S) + 0.5V, or drops below GND – 0.5V.

One common scenario where this condition can occur is when the output pin is connected to a sufficiently large capacitor, and the BUF08832 power-supply source (V_S) is suddenly removed. Removing the power-supply source allows the capacitor to discharge through the current-steering diodes. The energy released during the high current flow period causes the power dissipation limits of the diode to be exceeded. Protection against the high current flow may be provided by placing current-limiting resistors in series with the output, as shown in Figure 13. Select a resistor value that restricts the current level to the maximum rating for the particular pin.

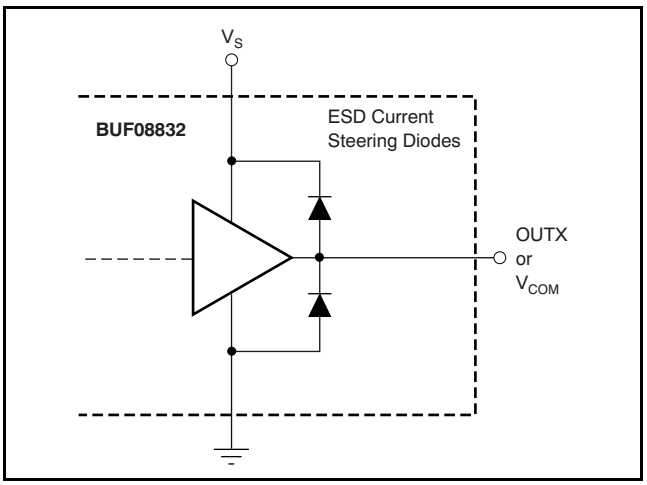


Figure 22. Output Pins ESD Protection Current-Steering Diodes

GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF08832 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted; see Figure 23(a) and Figure 23(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 23(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. This technique provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GND_A and GND_D.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns for the HTSSOP-20 PWP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils (0,33mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. An example thermal land pattern mechanical drawing is attached to the end of this data sheet.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area to help dissipate the heat generated by the BUF08832 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.
5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This configuration makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF08832 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its twelve holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, simply place the BUF08832 IC in position and run the chip through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

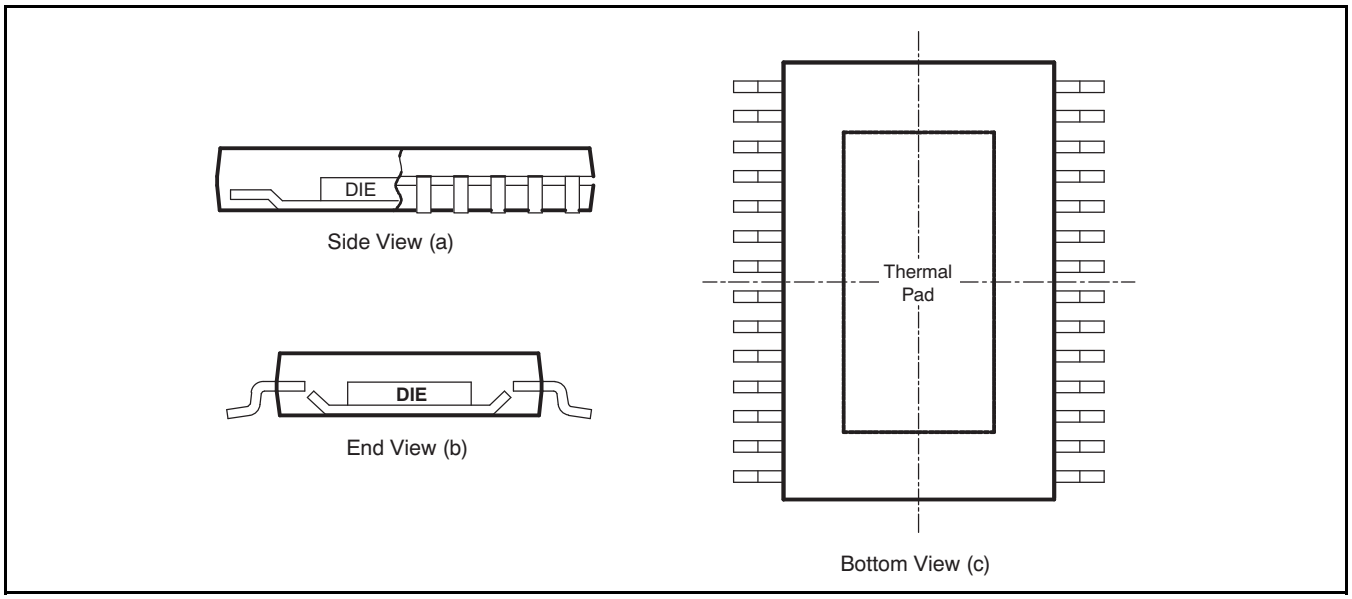


Figure 23. Views of Thermally-Enhanced PWP Package

For a given θ_{JA} (listed in the Electrical Characteristics), the maximum power dissipation is shown in Figure 24 and calculated by Equation 2:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (2)$$

Where:

P_D = maximum power dissipation (W)

T_{MAX} = absolute maximum junction temperature (+125°C)

T_A = free-ambient air temperature (°C)

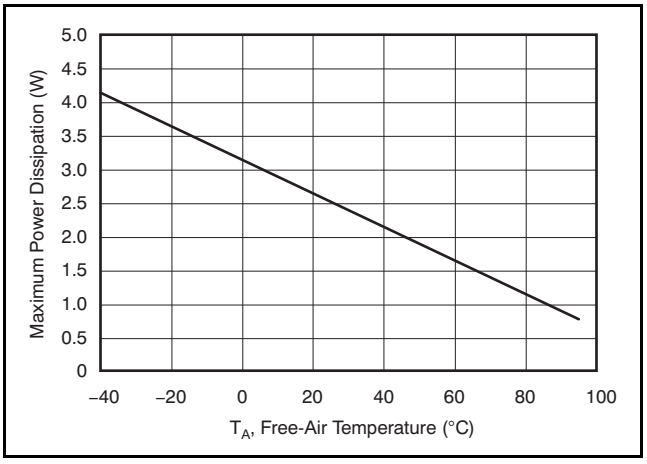


Figure 24. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision September, 2009 (B) to Revision C **Page**

- Corrected error in x-axis value for Figure 11 6

Changes from Revision September 2009 (A) to Revision B **Page**

- Changed the typ and max specifications for the Analog Power Supply, *Total Ananlog Supply Current* and *Over Temperature* parameters of the Electrical Characteristics table 3
- Added Figure 4 5
- Moved Figure 7 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BUF08832AIPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

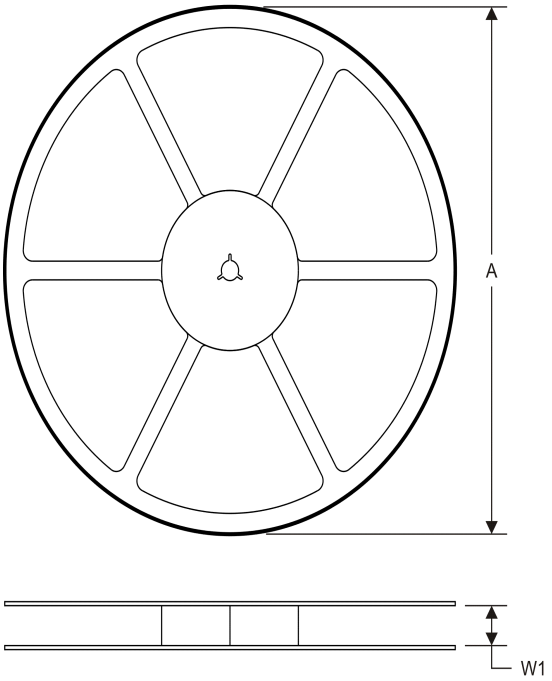
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

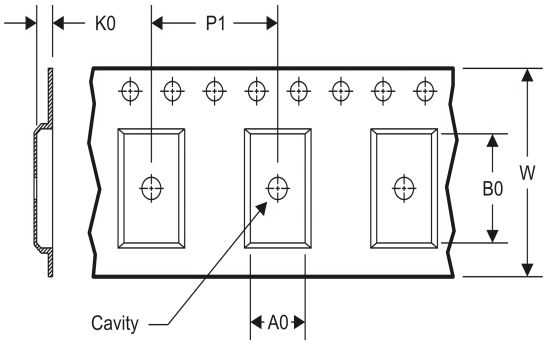
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



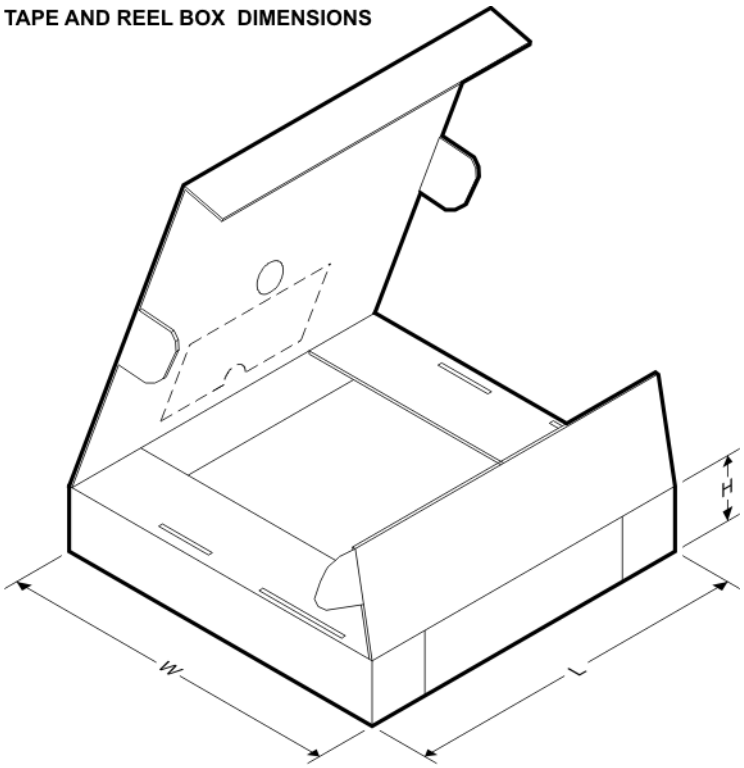
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF08832AIPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

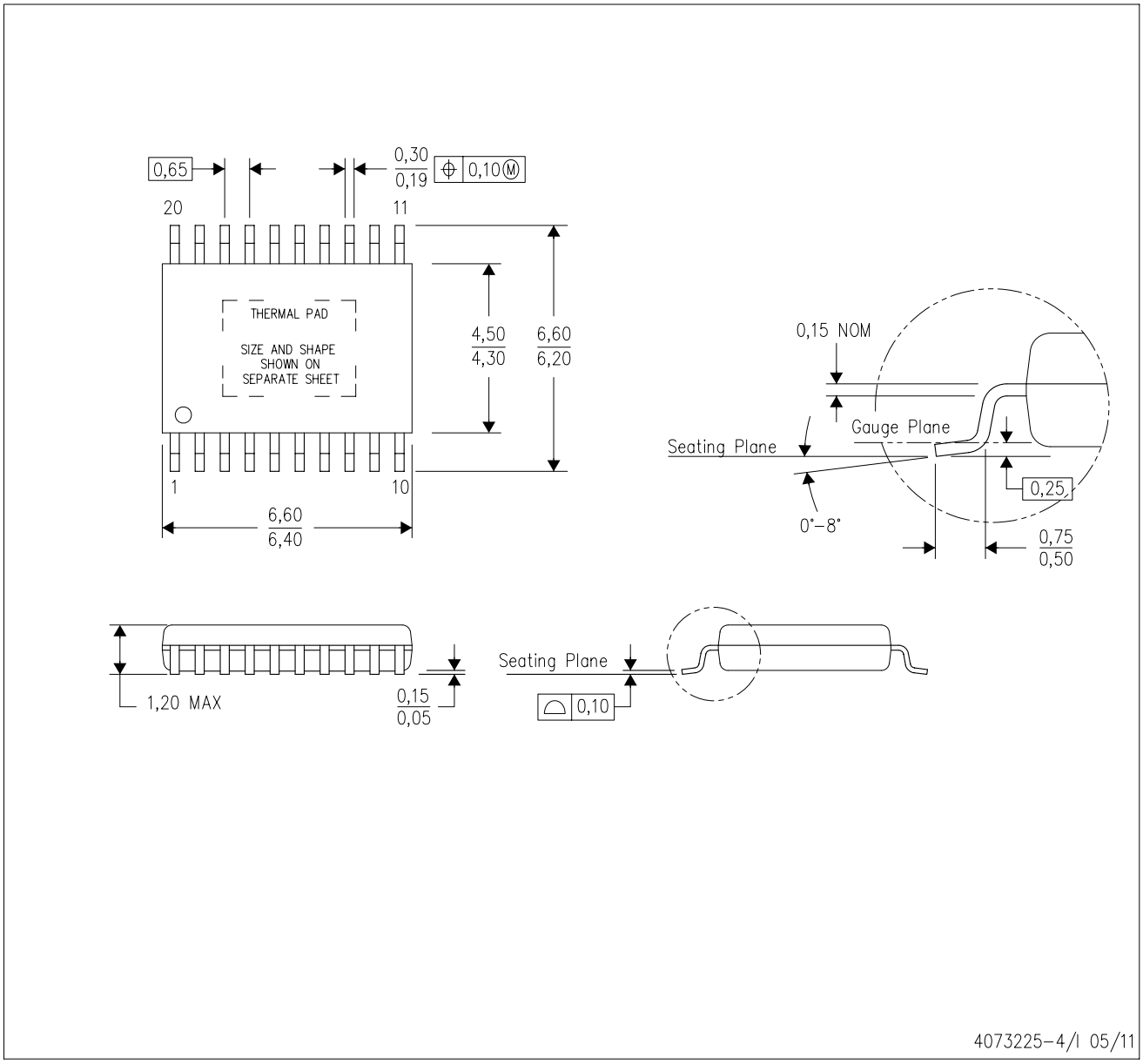
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF08832AIPWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

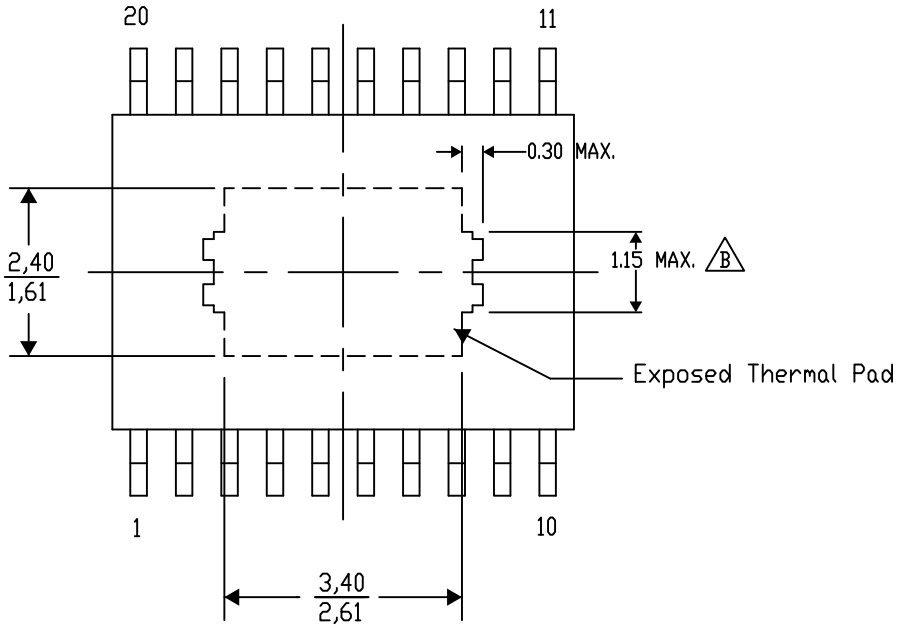
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

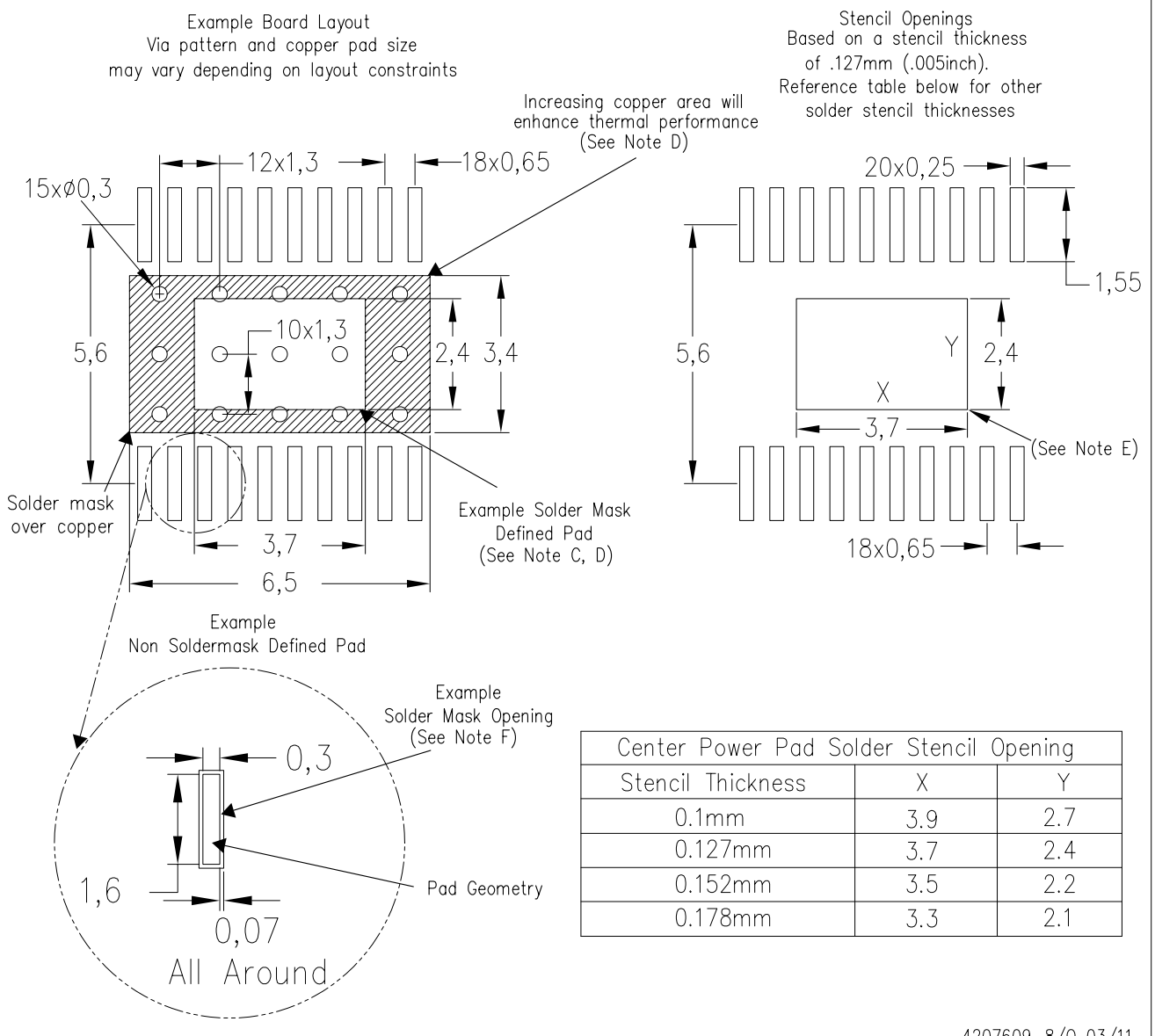
4206332–15/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/Q 03/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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