

## Overvoltage Protection for 2-Series to 4-Series Cell Li-Ion Batteries with External Delay Capacitor

Check for Samples: [bq294700](#), [bq294701](#), [bq294702](#), [bq294703](#), [bq294704](#), [bq294705](#)

### FEATURES

- 2-, 3-, and 4-Series Cell Overvoltage Protection
- External Capacitor-Programmed Delay Timer
- Factory Programmed OVP Threshold (Threshold Range 3.85 V to 4.6 V)
- Output Options: Active High or Open Drain Active Low
- High-Accuracy Overvoltage Protection:  $\pm 10$  mV
- Low Power Consumption  $I_{CC} \approx 1 \mu\text{A}$  ( $V_{CELL(ALL)} < V_{PROTECT}$ )
- Low Leakage Current Per Cell Input  $< 100$  nA
- Small Package Footprint
  - 8-Pin SON (2 mm x 2 mm)

### APPLICATIONS

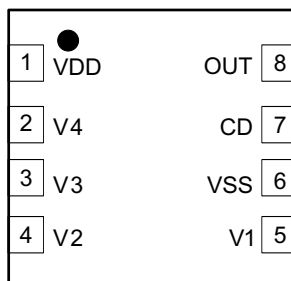
- Notebook
- UPS Battery Backup

### DESCRIPTION

The bq2947xy family of products is an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition.

In the bq2947xy device, an external delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low, depending on the configuration). The external delay timer feature also includes the ability to detect an open or shorted delay capacitor on the CD pin, which will similarly trigger the output driver in an overvoltage condition.

For quicker production-line testing, the bq2947xy device provides a Customer Test Mode with reduced delay time.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION

T <sub>A</sub>	Part Number	Package	Package Designator	OVP (V)	OV Hysteresis (V)	Output Drive	Tape and Reel (Large)
-40°C to 110°C	bq294700	8-pin SON	DSG	4.350	0.300	CMOS Active High	bq294700DSGR
	bq294701			4.250	0.300	CMOS Active High	bq294701DSGR
	bq294702			4.300	0.300	CMOS Active High	bq294702DSGR
	bq294703			4.325	0.300	CMOS Active High	bq294703DSGR
	bq294704			4.400	0.300	CMOS Active High	bq294704DSGR
	bq294705			4.450	0.300	CMOS Active High	bq294705DSGR
	bq2947xy <sup>(1)</sup>			3.850–4.600	0–0.300	CMOS Active High or Open Drain Active Low	bq2947xyTBD

(1) Future option, contact TI.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		bq2947xy	UNITS
		SON	
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	62	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	72	
$\theta_{JB}$	Junction-to-board thermal resistance	32.5	
$\Psi_{JT}$	Junction-to-top characterization parameter	1.6	
$\Psi_{JB}$	Junction-to-board characterization parameter	33	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	10	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

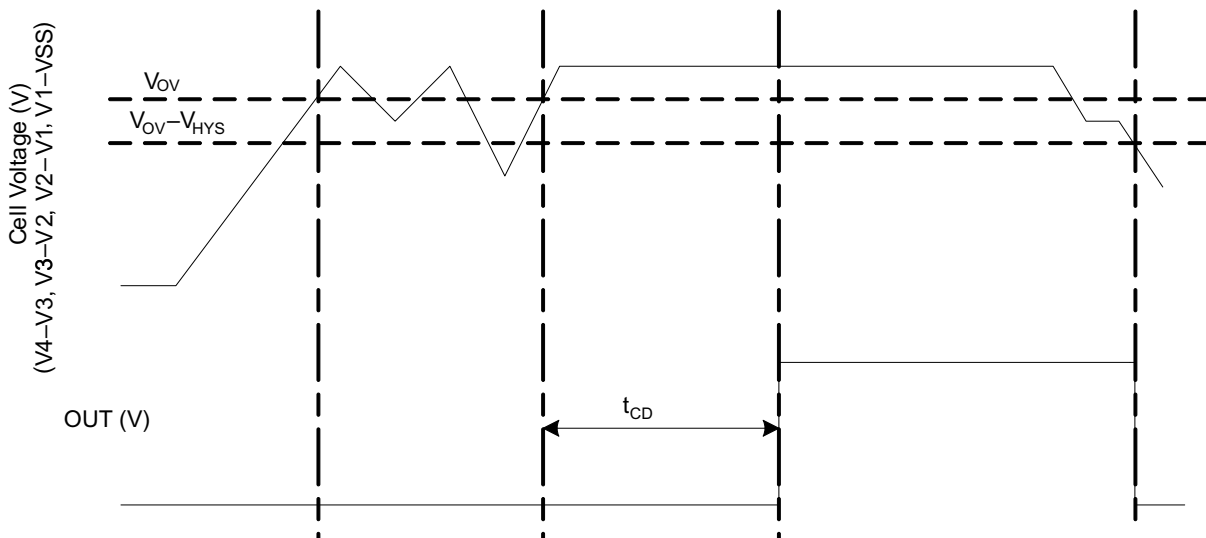
## PIN FUNCTIONS

bq2947xy	Pin Name	Type I/O	Description
1	VDD	P	Power supply input
2	V4	IA	Sense input for positive voltage of the fourth cell from the bottom of the stack
3	V3	IA	Sense input for positive voltage of the third cell from the bottom of the stack
4	V2	IA	Sense input for positive voltage of the second cell from the bottom of the stack
5	V1	IA	Sense input for positive voltage of the lowest cell in the stack
6	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
7	CD	OA	External capacitor connection for delay timer
8	OUT	OA	Analog Output drive for overvoltage fault signal. Active High or Open Drain Active Low
9	PWPD	P	TI recommends connecting the exposed pad to VSS on PCB.

## PIN DETAILS

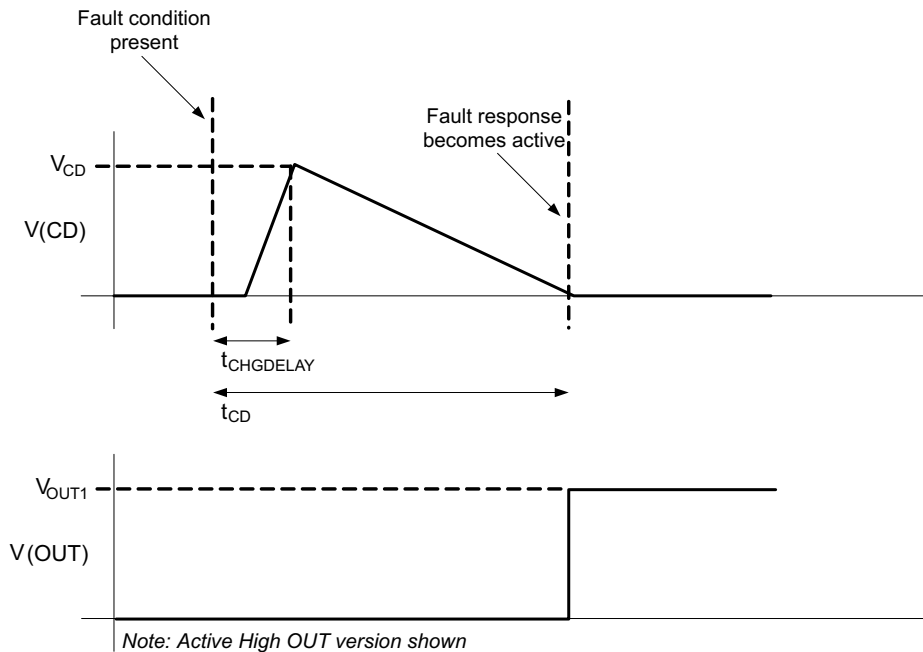
In the bq2947xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference,  $V_{OV}$ . If any cell voltage exceeds the programmed OV value, a timer circuit is activated. This timer circuit charges the CD pin to a nominal value, then slowly discharges it with a fixed current back down to VSS. When the CD pin falls below a nominal threshold near VSS, the OUT terminal goes from inactive to active state. Additionally, a timeout detection circuit checks to ensure that the CD pin successfully begins charging to above VSS and subsequently drops back down to VSS, and if a timeout error is detected in either direction, it will similarly trigger the OUT pin to become active. See Figure 2 for details on CD and OUT pin behavior during an overvoltage event.

For an NCH Open Drain Active Low configuration, the OUT pin pulls down to VSS when active (OV present) and is high impedance when inactive (no OV).



**Figure 1. Timing for Overvoltage Sensing**

Figure 2 shows the behavior of CD pin during an OV sequence.



**Figure 2. CD Pin Mechanism**

**NOTE**

In the case of an Open Drain Active Low version, the  $V_{OUT}$  signal will be high and transition to low state when the voltage on the  $V_{CD}$  capacitor discharges to the set level based on the  $t_{CD}$  timer.

**Input Sense Voltage, Vx**

These inputs sense each battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

**Output Drive, OUT**

This terminal serves as the fault signal output, and may be ordered in either Active High or Open Drain Active Low options.

**Supply Input, VDD**

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

**External Delay Capacitor, CD**

This terminal is connected to an external capacitor that sets the delay timer during an overvoltage fault event.

The CD pin includes a timeout detection circuit to ensure that the output drives active even with a shorted or open capacitor during an overvoltage event.

The capacitor connected on the CD pin rapidly charges to a voltage if any one of the cell inputs exceeds the OV threshold. Then the delay circuit gradually discharges the capacitor on the CD pin. Once this capacitor discharges below a set voltage, the OUT transitions from an inactive to active state.

To calculate the delay, use the following equation:

$$t_{CD} \text{ (sec)} = K * C_{CD} \text{ (}\mu\text{F)}, \text{ where } K = 10 \text{ to } 20 \text{ range.} \tag{1}$$

Example: If  $C_{CD} = 0.1 \mu\text{F}$  (typical), then the delay timer range is

$$t_{CD} \text{ (sec)} = 10 * 0.1 = 1 \text{ s (Minimum)}$$

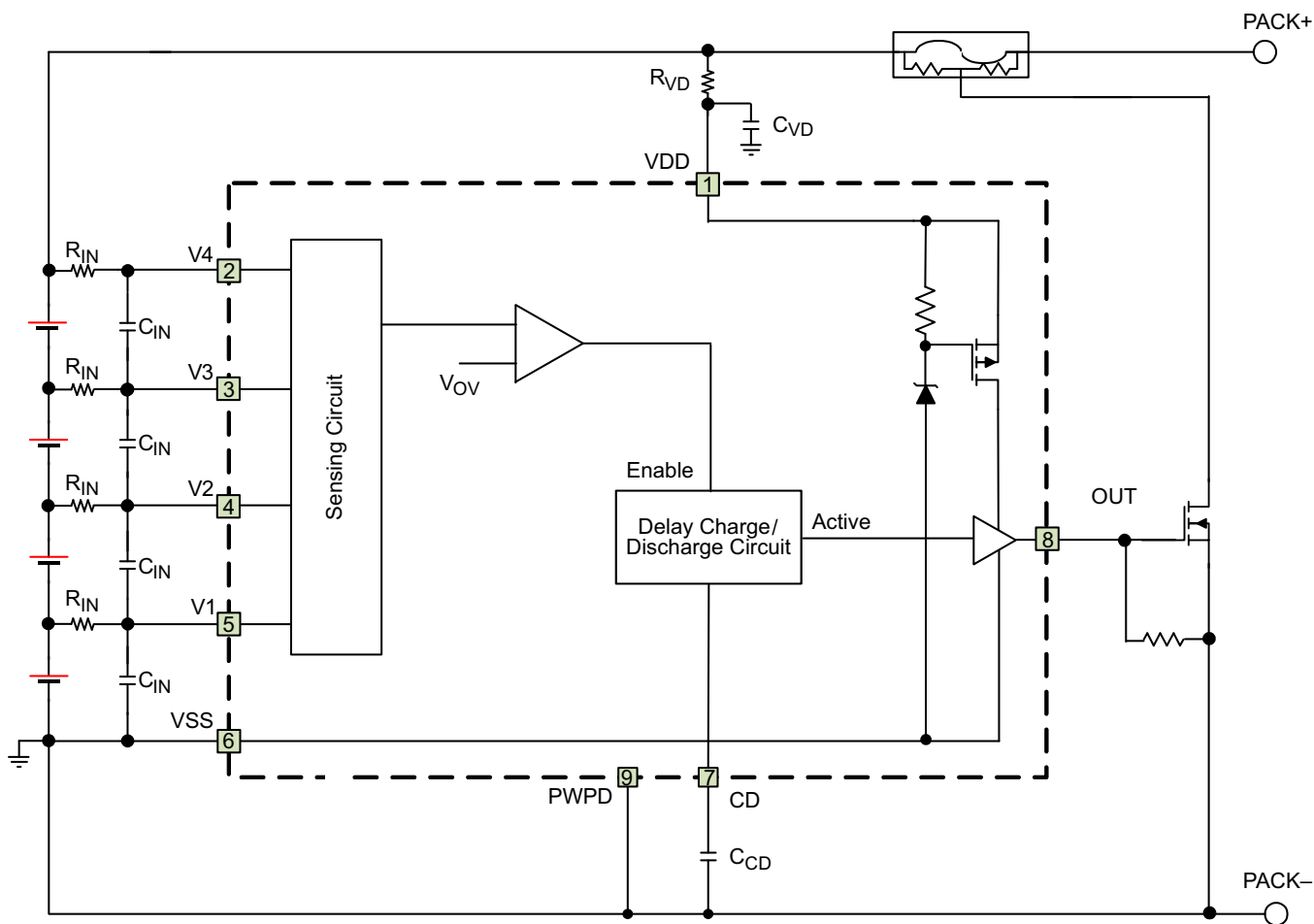
$$t_{CD} \text{ (sec)} = 20 * 0.1 = 2 \text{ s (Maximum)}$$

**NOTE**

The tolerance on the capacitor used for  $C_{CD}$  increases the range of the  $t_{CD}$  timer.

**FUNCTIONAL BLOCK DIAGRAM**

Figure 3 shows a CMOS Active High configuration.



**Figure 3. Block Diagram**

**NOTE**

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	CONDITION	VALUE/UNIT
Supply voltage range	VDD–VSS	–0.3 to 30 V
Input voltage range	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	–0.3 to 30 V
Output voltage range	OUT–VSS	–0.3 to 30 V
Continuous total power dissipation, P <sub>TOT</sub>		See package dissipation rating.
Storage temperature range, T <sub>STG</sub>		–65 to 150°C
Lead temperature (soldering, 10 s), T <sub>SOLDER</sub>		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>DD</sub> <sup>(1)</sup>		3		20	V
Input voltage range	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	0		5	V
Operating ambient temperature range, T <sub>A</sub>		–40		110	°C

(1) See [APPLICATION SCHEMATIC](#).

## DC CHARACTERISTICS

Typical values stated where T<sub>A</sub> = 25°C and V<sub>DD</sub> = 14.4 V, MIN/MAX values stated where T<sub>A</sub> = –40°C to 110°C and V<sub>DD</sub> = 3 V to 20 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Protection Thresholds						
V <sub>OV</sub>	V <sub>(PROTECT)</sub> Overvoltage Detection	bq294700, R <sub>IN</sub> = 1 kΩ		4.350		V
		bq294701, R <sub>IN</sub> = 1 kΩ		4.250		V
		bq294702, R <sub>IN</sub> = 1 kΩ		4.300		V
		bq294703, R <sub>IN</sub> = 1 kΩ		4.325		V
		bq294704, R <sub>IN</sub> = 1 kΩ		4.400		V
		bq294705, R <sub>IN</sub> = 1 kΩ		4.450		V
V <sub>HYS</sub>	OV Detection Hysteresis	bq2947xy <sup>(1)</sup>	250	300	400	mV
V <sub>OA</sub>	OV Detection Accuracy	T <sub>A</sub> = 25°C	–10		10	mV
V <sub>OADRIFT</sub>	OV Detection Accuracy Across Temperature	T <sub>A</sub> = –40°C	–40		40	mV
		T <sub>A</sub> = 0°C	–20		20	mV
		T <sub>A</sub> = 60°C	–24		24	mV
		T <sub>A</sub> = 110°C	–54		54	mV
Supply and Leakage Current						
I <sub>DD</sub>	Supply Current	(V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V at T <sub>A</sub> = 25°C (See <a href="#">Figure 14.</a> )		1	2	μA
I <sub>IN</sub>	Input Current at V <sub>x</sub> Pins	(V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V at T <sub>A</sub> = 25°C (See <a href="#">Figure 14.</a> )	–0.1		0.1	μA
I <sub>CELL</sub>	Input Current (ALL V <sub>x</sub> and V <sub>DD</sub> Input Pins)	Current Consumption at Power down, (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 2.30 V at T <sub>A</sub> = 25°C		1.1		μA
Output Drive OUT, CMOS Active High Versions Only						

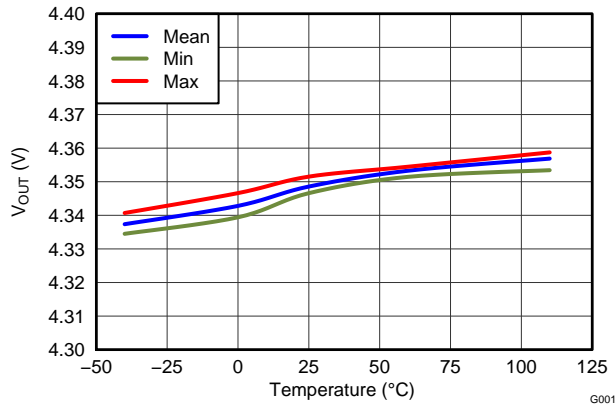
(1) Future option, contact TI.

## DC CHARACTERISTICS (continued)

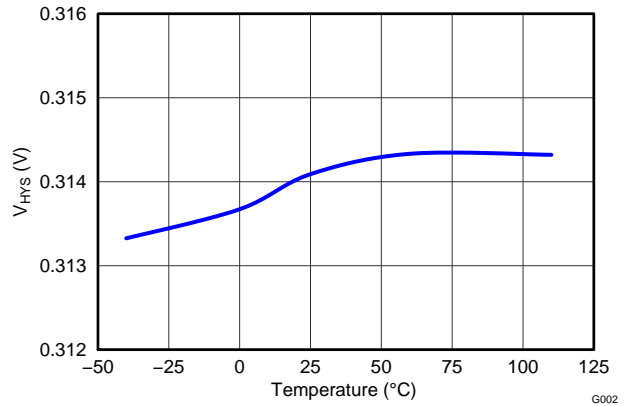
Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 14.4\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $110^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$  to  $20\text{ V}$  (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$V_{OUT}$	Output Drive Voltage, Active High	$(V4-V3), (V3-V2), (V2-V1),$ or $(V1-VSS) > V_{OV},$ $V_{DD} = 14.4\text{ V}, I_{OH} = 100\text{ }\mu\text{A}$	6			V
		If three of four cells are short circuited, only one cell remains powered and $> V_{OV},$ $V_{DD} = V_x$ (cell voltage), $I_{OH} = 100\text{ }\mu\text{A}$		$V_{DD} - 0.3$		V
		$(V4-V3), (V3-V2), (V2-V1),$ and $(V1-VSS) < V_{OV},$ $V_{DD} = 14.4\text{ V}, I_{OL} = 100\text{ }\mu\text{A}$ measured into OUT pin.		250	400	mV
$I_{OUTH}$	OUT Source Current (during OV)	$(V4-V3), (V3-V2), (V2-V1),$ or $(V1-VSS) > V_{OV},$ $V_{DD} = 14.4\text{ V},$ OUT = 0 V, measured out of OUT pin.			4.5	mA
$I_{OUTL}$	OUT Sink Current (no OV)	$(V4-V3), (V3-V2), (V2-V1),$ and $(V1-VSS) < V_{OV},$ $V_{DD} = 14.4\text{ V},$ OUT = VDD, measured into OUT pin. Pull resistor $R_{PU} = 5\text{ k}\Omega$ to VDD = 14.4 V	0.5		14	mA
Output Drive OUT, CMOS Open Drain Active Low Versions Only						
$V_{OUT}$	Output Drive Voltage, Active High	$(V4-V3), (V3-V2), (V2-V1),$ and $(V1-VSS) < V_{OV},$ $V_{DD} = 14.4\text{ V}, I_{OL} = 100\text{ }\mu\text{A}$ measured into OUT pin.		250	400	mV
$I_{OUTL}$	OUT Sink Current (no OV)	$(V4-V3), (V3-V2), (V2-V1),$ and $(V1-VSS) < V_{OV},$ $V_{DD} = 14.4\text{ V},$ OUT = VDD, measured into OUT pin. Pull resistor $R_{PU} = 5\text{ k}\Omega$ to VDD = 14.4 V	0.5		14	mA
$I_{OUTLK}$	OUT pin leakage	$(V4-V3), (V3-V2), (V2-V1),$ and $(V1-VSS) < V_{OV},$ $V_{DD} = 14.4\text{ V},$ OUT = VDD, measured into OUT pin.			100	nA
Delay Timer						
$t_{CD}$	OV Delay Time	$C_{CD} = 0.1\text{ }\mu\text{F}$ (see <a href="#">Equation 1</a> )	1	1.5	2	s
$t_{CD\_GND}$	OV Delay Time with CD pin = 0 V	Delay due to $C_{CD}$ capacitor shorted to ground for Customer Test Mode	20		170	ms

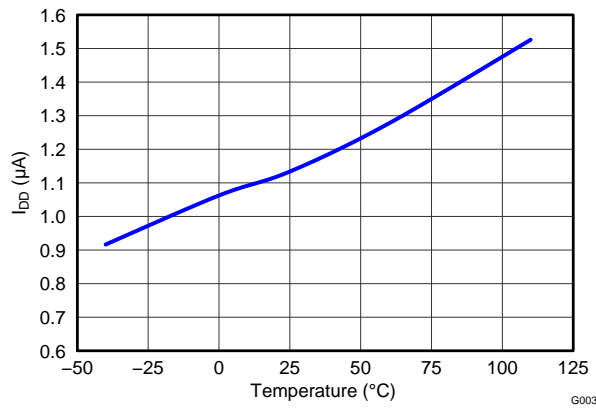
**TYPICAL CHARACTERISTICS**



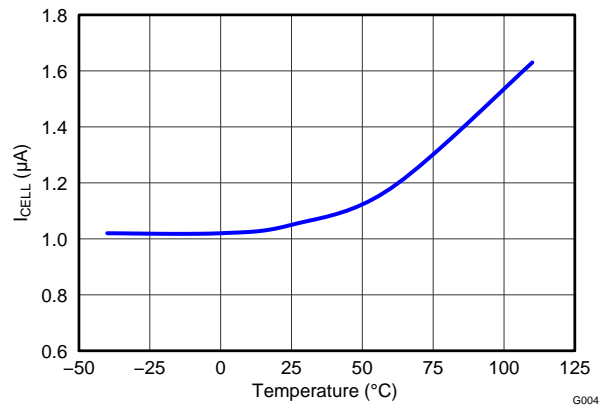
**Figure 4. Overtolerance Threshold (OVT) vs. Temperature**



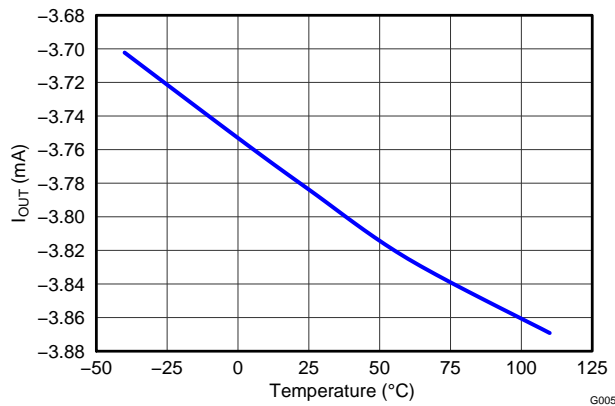
**Figure 5. Hysteresis V<sub>HYS</sub> vs. Temperature**



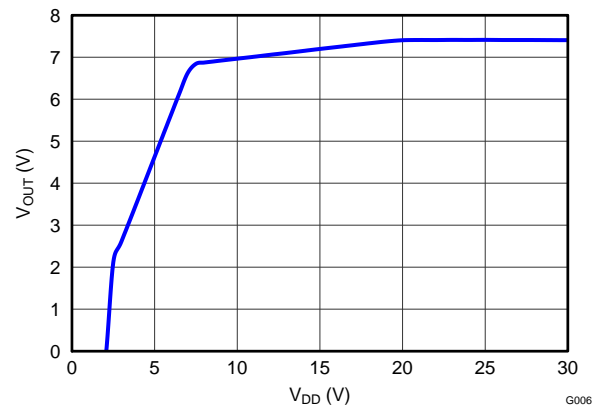
**Figure 6. I<sub>DD</sub> Current Consumption vs. Temperature at V<sub>DD</sub> = 16 V**



**Figure 7. I<sub>CELL</sub> vs. Temperature at V<sub>CELL</sub> = 9.2 V**



**Figure 8. Output Current I<sub>OUT</sub> vs. Temperature**



**Figure 9. V<sub>OUT</sub> vs. V<sub>DD</sub>**

## APPLICATION INFORMATION

Figure 10 shows the recommended reference design components.

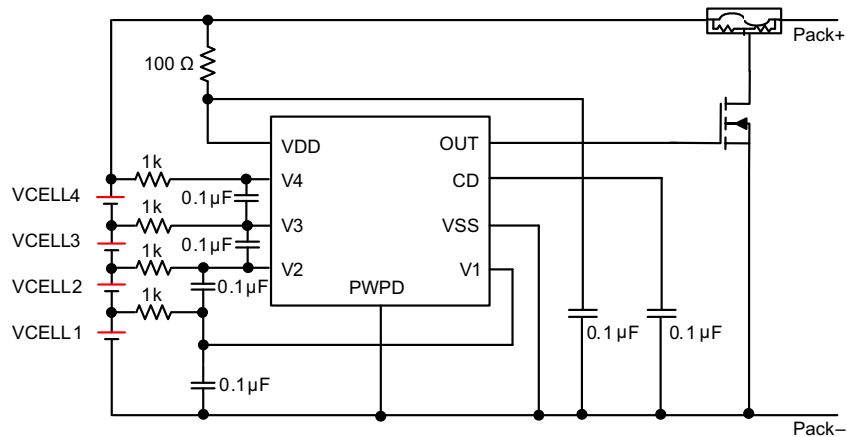


Figure 10. Application Configuration for Active High

### NOTE

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements.

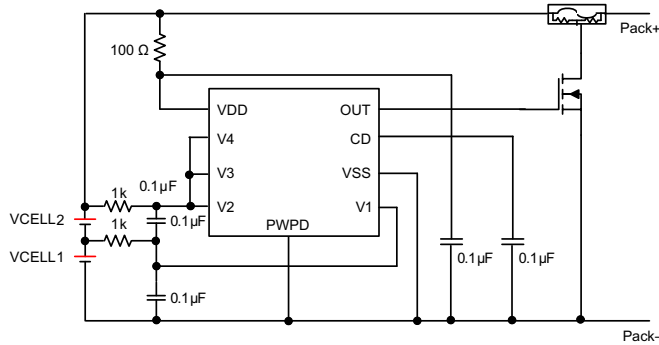
Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	$R_{IN}$	900	1000	4700	$\Omega$
Voltage monitor filter capacitance	$C_{IN}$	0.01	0.1	1.0	$\mu F$
Supply voltage filter resistance	$R_{VD}$	100		1	$K\Omega$
Supply voltage filter capacitance	$C_{VD}$		0.1	1.0	$\mu F$
CD external delay capacitance	$C_{CD}$		0.1	1.0	$\mu F$

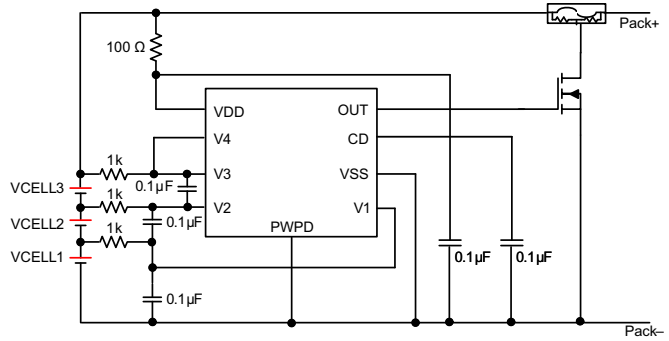
### NOTE

The device is calibrated using an  $R_{IN}$  value = 1 k $\Omega$ . Using a value other than this recommended value changes the accuracy of the cell voltage measurements and  $V_{OV}$  trigger level.

## APPLICATION SCHEMATIC



**Figure 11. 2-Series Cell Configuration Active High with Capacitor-Programmed Delay**



**Figure 12. 3-Series Cell Configuration Active High with Capacitor-Programmed Delay**

### NOTE

In these application examples of 2s and 3s, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

## CUSTOMER TEST MODE

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the  $t_{(CD\_GND)}$  value, which has a maximum of 170 ms.

Figure 13 shows the timing for the Customer Test Mode.

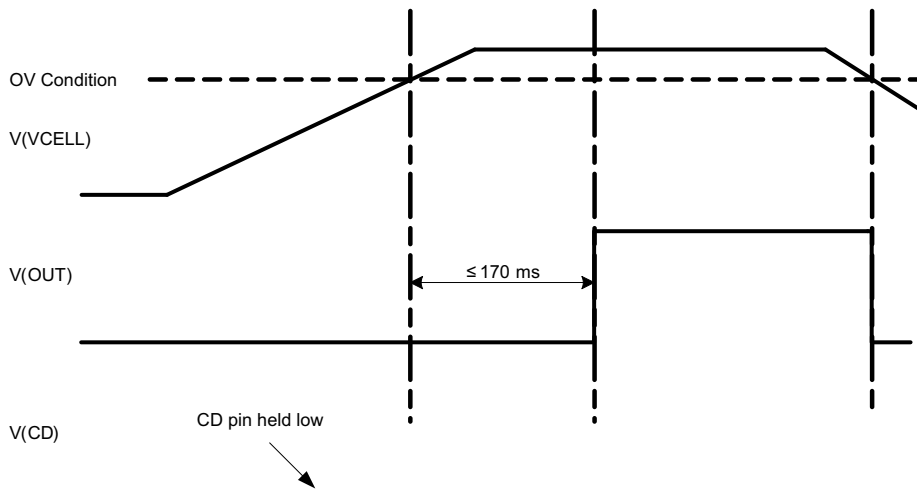


Figure 13. Timing for Customer Test Mode

Figure 14 shows the measurement for current consumption of the product for both VDD and Vx.

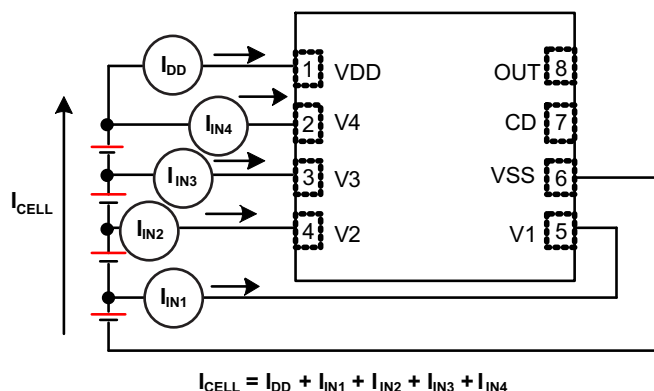


Figure 14. Configuration for IC Current Consumption Test

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
BQ294700DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294700DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294701DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294701DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294702DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294702DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294703DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294703DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294704DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294704DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294705DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294705DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294700DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294700DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294701DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294701DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294702DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294702DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294703DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294703DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294704DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294704DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294705DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294705DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

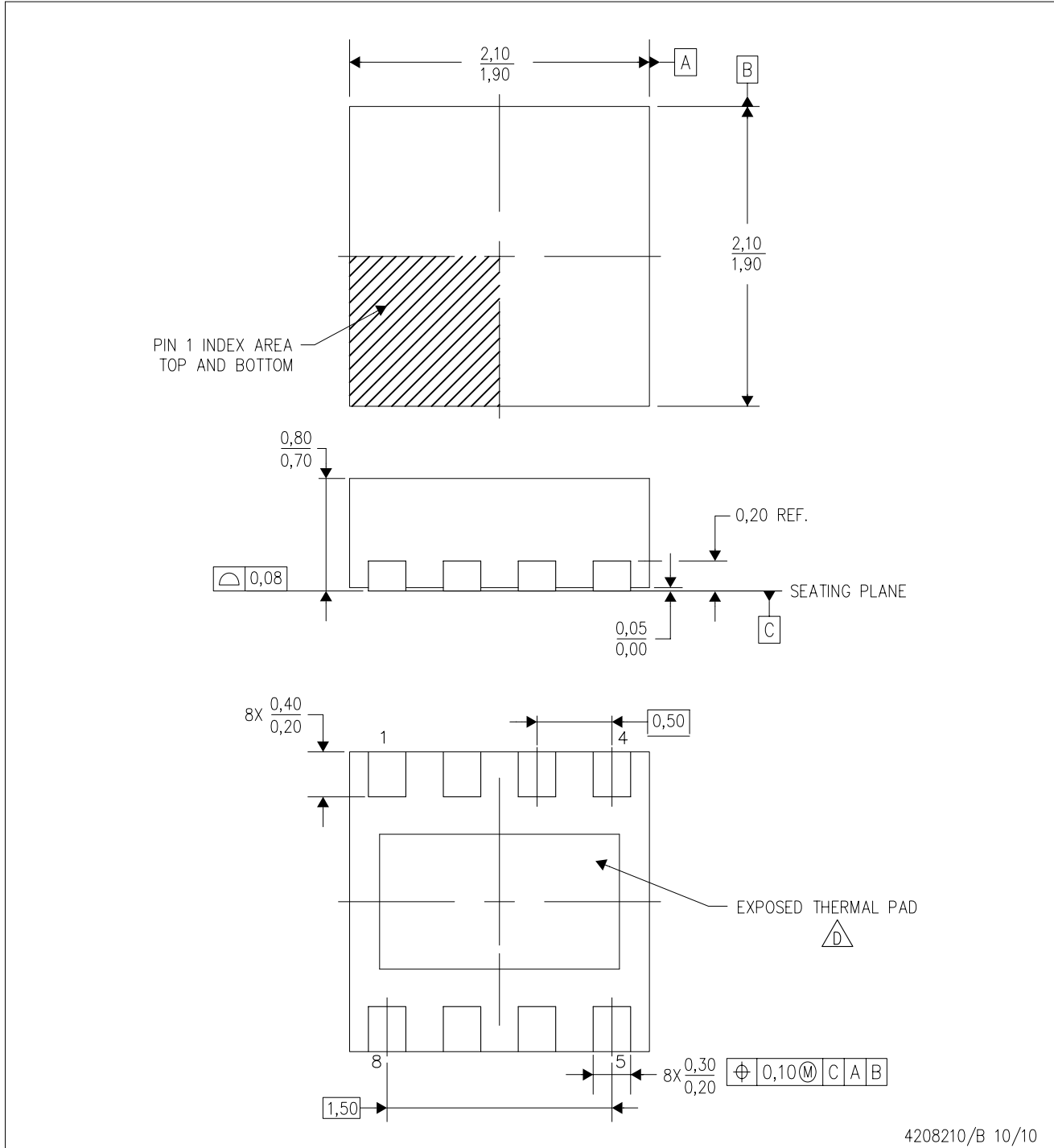
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294700DSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ294700DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294701DSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ294701DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294702DSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ294702DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294703DSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ294703DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294704DSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ294704DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294705DSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ294705DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-229.

## THERMAL PAD MECHANICAL DATA

DSG (S-PWSON-N8)

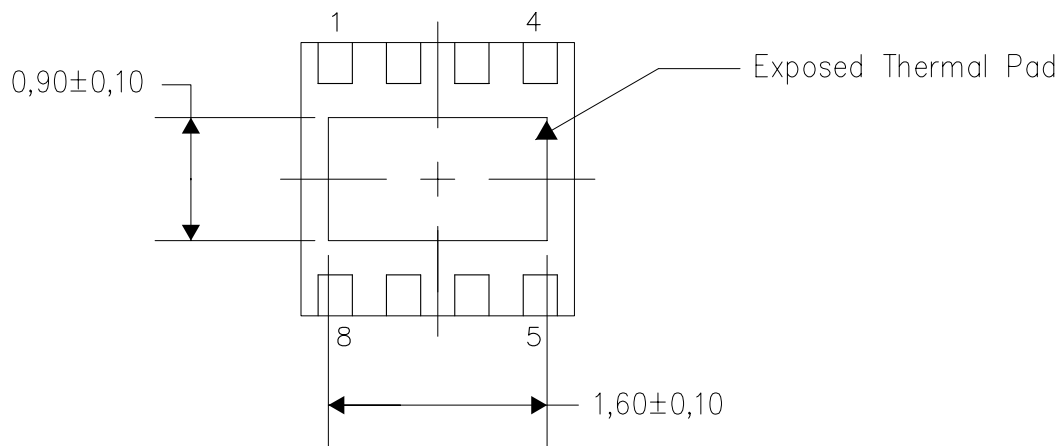
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

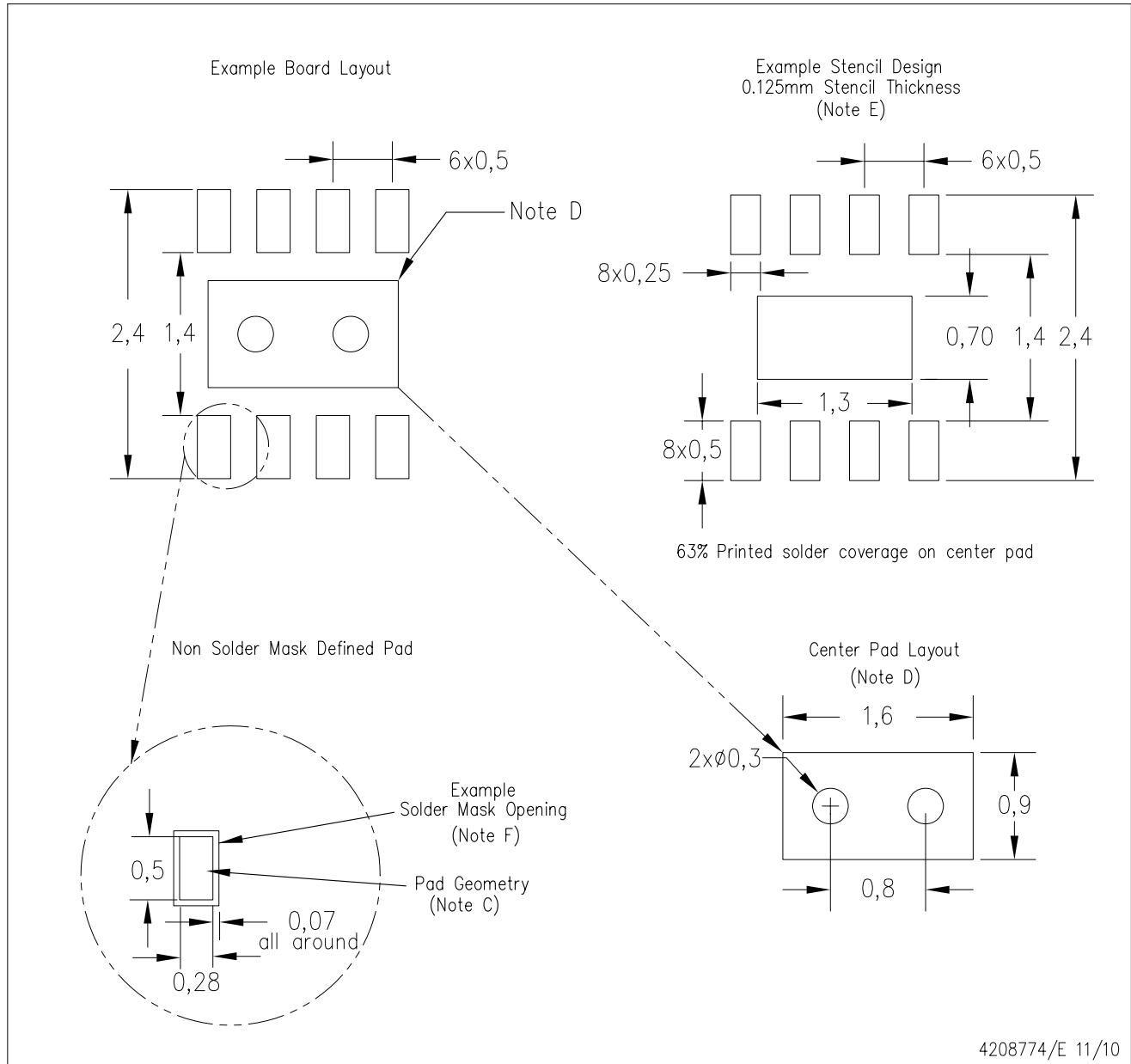


Bottom View

Exposed Thermal Pad Dimensions

4208347/E 11/10

NOTE: A. All linear dimensions are in millimeters



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

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