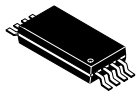
TEXAS INSTRUMENTS



SLUS491 – JULY 2001

LOW-COST BATTERY COULOMB COUNTER FOR EMBEDDED PORTABLE APPLICATIONS

FEATURES

- **Multifunction High-Accuracy Coulometric Charge and Discharge Counter**
- **Ideal for Portable Applications With Nonremovable Rechargeable Battery Pack**
- **Resolves Signals Less Than 12.5 μV**
- **Internal Offset Calibration Improves Accuracy**
- **128 Bytes of General-Purpose RAM**
- **Internal Temperature Sensor Eliminates the Need for an External Thermistor**
- **High-Accuracy Internal Timebase Eliminates External Crystal Oscillator**
- **Low Power Consumption:**
  - **Operating: < 80 μA**
  - **Sleep: < 10 μA**
- **Single-Wire HDQ Serial Interface**
- **Packaging: 8-Lead TSSOP**

DESCRIPTION

The bq26231 is a low-cost charge/discharge counter peripheral in an 8-pin TSSOP. It works with an intelligent host controller, providing state-of-charge information for rechargeable Li-Ion, Li-Pol, or NiMH batteries. The bq26231 measures the voltage drop across a low-value series sense resistor between the negative terminal of the battery and the battery pack ground contact. By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent host controller can determine battery state-of-charge information. To improve accuracy, an offset count register is available. The system host controller is responsible for the register maintenance by resetting the charge in/out and self-discharge registers as needed.

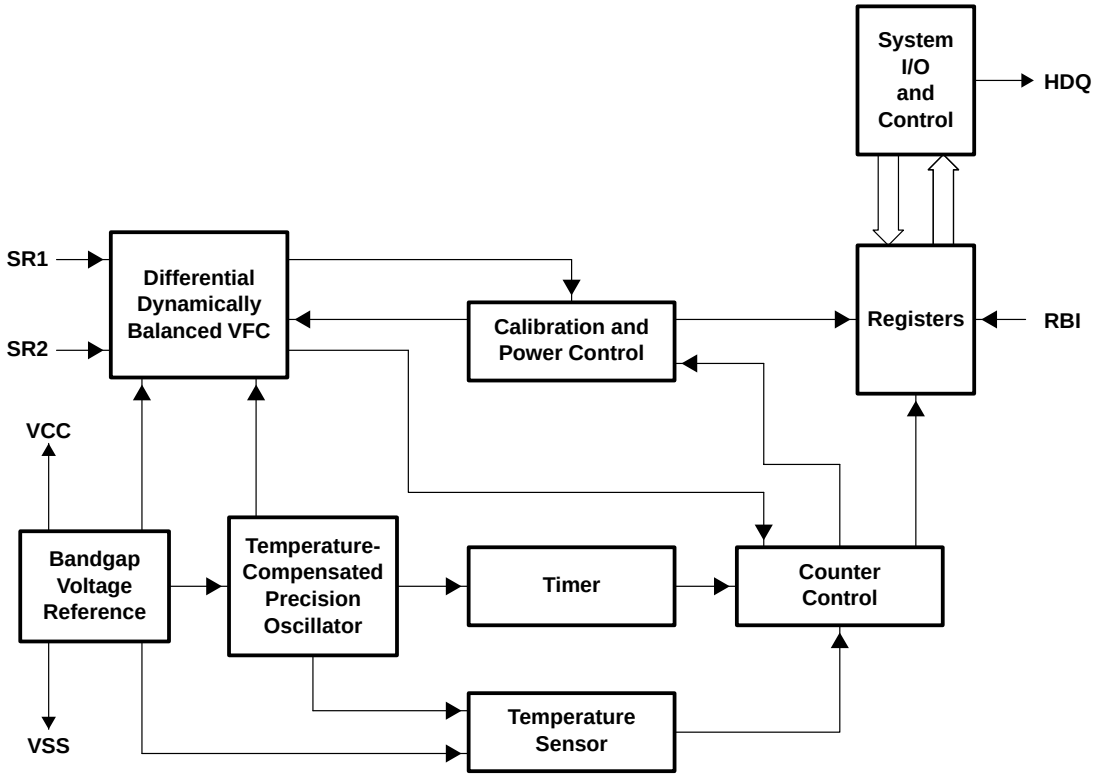
The bq26231 features 13 bytes of registers, which contain the capacity monitoring and status information. The RBI input operates from an external power storage source such as a capacitor or a series cell in the battery pack, providing register nonvolatility for periods when the battery is shorted to ground or when the battery charge state is not sufficient to operate the bq26231. During this mode, the register backup current is less than 100 nA. Packaged in an 8-pin TSSOP, the bq26231 is small enough to fit in the crevice between two A-size cells or within the width of a prismatic cell.

PW PACKAGE
(TOP VIEW)

AVAILABLE OPTIONS

T_{OPR}	PACKAGE
	8-Lead TSSOP (PW)
–20°C to 70°C	bq26231PW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	
NC	1		No connect. This pin must be left floating.	
VCC	2	I	Supply voltage	
VSS	3		Ground	
HDQ	4	I/O	Single-wire HDQ interface	
RBI	5	I	Register backup input	
SR1	6	I	Current sense input 1	
SR2	7	I	Current sense input 2	
NC	8		No connect. This pin must be left floating.	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{CC} with respect to V_{SS}) . . . . . –0.3 V to 6 V
Input voltage: HDQ (all with respect to V_{SS}) . . . . . –0.3 V to 6 V
RBI, SR1, and SR2 (with respect to V_{SS}) . . . . . V_{SS} – 0.3 V to V_{CC} + 3 V
Operating free-air temperature range, T_A . . . . . –20°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature (soldering, 10 s) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		2.8	4.25	5.5	V
Supply current, $I_{I(OP)}$	V_{CC} = 3.7 V, $V_{I(HDQ)}$ = 3.7 V		60	70	µA
	V_{CC} = 5.5 V, $V_{I(HDQ)}$ = 5.5 V		70	80	
Sleep current, $I_{I(SLEEP)}$	V_{CC} = 5.5 V			10	µA
RBI current, $I_{I(RBI)}$	V_{CC} < 2.4 V			100	nA
Operating ambient temperature, T_A		–20		70	°C

dc electrical characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{Il(HDQ)}$	Digital input low HDQ pin				0.8	V
$V_{IH(HDQ)}$	Digital input high HDQ pin		2.5			V
	SR1 and SR2 input impedance	–200 mV < $V_{(SR)}$ < 200 mV	10			MΩ

timer characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$E_{(TMR)}$	Timer accuracy error	3.5 V ≤ V_{CC} ≤ 3.9 V, 0°C ≤ T_A ≤ 70°C	–3%	1.5%	3%	

VFC characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR1 and SR2 input voltage		–200		200	mV
Offset voltage, $V_{(OS)}$				500	µV
Integrated nonlinearity	Add 0.05% per °C above or below 25°C and 0.5% per volt above or below 3.7 V		1%	2%	
Integrated nonrepeatability error	Measured repeatability given similar operating conditions		0.5%	1%	

standard serial communication timing specification over recommended operating temperature and supply voltage, refer to Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CYCH)}$	Cycle time, host to bq26231 (write)		190			µs
$t_{(CYCB)}$	Cycle time, bq26231 to host (read)		190	205	250	µs
$t_{(STRH)}$	Start hold, host to bq26231 (write)		5			ns
$t_{(STRB)}$	Start hold, bq26231 to host (read)		32			µs
$t_{(DSU)}$	Data setup (write)				50	µs
$t_{(DSUB)}$	Data setup (read)				50	µs
$t_{(DH)}$	Data hold		100			µs
$t_{(DV)}$	Data valid		80			µs
$t_{(SSUB)}$	Stop setup (bq26231 to host)				145	µs
$t_{(SSU)}$	Stop setup (host to bq26231)				145	µs
$t_{(B)}$	Break		190			µs
$t_{(BR)}$	Break recovery		40			µs
$t_{(RSPS)}$	Response time, bq26231 to host		190		320	µs

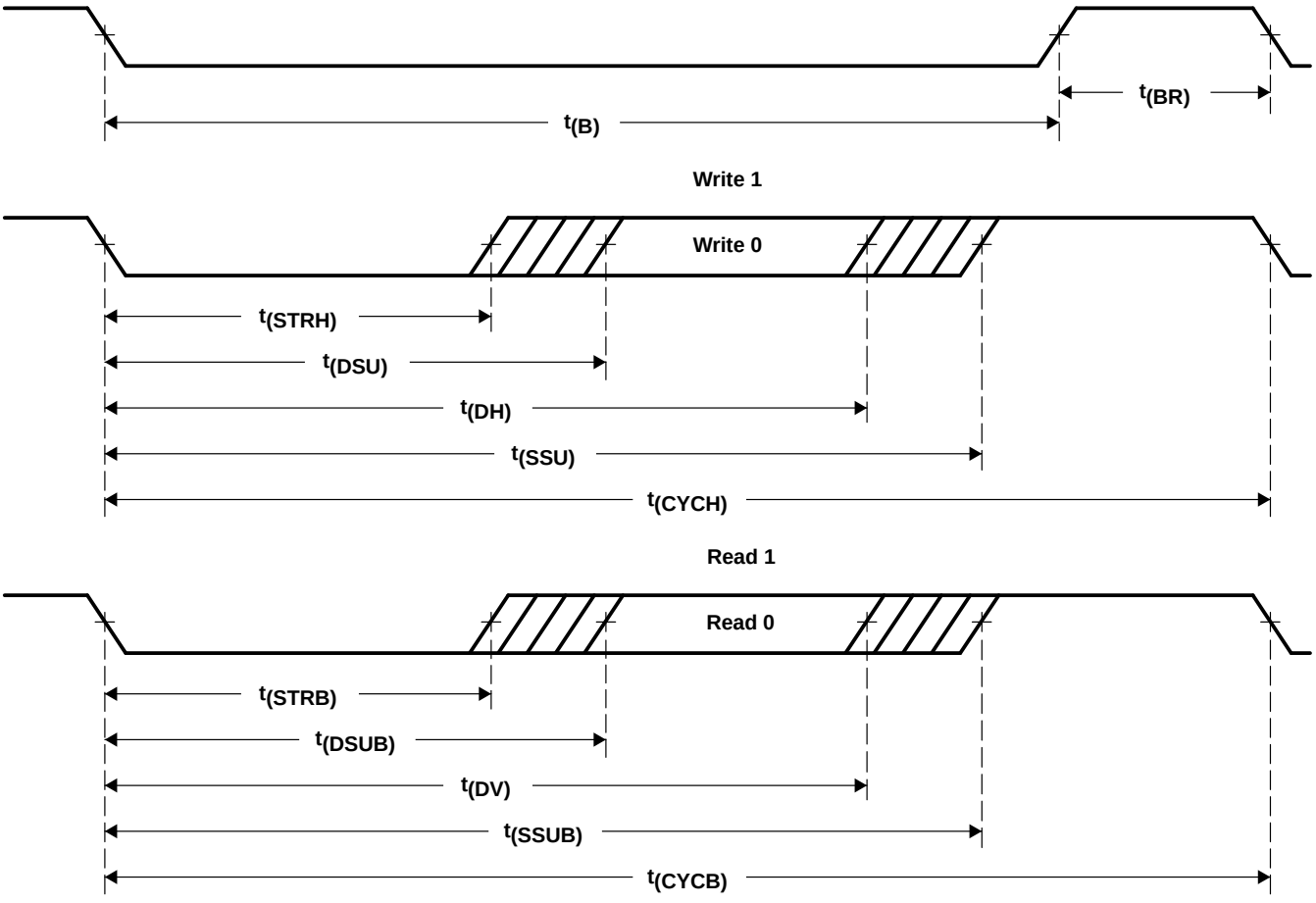


Figure 1. Standard Serial Communication Timing Diagram

detailed description

SR1–SR2 current sense inputs

The bq26231 interprets charge and discharge activity by monitoring and integrating the voltage drop $V_{(SR)}$ across pins SR1 and SR2. The SR1 input connects to the sense resistor and the negative terminal of the battery. The SR2 input connects to the sense resistor and the negative terminal of the pack. $V_{(SR1)} < V_{(SR2)}$ indicates discharge, and $V_{(SR1)} > V_{(SR2)}$ indicates charge. The effective voltage drop, $V_{(SRO)}$, as seen by the bq26231, is $V_{(SR)} + V_{(OS)}$. Valid input range is ±200 mV. A 100 kΩ series resistor is recommended to protect these inputs in case of a shorted battery.

HDQ data input/output

This bidirectional input/output communicates the register information to the host system. HDQ is open drain and requires a pullup/pulldown resistor in the battery pack to disable/enable sleep mode if the pack is removed from the system.

RBI register backup input

This input maintains the internal register states during periods when V_{CC} is below the minimum operating voltage.

APPLICATION INFORMATION

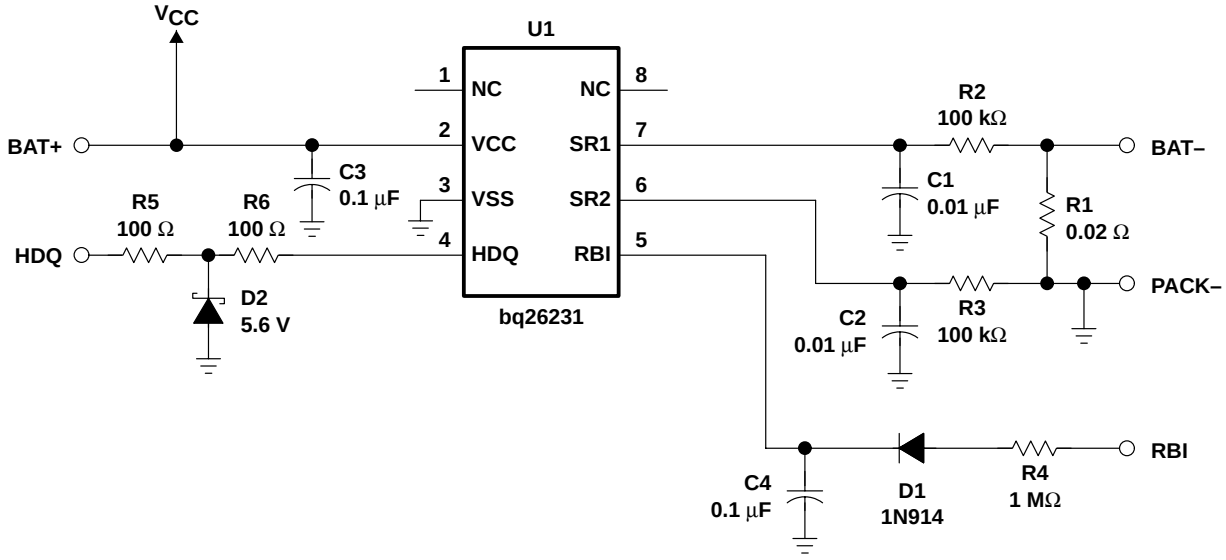


Figure 2. Typical Application

functional description

The bq26231 measures the voltage drop across a low-value series current sense resistor between the SR1 and SR2 pins using a voltage-to-frequency converter. This information is placed into various internal counter and timer registers. Using information from the bq26231, the system host can determine the battery state-of-charge, estimate self-discharge, and calculate the average charge and discharge currents. During pack storage periods, the use of an internal temperature sensor doubles the self-discharge count rate every 10° above 25°C.

A register is available to store the calculated offset, allowing current calibration. The offset cancellation register is written by the bq26231 during pack assembly and is available to the host system to adjust the current measurements. By adding or subtracting the offset value stored in the OFR, the true charge and discharge counts can be calculated to a high degree of certainty.

A typical application diagram is shown in Figure 2 and operation states are shown in Table 1.

Table 1. bq26231 Operational States

HDQ PIN	DCR/CCR/SCR	WOE	OPERATING STATE
HDQ high	Yes	$\lvert V_{(SRO)} \rvert > V_{(WOE)}$	Normal
HDQ high	Yes	$\lvert V_{(SRO)} \rvert < V_{(WOE)}$	Normal
HDQ low	No	$\lvert V_{(SRO)} \rvert < V_{(WOE)}$	Sleep

NOTE: $V_{(SRO)}$ is the voltage difference between SR1 and SR2 plus the offset voltage, $V_{(OS)}$.

RBI input

The RBI input pin is used with a storage capacitor or external supply to provide backup potential to the internal registers when V_{CC} drops below 2.4 V. The maximum discharge current is 100 nA in this mode. The bq26231 outputs V_{CC} on RBI when the supply is above 2.4 V; therefore, a diode is required to isolate an external supply. (See the application diagram.)

APPLICATION INFORMATION

functional description (continued)

charge and discharge count operation

Table 2 shows the main counters and registers of the bq26231. The bq26231 accumulates charge and discharge counts into two main count registers the discharge count register (DCR) and the charge count register (CCR). The bq26231 produces charge and discharge counts by sensing the voltage difference across a low-value resistor between the negative terminal of the battery pack and the negative terminal of the battery. The DCR or CCR counts depending on the signal between SR1 and SR2.

Table 2. bq26231 Counters

NAME	DESCRIPTION	RANGE	RAM SIZE
DCR	Discharge count register	$V_{(SR1)} < V_{(SR2)}$ (max = –200 mV) 12.5 μV increments	16 bit
CCR	Charge count register	$V_{(SR1)} > V_{(SR2)}$ (max = +200 mV) 12.5 μV increments	16 bit
SCR	Self-discharge count register	1 count/hour at 25°C	16 bit
DTC	Discharge time counter	1 count/0.8789 s (default) 1 count/225 s if STD is set	16 bit
CTC	Charge time counter	1 count/0.8789 s (default) 1 count/225 s if STC is set	16 bit

During discharge, the DCR and the discharge time counter (DTC) are active. If $V_{(SR1)}$ is less than $V_{(SR2)}$, indicating a discharge, the DCR counts at a rate equivalent to 12.5 μV every hour, and the DTC counts at a rate of 1 count/0.8789 seconds (4096 counts per hour). For example, a –100 mV signal produces 8000 DCR counts and 4096 DTC counts each hour. The amount of charge removed from the battery is easily calculated.

During charge, the CCR and the charge time counter (CTC) are active. If $V_{(SR1)}$ is greater than $V_{(SR2)}$, indicating a charge, the CCR counts at a rate equivalent to 12.5 μV every hour, and the CTC counts at a rate of 1 count/0.8789 seconds. For example, a +100 mV signal produces 8000 CCR counts and 4096 CTC counts each hour. The amount of charge added to the battery can easily be calculated.

The DTC and the CTC are 16-bit registers, and roll over beyond FFFF hex. If a rollover occurs, the corresponding bit in the MODE/WOE register is set, and the counter will subsequently increment at 1/256 of the normal rate (16 counts/hr). Whenever the signal between SR1 and SR2 is above the wake-up output enable (WOE) threshold and the HDQ pin is high, the bq26231 is in its full operating state. In this state, the DCR, CCR, DTC, CTC, and SCR are fully operational, and the WAKE output is low. During this mode, the internal RAM registers of the bq26231 may be accessed over the HDQ pin, as described in the section *Communicating With the 26230*.

If the signal between SR1 and SR2 is below the WOE threshold (refer to the *Mode/Wake-Up Enable Register* section for details) and HDQ remains low for greater than 10 seconds, the bq26231 enters a sleep mode where all register counting is suspended. The bq26231 remains in this mode until HDQ returns high.

For self-discharge calculation, the self-discharge count register (SCR) counts at a rate equivalent to 1 count every hour at a nominal 25°C. This rate and doubles approximately every 10°C up to 60°C. The SCR count rate is halved every 10°C below 25°C down to 0°C. The value in SCR is useful in determining an estimation of the battery self-discharge based on capacity and storage temperature conditions.

At any time during pack assembly, by invoking the calibration mode, the bq26231 may be programmed to measure the voltage offset between SR1 and SR2. The offset register (OFR) stores the bq26231 offset. The bit 2s complement value stored in the OFR is scaled the same units as the DCR and CCR, representing the amount of positive or negative offset in the bq26231. The maximum offset for the bq26231 is specified as ± 500 μV. Care should be taken to ensure proper PCB layout. Using OFR, the system host can cancel most of the effects of bq26231 offset for greater resolution and accuracy.

APPLICATION INFORMATION

charge and discharge count operation (continued)

Figure 3 shows the bq26231 register address map. The bq26231 uses the upper 13 locations. The remaining memory can store user-specific information such as chemistry, serial number, and manufacturing date.

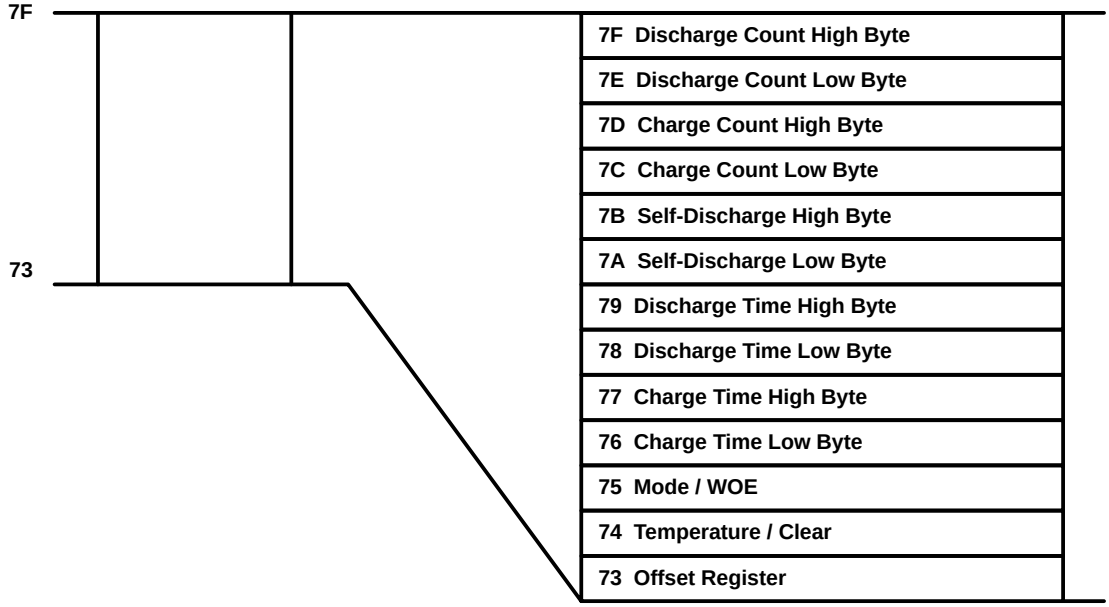


Figure 3. bq26231 Register Map

temperature

The bq26231 has an internal temperature sensor to set the value in the temperature register (TMP/CLR) and to set the self-discharge count rate value. The register reports the temperature in 8 steps of 10°C from < 0°C to > 60°C as Table 3 specifies. The bq26231 temperature sensor has typical accuracy of ±2°C at 25°C. See the TMP/CLR register description for more details.

Table 3. Temperature Steps

TEMPERATURE	VALUE (hex)	SDR COUNT RATE
< 0°C	0h	× 1/8
0–10°C	1h	× 1/4
10–20°C	2h	× 1/2
20–30°C	3h	1 count/hr
30–40°C	4h	× 2
40–50°C	5h	×c4
50–60°C	6h	× 8
>60°C	7h	× 16

APPLICATION INFORMATION

CLEAR register

The host system is responsible for register maintenance. To facilitate this maintenance, the bq26231 has a clear register (TMP/CLR) designed to reset the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq26231 completes the reset, the corresponding bit in the TMP/CLR register is automatically reset to 0, which saves the host an extra write/read cycle. Clearing the DTC register clears the STD bit and sets the DTC count rate to the default value of 1 count per 0.8789 s. Clearing the CTC register clears the STC bit and sets the CTC count rate to the default value of 1 count per 0.8789 s.

calibration mode

The system can enable bq26231 $V_{(OS)}$ calibration by setting the calibration bit in the MODE/WOE register (bit 6) to 1. The bq26231 then enters calibration mode when the HDQ line is low for greater than 10 seconds and when the signal between SR1 and SR2 pins is below $V_{(WOE)}$.

CAUTION:

Ensure that no low-level external signal is present between SR1 and SR2, because it affects the calibration value that the bq26231 calculates.

If HDQ remains low for one hour and $|V_{(SR)}| < V_{(WOE)}$ for the entire time, the measured $V_{(OS)}$ is latched into the OFR register, and the calibration bit is reset to zero, indicating to the system that the calibration cycle is complete. Once calibration is complete, the bq26231 enters a low-power mode until HDQ goes high, indicating that an external system is ready to access the bq26231. If HDQ transitions high before completion of the $V_{(OS)}$ calculation or if $|V_{(SR)}| > V_{(WOE)}$, then the calibration cycle is reset. The bq26231 then postpones the calibration cycle until the conditions are met. The calibration bit does not reset to zero until a valid calibration cycle is completed. The requirement for HDQ to remain low for the calibration cycle can be disabled by setting the OVRDQ bit to 1. In this case, calibration continues as long as $|V_{(SR)}| < V_{(WOE)}$. The OVRDQ bit is reset to zero at the end of a valid calibration cycle.

communicating with the bq26231

The bq26231 includes a simple single-wire (referenced to VSS) serial data interface. A host processor uses the interface to access various bq26231 registers.

NOTE:

The HDQ pin requires an external pullup or pulldown resistor.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq26231. The command directs the bq26231 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data from a register specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/s. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq26231 may be sampled using the pulse-width capture timers available on some microcontrollers. A UART may also be used to communicate through the HDQ pin.

If a communication timeout occurs (i.e., if the host waits longer than $t_{(CYCB)}$ for the bq26231 to respond, or if this is the first access command), then a break should be sent by the host. The host may then resend the command. The bq26231 detects a break when the HDQ pin is driven to a logic-low state for time $t_{(B)}$ or greater. The HDQ pin then returns to its normal ready-high logic state for a time, $t_{(BR)}$. The bq26231 is then ready to receive a command from the host processor.

APPLICATION INFORMATION

communicating with the bq26231 (continued)

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq26231 taking the HDQ pin to a logic-low state for a period $t_{(STRH,B)}$. The next section is the actual data transmission, where the data should be valid by a period $t_{(DSU,B)}$ after the negative edge used to start communication. The data should be held for a period $t_{(DV)}$ / $t_{(DH)}$, to allow the host or bq26231 to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period $t_{(SSU,B)}$ after the negative edge used to start communication. The final logic-high state should be held for a period $t_{(CYCH,B)}$, to allow the bit transmission to cease properly. The Standard Serial Communication Timing Specification table and Figure 1 give the timings for data and break communication.

Communication with the bq26231 always occurs with the least-significant bit being transmitted first. Figure 4 shows an example of a communication sequence to read the bq26231 OFR register.

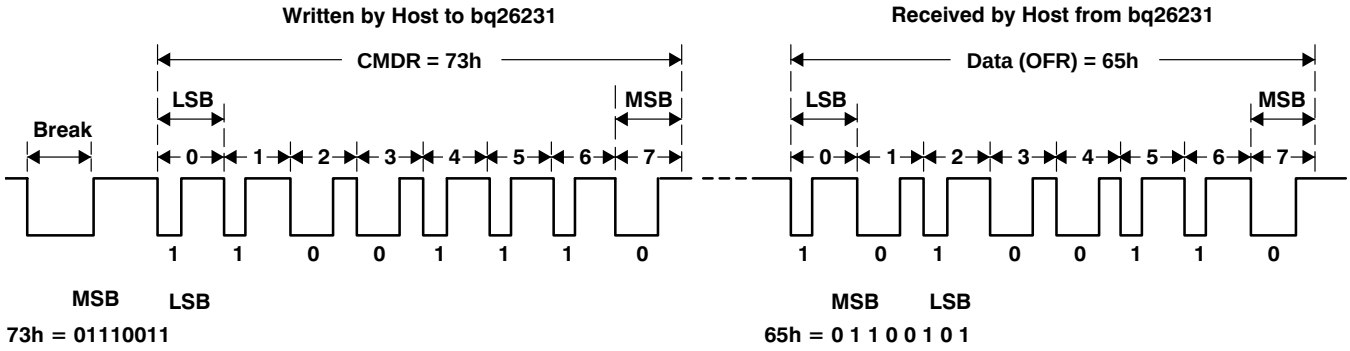


Figure 4. Typical Communication With the bq26231

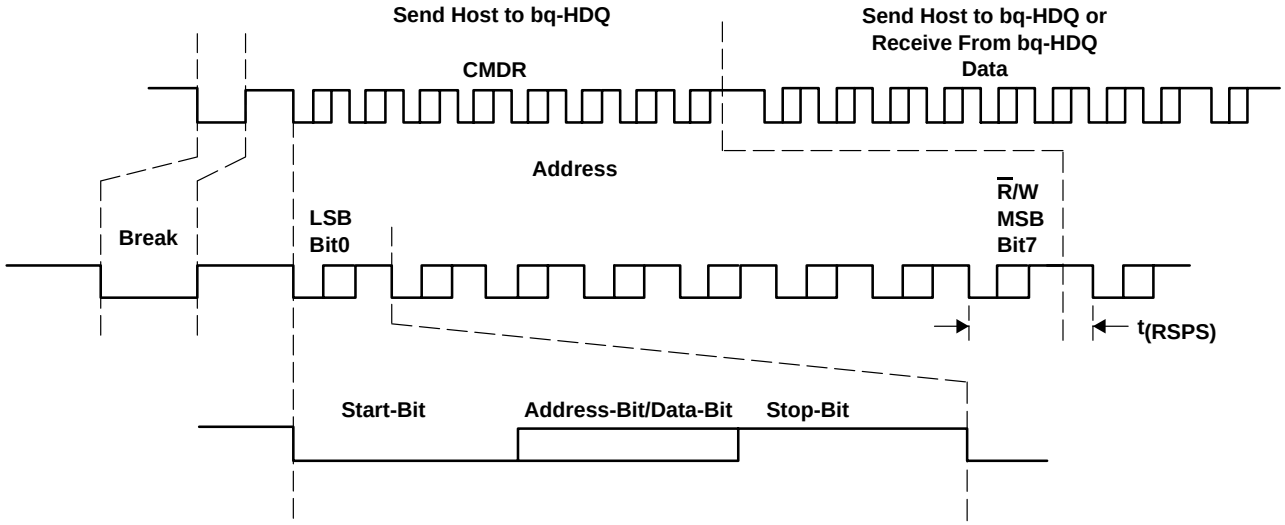


Figure 5. Communication Frame Example

APPLICATION INFORMATION

bq26231 command and status registers

The bq26231 command and status registers are listed and described in Table 4.

command (CMDR)

The write-only command register is accessed when the bq26231 has received eight contiguous valid command bits. The command register contains two fields:

- W/$\overline{R}$
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function. The W/$\overline{R}$ values are:

CDMR BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
W/$\overline{R}$	–	–	–	–	–	–	–

where W/$\overline{R}$ is

0 The bq26231 outputs the requested register contents specified by the address portion of the CMDR.

1 The following eight bits should be written to the register specified by the address portion of the CMDR.

Table 4. bq26231 Command and Status Registers

Symbol	Register Name	HDQ Address (hex)	Read/ Write	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0 (LSB)
CMDR	Command register	–	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
DCRH	Discharge count register high byte	7F	Read	DCRH7	DCRH6	DCRH5	DCRH4	DCRH3	DCRH2	DCRH1	DCRH0
DCRL	Discharge count register low byte	7E	Read	DCRL7	DCRL6	DCRL5	DCRL4	DCRL3	DCRL2	DCRL1	DCRL0
CCRH	Charge count register high byte	7D	Read	CCRH7	CCRH6	CCRH5	CCRH4	CCRH3	CCRH2	CCRH1	CCRH0
CCRL	Charge count register low byte	7C	Read	CCRL7	CCRL6	CCRL5	CCRL4	CCRL3	CCRL2	CCRL1	CCRL0
SCRH	Self-discharge count register high byte	7B	Read	SCRH7	SCRH6	SCRH5	SCRH4	SCRH3	SCRH2	SCRH1	SCRH0
SCRL	Self-discharge count register low byte	7A	Read	SCRL7	SCRL6	SCRL5	SCRL4	SCRL3	SCRL2	SCRL1	SCRL0
DTCH	Discharge time count high byte	79	Read	DTCH7	DTCH6	DTCH5	DTCH4	DTCH3	DTCH2	DTCH1	DTCH0
DTCL	Discharge time count low byte	78	Read	DTCL7	DTCL6	DTCL5	DTCL4	DTCL3	DTCL2	DTCL1	DTCL0
CTCH	Charge time count high byte	77	Read	CTCH7	CTCH6	CTCH5	CTCH4	CTCH3	CTCH2	CTCH1	CTCH0
CTCL	Charge time count low byte	76	Read	CTCL7	CTCL6	CTCL5	CTCL4	CTCL3	CTCL2	CTCL1	CTCL0
MODE/ WOE	Mode/WOE register	75	Read/ Write	OVERDQ	CAL	STC	STD	WOE3	WOE2	WOE1	0
TMP/ CLR	Temperature/clear register	74	Read/ Write	TMP2	TMP1	TMP0	CTC	DTC	SCR	CCR	DCR
OFR	Offset register	73	Read/ Write	OFR7	OFR6	OFR5	OFR4	OFR3	OFR2	OFR1	OFR0

APPLICATION INFORMATION

command (CMDR) (continued)

The lower seven-bit field of CMDR contains the address portion of the register to be accessed.

CDMR BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
–	AD6	AD5	AD4	AD3	AD2	AD1	AD0

discharge count registers (DCRH/DCRL)

The DCRH high-byte register (address = 7F hex) and the DCRL low-byte register (address = 7E hex) contain the count of the discharge and are incremented whenever $V_{(SR1)} < V_{(SR2)}$. These registers continue to count beyond FFFF hex, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the DCRH and DCRL to zero.

charge count registers (CCRH/CCRL)

The CCRH high-byte register (address = 7D hex) and the CCRL low-byte register (address = 7C hex) contain the count of the charge, and are incremented whenever $V_{(SR1)} > V_{(SR2)}$. These registers continue to count beyond FFFF hex, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the CCRH and CCRL to zero.

self-discharge count registers (SCRH/SCRL)

The SCRH high-byte register (address = 7B hex) and the SCRL low-byte register (address = 7A hex) contain the self-discharge count. These registers are continually updated when the bq26231 is in its normal operating mode. The counts in these registers are incremented based on time and temperature. The SCR counts at a rate of 1 count per hour at 20–30°C and doubles every 10°C to greater than 60°C (16 counts/hour). The count will halve every 10°C below 20–30°C to less than 0°C (1 count/8 hours). These registers continue to count beyond FFFF hex, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the SCRH and SCRL to zero.

discharge time count registers (DTCH/DTCL)

The DTCH high-byte register (address = 79 hex) and the DTCL low-byte register (address = 78 hex) are used to determine the length of time the $V_{(SR1)} < V_{(SR2)}$, indicating a discharge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the DTCH/DTCL register continues to count beyond FFFF hex, the STD bit is set in the MODE/WOE register, indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour. The TMP/CLR register is used to force the reset of both the DTCH and DTCL to zero.

NOTE:

If a second rollover occurs, STD is cleared. Access to the bq26231 should be timed to clear DTCH/DTCL more often than every 170 days.

charge time count registers (CTCH/CTCL)

The CTCH high-byte register (address = 77 hex) and the CTCL low-byte register (address = 76 hex) are used to determine the length of time the $V_{(SR1)} > V_{(SR2)}$, indicating a charge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the CTCH/CTCL registers continue to count beyond FFFF hex, the STC bit is set in the MODE/WOE register, indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour. The TMP/CLR register is used to force the reset of both the CTCH and CTCL to zero.

NOTE:

If a second rollover occurs, STD is cleared. Access to the bq26231 should be timed to clear CTCH/CTCL more often than every 170 days.

APPLICATION INFORMATION

mode/wake-up enable register

The Mode/WOE register (address = 75 hex) contains the calibration and wake-up enable information, and the STC and STD bits as described below.

The override DQ (OVRDQ) bit (bit 7) is used to override the requirement for HDQ to be low before initiating $V_{(OS)}$ calibration. This bit is normally set to zero. If OVRDQ is written to one, the bq26231 begins offset calibration when $|V_{(SR)}| < V_{(WOE)}$ where HDQ = Don't care.

The OVRDQ location is

MODE/WOE BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVERDQ	–	–	–	–	–	–	–

where OVRDQ is

0 HDQ = 0 and $|V_{(SR)}| < V_{(WOE)}$ for $V_{(OS)}$ calibration to begin

1 HDQ = Don't care and $|V_{(SR)}| < V_{(WOE)}$ for $V_{(OS)}$ calibration to begin

NOTE:

The OVRDQ bit should only be used in conjunction with a calibration cycle. Normal operation of the bq26231 is not ensured when this bit is set. After a valid calibration cycle, bit 7 is reset to zero.

The calibration (CAL) bit 6 is used to enable the bq26231 offset calibration test. Setting this bit to 1 enables a $V_{(OS)}$ calibration whenever HDQ is low (default), and $|V_{(SR)}| < V_{(WOE)}$. This bit is cleared to 0 by the bq26231 whenever a valid $V_{(OS)}$ calibration is completed, and the OFR register is updated with the new calculated offset. The bit remains 1 if the offset calibration was not completed.

The CAL location is

MODE/WOE BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
–	CAL	–	–	–	–	–	–

where CAL is

0 Valid offset calibration

1 Offset calibration pending

The slow time charge (STC) and slow time discharge (STD) flags indicate if the CTC or DTC registers have rolled over beyond FFFF hex. STC set to 1 indicates a CTC rollover; STD set to 1 indicates a DTC rollover.

The STC and STD locations are

MODE/WOE BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
–	–	STC	STD	–	–	–	–

where STC/STD is

0 No rollover

1 Rollover occurred in the corresponding CTC/DTC register.

The WOE bits (bits 3–1) are used in conjunction with the CAL bit for the calibration process. When the CAL bit is set to 1, the bq26231 enables a $V_{(OS)}$ calibration whenever HDQ is low (default), and $|V_{(SR)}| < V_{(WOE)}$. On bq26231 initialization (power-on reset) the WOE bits are set to1. Setting all of these bits to zero is not valid. Refer to Table 5 for the various WOE values.

APPLICATION INFORMATION

mode/wake-up enable register (continued)

The WOE 3–1 locations are

MODE/WOE BITS							
7	6	5	4	3	2	1	0
–	–	–	–	WOE3	WOE2	WOE1	–

where WOE3–1 is determined by dividing 3.84 mV by the value in WOE.

NOTE:
Bit 0 of the MODE/WOE register is reserved and *must* remain 0.

Table 5. WOE Thresholds

WOE3–1 (hex)	$V_{(WOE)}$ (mV)
0	N/A
1	3.840
2	1.920
3	1.280
4	0.960
5	0.768
6	0.640
7 (default after POR)	0.549

temperature and clear register

The TMP/CLR register (address = 74 hex) is used to give the present temperature step between < 0°C and > 60°C and clear the various count registers. The values of the TMP0–TMP2 (bits 5–7) denote the current temperature step sense by the bq26231 as outlined in Table 3. The bq26231 temperature sense is trimmed to ±2°C typical (±4°C maximum).

The TMP2–0 locations are

TMP/CLR BITS							
7	6	5	4	3	2	1	0
$\overline{\text{TMP2}}$	TMP1	TMP0	–	–	–	–	–

where TMP2–0 is the temperature step sensed by this bq26231.

The Clear bits (Bits 0–4) are used to reset the various bq26231 counters and STC and STD bits to zero. Writing the bits to 1 resets the corresponding register to 0. The clear bit resets to 0, indicating a successful register reset. Each clear bit is independent, so it is possible to clear the DCRH/DCRL registers without affecting the values in any other bq26231 register. The high-byte and low-byte registers are both cleared when the corresponding bit is written to 1.

APPLICATION INFORMATION

temperature and clear register (continued)

The clear bit locations are

TMP/CLR BITS							
7	6	5	4	3	2	1	0
–	–	–	CTC	DTC	SCR	CCR	DCR

Where:

The CTC bit (bit 4) resets both the CTCH and CTCL registers and the STC bit to 0.

The DTC bit (bit 3) resets both the DTCH and DTCL registers and the STD bit to 0.

The SCR bit (bit 2) resets both the SCRH and SCRL registers to 0.

The CCR bit (bit 1) resets both the CCRH and CCRL registers to 0.

The DCR bit (bit 0) resets both the DCRH and DCRL registers to 0.

offset register (OFR)

The OFR register (address = 73 hex) is used to store the calculated $V_{(OS)}$ of the bq26231. The OFR value can be used to cancel the voltage offset between $V_{(SR1)}$ and $V_{(SR2)}$. The up/down offset counter is centered at zero. The actual offset is an 8-bit 2s complement value located in OFR.

The OFR locations are

TMP/CLR BITS							
7	6	5	4	3	2	1	0
OFR7	OFR6	OFR5	OFR4	OFR3	OFR2	OFR1	OFR0

where OFR7 is

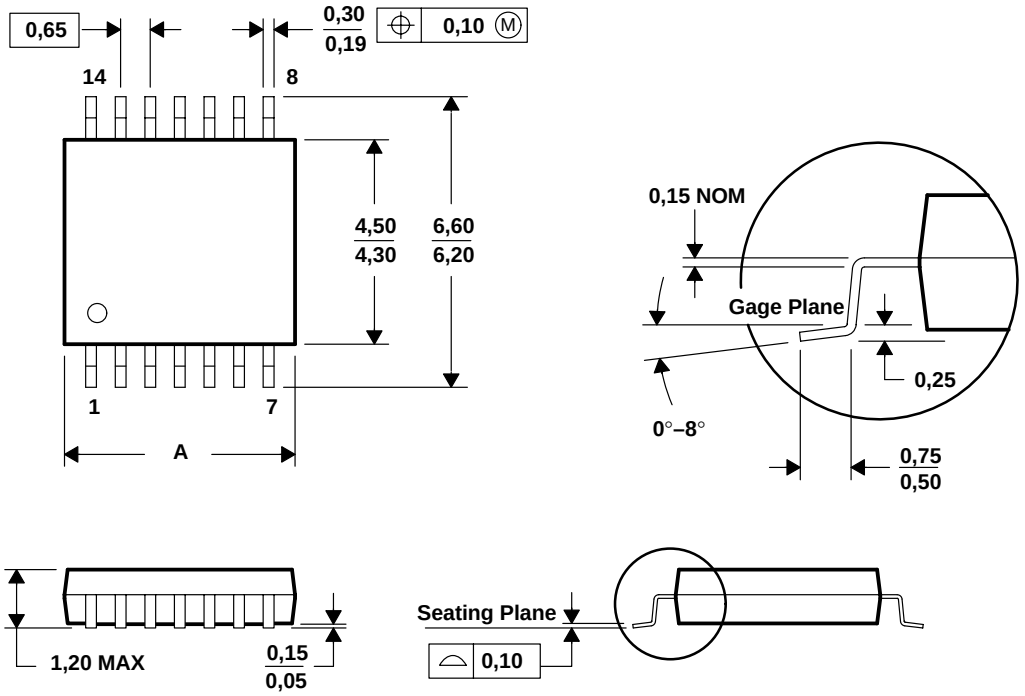
0 Discharge

1 Charge

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ26231PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ26231PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ26231PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ26231PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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