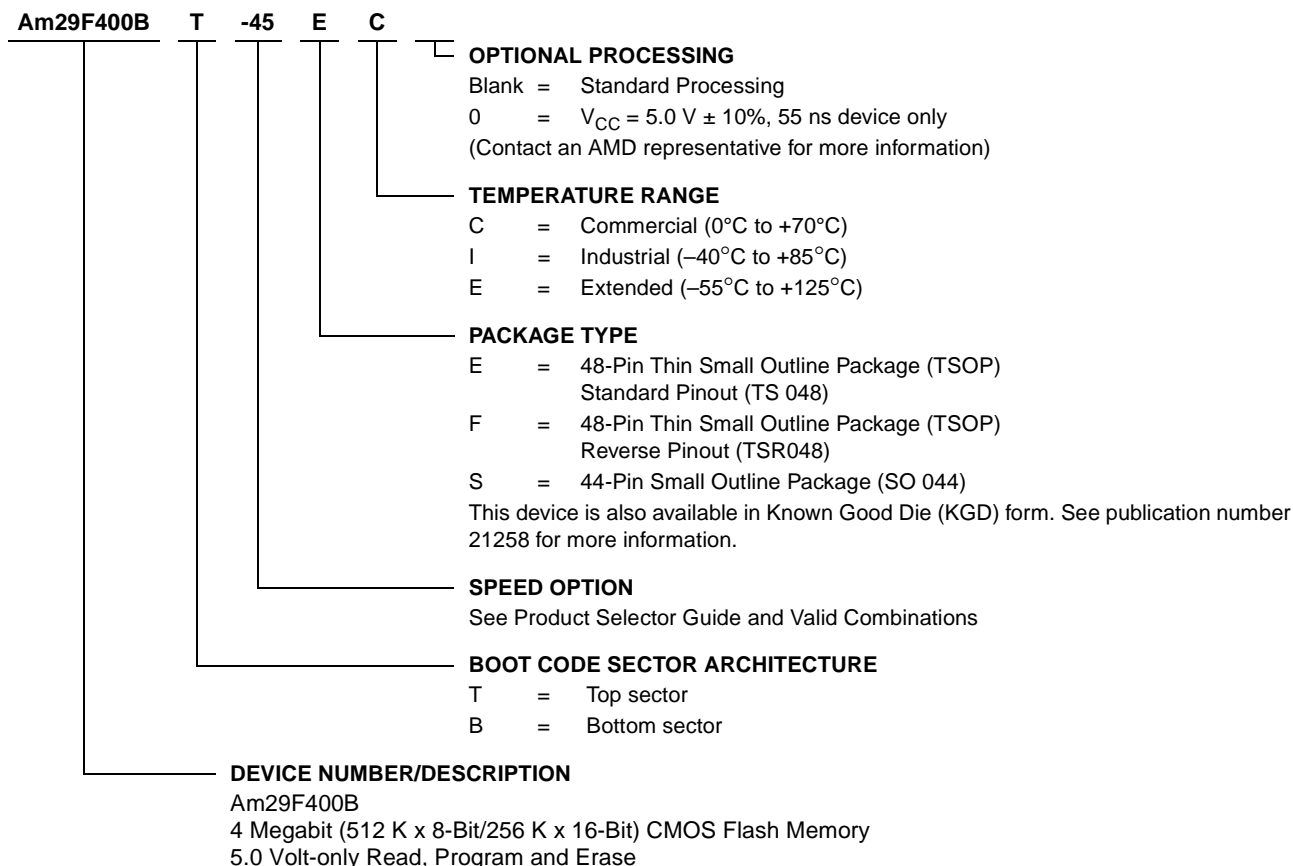


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		Voltage Range
AM29F400BT-45, AM29F400BB-45,	EC, EI, FC, FI, SC, SI	5.0 V $\pm$ 5%
AM29F400BT-50, AM29F400BB-50	EC, EI, EE, FC, FI, FE, SC, SI, SE	
AM29F400BT-55, AM29F400BB-55		
AM29F400BT-55, AM29F400BB-55	EC0, EI0, EE0, FC0, FI0, FE0, SC0, SI0, SE0	5.0 V $\pm$ 10%
AM29F400BT-70, AM29F400BB-70	EC, EI, EE, FC, FI, FE, SC, SI, SE	
AM29F400BT-90, AM29F400BB-90		
AM29F400BT-120, AM29F400BB-120		
AM29F400BT-150, AM29F400BB-150		

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of

the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

**Table 1. Am29F400B Device Bus Operations**

Operation	CE#	OE#	WE#	RESET#	A0–A17	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V <sub>IH</sub>	BYTE# = V <sub>IL</sub>
Read	L	L	H	H	A <sub>IN</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	High-Z
Write	L	H	L	H	A <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	High-Z
CMOS Standby	V <sub>CC</sub> ± 0.5 V	X	X	V <sub>CC</sub> ± 0.5 V	X	High-Z	High-Z	High-Z
TTL Standby	H	X	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Temporary Sector Unprotect (See Note)	X	X	X	V <sub>ID</sub>	A <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	X

**Legend:**

L = Logic Low = V<sub>IL</sub>, H = Logic High = V<sub>IH</sub>, V<sub>ID</sub> = 12.0 ± 0.5 V, X = Don't Care, D<sub>IN</sub> = Data In, D<sub>OUT</sub> = Data Out, A<sub>IN</sub> = Address In

**Note:** See the sections on Sector Group Protection and Temporary Sector Unprotect for more information.

### Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

### Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V<sub>IL</sub>. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V<sub>IH</sub>. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert

valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See “Reading Array Data” for more information. Refer to the AC Read Operations table for timing specifications and to Figure 9 for the timing diagram. I<sub>CC1</sub> in the DC Characteristics table represents the active current specification for reading array data.

### Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V<sub>IL</sub>, and OE# to V<sub>IH</sub>.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to “Word/Byte Configuration” for more information.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 2 and 3 indicate the address space that each sector occupies. A “sector address” consists of the address bits required to uniquely select a sector. The “Command Definitions” section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.