Am29F040B

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **21445** Revision **E** Amendment **0** Issue Date **November 29, 2000**

Am29F040B

4 Megabit (512 K x 8-Bit)
CMOS 5.0 Volt-only, Uniform Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% for read and write operations**
  - — Minimizes system level power requirements
- **Manufactured on 0.32 µm process technology**
  - — Compatible with 0.5 µm Am29F040 device
- **High performance**
  - — Access times as fast as 55 ns
- **Low power consumption**
  - — 20 mA typical active read current
  - — 30 mA typical program/erase current
  - — 1 µA typical standby current (standard access time to active mode)
- **Flexible sector architecture**
  - — 8 uniform sectors of 64 Kbytes each
  - — Any combination of sectors can be erased
  - — Supports full chip erase
  - — Sector protection:

    A hardware method of locking sectors to prevent any program or erase operations within that sector
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies bytes at specified addresses
- **Minimum 1,000,000 program/erase cycles per sector guaranteed**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system
- **Package options**
  - — 32-pin PLCC, TSOP, or PDIP
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply Flash standard
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends a sector erase operation to read data from, or program data to, a non-erasing sector, then resumes the erase operation

Publication# **21445** Rev: **E** Amendment/**0**
Issue Date: **November 29, 2000**

GENERAL DESCRIPTION

The Am29F040B is a 4 Mbit, 5.0 volt-only Flash memory organized as 524,288 Kbytes of 8 bits each. The 512 Kbytes of data are divided into eight sectors of 64 Kbytes each for flexible erase capability. The 8 bits of data appear on DQ0–DQ7. The Am29F040B is offered in 32-pin PLCC, TSOP, and PDIP packages. This device is designed to be programmed in-system with the standard system 5.0 volt V_{CC} supply. A 12.0 volt V_{PP} is not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

This device is manufactured using AMD's 0.32 µm process technology, and offers all the features and benefits of the Am29F040, which was manufactured using 0.5 µm process technology. In addtion, the Am29F040B has a second toggle bit, DQ2, and also offers the ability to program in the Erase Suspend mode.

The standard Am29F040B offers access times of 55, 70, 90, 120, and 150 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

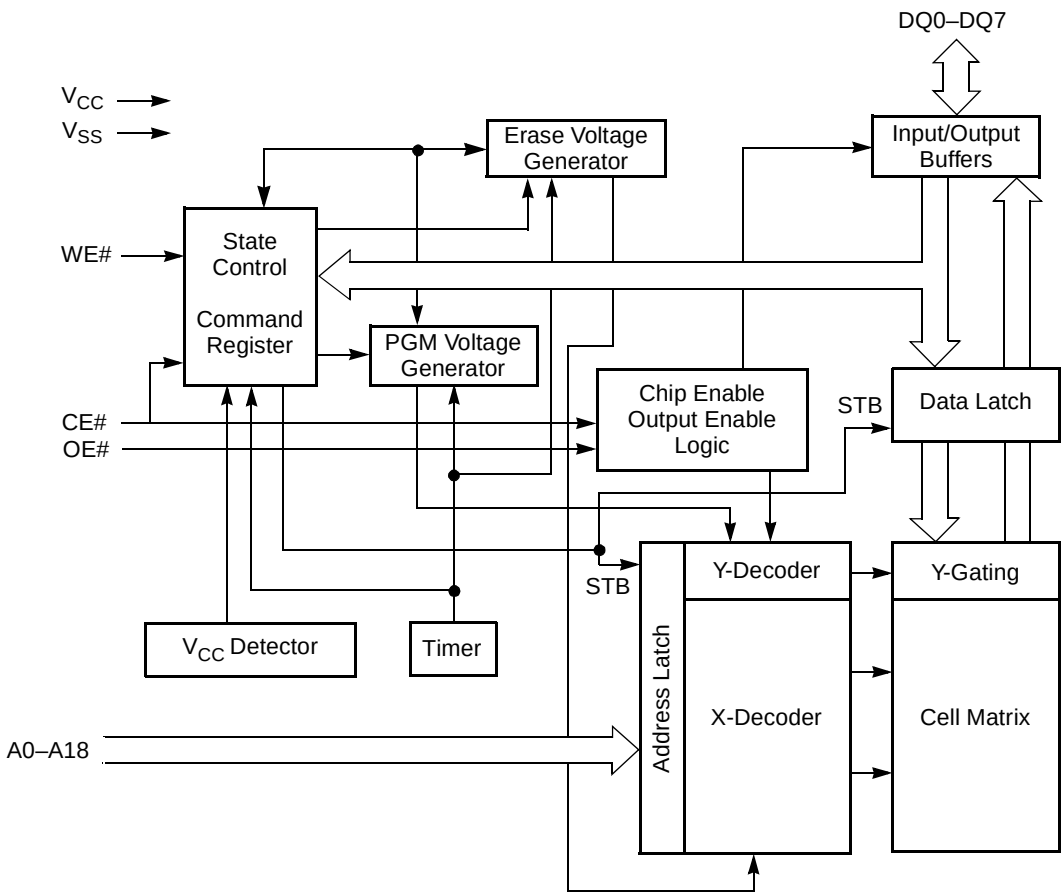
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

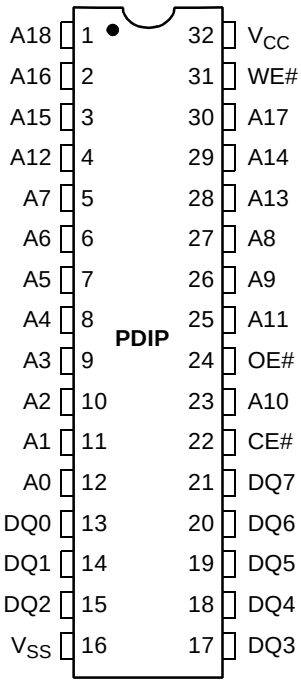
Family Part Number		Am29F040B				
Speed Option	V_{CC} = 5.0 V ± 5%	**-55**				
	V_{CC} = 5.0 V ± 10%		**-70**	**-90**	**-120**	**-150**
Max access time, ns (t_{ACC})		55	70	90	120	150
Max CE# access time, ns (t_{CE})		55	70	90	120	150
Max OE# access time, ns (t_{OE})		25	30	35	50	55

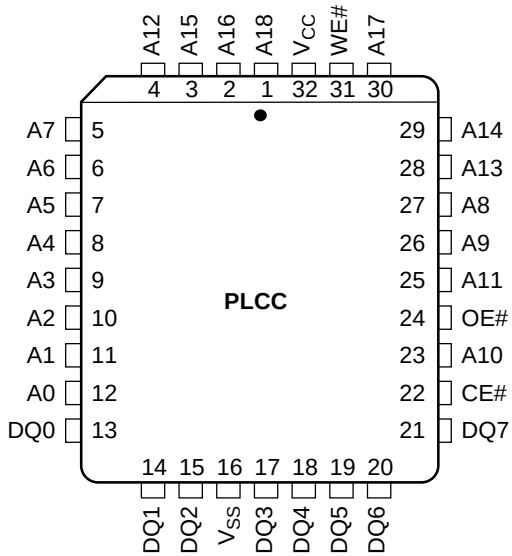
Note: *See the "AC Characteristics" section for more information.*

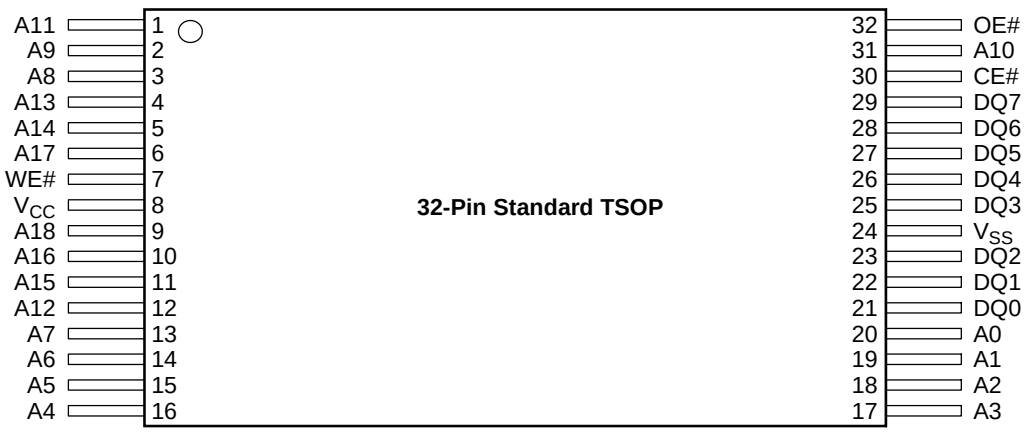
BLOCK DIAGRAM

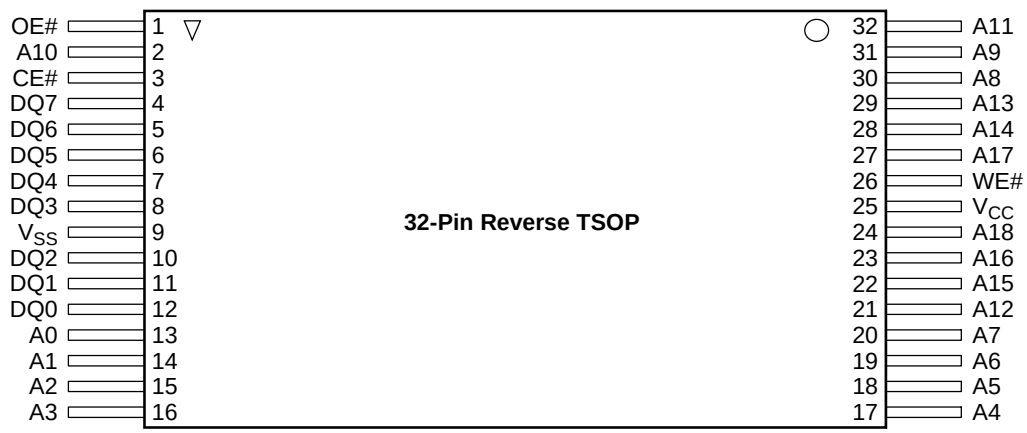


CONNECTION DIAGRAMS









PIN CONFIGURATION

A0–A18 = Address Inputs

DQ0–DQ7 = Data Input/Output

CE# = Chip Enable

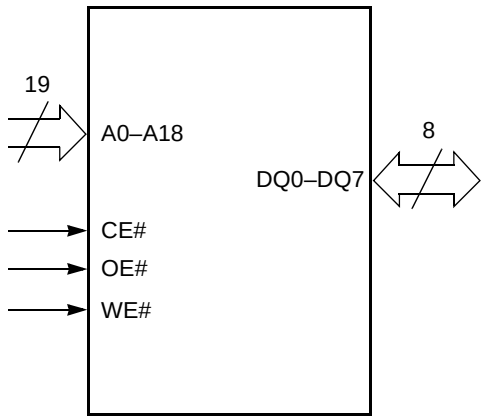
WE# = Write Enable

OE# = Output Enable

V_{SS} = Device Ground

V_{CC} = +5.0 V single power supply (see Product Selector Guide for device speed ratings and voltage supply tolerances)

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29F040B -55 E C

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 032)
F = 32-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F040B
4 Megabit (512 K x 8-Bit) CMOS 5.0 Volt-only Sector Erase Flash Memory
5.0 V Read, Program, and Erase

Valid Combinations		V_{CC} Voltage
AM29F040B-55	JC, JI, JE, EC, EI, EE, FC, FI, FE	5.0 V ± 5%
AM29F040B-70		5.0 V ± 10%
AM29F040B-90	PC, PI, PE, JC, JI, JE, EC, EI, EE, FC, FI, FE	
AM29F040B-120		
AM29F040B-150		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29F040B Device Bus Operations

Operation	CE#	OE#	WE#	A0–A20	DQ0–DQ7
Read	L	L	H	A_{IN}	D_{OUT}
Write	L	H	L	A_{IN}	D_{IN}
CMOS Standby	$V_{CC} \pm 0.5$ V	X	X	X	High-Z
TTL Standby	H	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out, A_{IN} = Address In

Note: *See the "Sector Protection/Unprotection" section. for more information.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the

outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# pin is held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when CE# is held at V_{IH}. The device requires the standard access time (t_{CE}) before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics tables represents the standby current specification.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Addresses Table

Sector	A18	A17	A16	Address Range
SA0	0	0	0	00000h–0FFFFh
SA1	0	0	1	10000h–1FFFFh
SA2	0	1	0	20000h–2FFFFh
SA3	0	1	1	30000h–3FFFFh
SA4	1	0	0	40000h–4FFFFh
SA5	1	0	1	50000h–5FFFFh
SA6	1	1	0	60000h–6FFFFh
SA7	1	1	1	70000h–7FFFFh

Note: *All sectors are 64 Kbytes in size.*