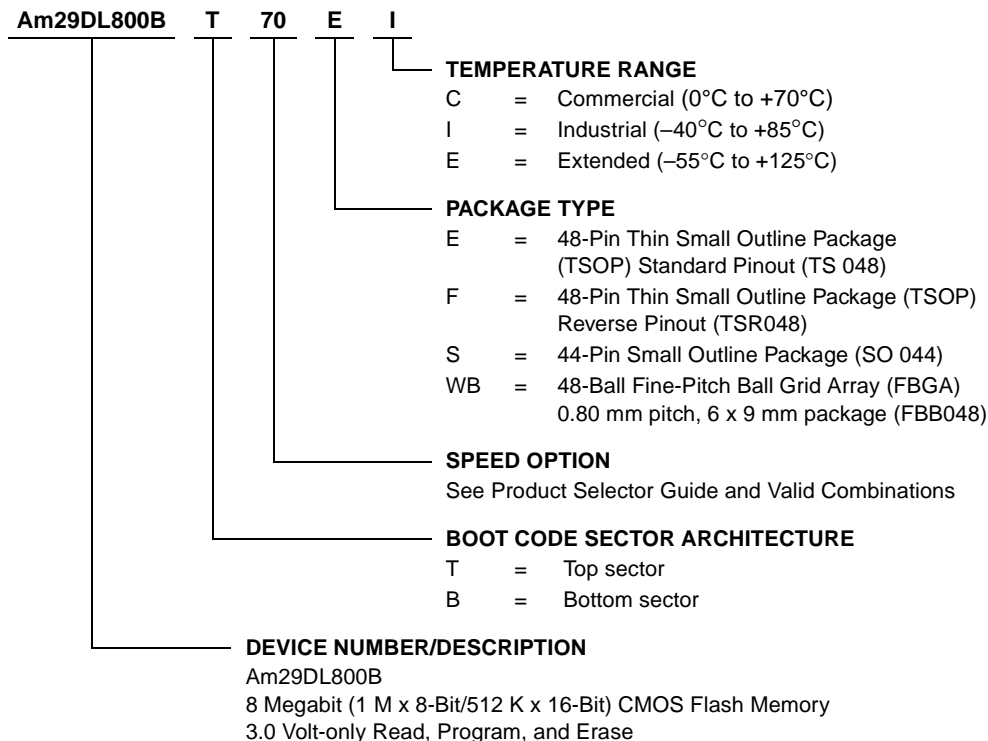


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations for TSOP and SO Packages	
AM29DL800BT70, AM29DL800BB70	EC, EI, FC, FI, SC, SI
AM29DL800BT90, AM29DL800BB90	EC, EI, EE, FC, FI, FE, SC, SI, SE
AM29DL800BT120, AM29DL800BB120	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations for FBGA Packages			
Order Number		Package Marking	
AM29DL800BT70, AM29DL800BB70	WBC, WBI	D800BT70V, D800BB70V	C, I
AM29DL800BT90, AM29DL800BB90	WBC, WBI, WBE	D800BT90V, D800BB90V	C, I, E
AM29DL800BT120, AM29DL800BB120		D800BT12V, D800BB12V	

## DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the

register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

**Table 1. Am29DL800B Device Bus Operations**

Operation	CE#	OE#	WE#	RESET#	Addresses (Note 1)	DQ0– DQ7	DQ8–DQ15	
							BYTE# = V <sub>IH</sub>	BYTE# = V <sub>IL</sub>
Read	L	L	H	H	A <sub>IN</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	
Standby	V <sub>CC</sub> ± 0.3 V	X	X	V <sub>CC</sub> ± 0.3 V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V <sub>ID</sub>	Sector Address, A6 = L, A1 = H, A0 = L	D <sub>IN</sub>	X	X
Sector Unprotect (Note 2)	L	H	L	V <sub>ID</sub>	Sector Address, A6 = H, A1 = H, A0 = L	D <sub>IN</sub>	X	X
Temporary Sector Unprotect	X	X	X	V <sub>ID</sub>	A <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	High-Z

**Legend:**

L = Logic Low = V<sub>IL</sub>, H = Logic High = V<sub>IH</sub>, V<sub>ID</sub> = 12.0 ± 0.5 V, X = Don't Care, A<sub>IN</sub> = Address In, D<sub>IN</sub> = Data In, D<sub>OUT</sub> = Data Out

**Notes:**

- Addresses are A18:A0 in word mode (BYTE# = V<sub>IH</sub>), A18:A-1 in byte mode (BYTE# = V<sub>IL</sub>).
- The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.

### Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0-15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

### Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V<sub>IL</sub>. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V<sub>IH</sub>. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 13 for the timing diagram. I<sub>CC1</sub> in the DC Characteristics table represents the active current specification for reading array data.

### Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing

sectors of memory), the system must drive WE# and CE# to  $V_{IL}$ , and OE# to  $V_{IH}$ .

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to “Word/Byte Configuration” for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “Byte/Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 2 and 3 indicate the address space that each sector occupies. The device address space is divided into two banks: Bank 1 contains the boot/parameter sectors, and Bank 2 contains the larger, code sectors of uniform size. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” is the address bits required to uniquely select a sector.

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

$I_{CC2}$  in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

### Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be sus-

pending to read from or program to another location within the same bank (except the sector being erased). Figure 19 shows how read and write cycles may be initiated for simultaneous operation with zero latency.  $I_{CC6}$  and  $I_{CC7}$  in the DC Characteristics table represent the current specifications for read-while-program and read-while-erase, respectively.

### Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at  $V_{CC} \pm 0.3$  V. (Note that this is a more restricted voltage range than  $V_{IH}$ .) If CE# and RESET# are held at  $V_{IH}$ , but not within  $V_{CC} \pm 0.3$  V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time ( $t_{CE}$ ) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

$I_{CC3}$  in the DC Characteristics table represents the standby current specification.

### Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for  $t_{ACC} + 30$  ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.  $I_{CC4}$  in the DC Characteristics table represents the automatic sleep mode current specification.