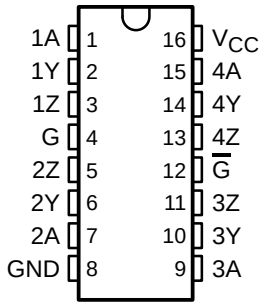
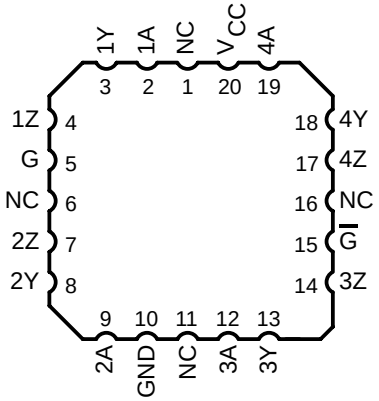
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B and ITU Recommendation V.11**
- **Operates From a Single 5-V Supply**
- **TTL Compatible**
- **Complementary Outputs**
- **High Output Impedance in Power-Off Conditions**
- **Complementary Output-Enable Inputs**

D, DB, N, NS, OR J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description/ordering information

The AM26LS31 is a quadruple complementary-output line driver designed to meet the requirements of ANSI TIA/EIA-422-B and ITU (formerly CCITT) Recommendation V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they are in the high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable (G, $\overline{G}$) input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	AM26LS31CN	AM26LS31CN
	SOIC – D	Tube	AM26LS31CD	AM26LS31C
		Tape and reel	AM26LS31CDR	
	SOP – NS	Tape and reel	AM26LS31CNSR	26LS31
	SSOP – DB	Tape and reel	AM26LS31CDBR	SA31C
–55°C to 125°C	CDIP – J	Tube	AM26LS31MJ	AM26LS31MJB
	LCCC – FK	Tube	AM26LS31MFK	AM26LS31MFKB

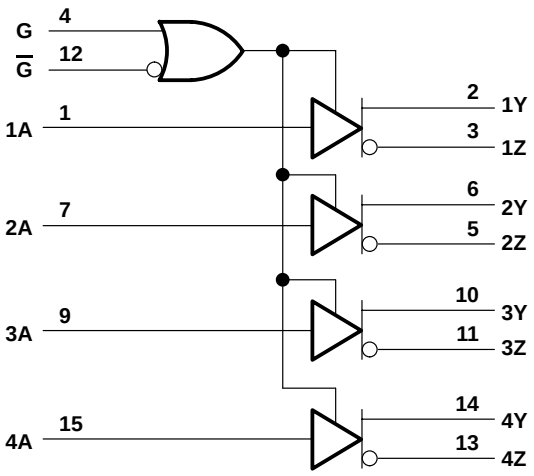
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each driver)

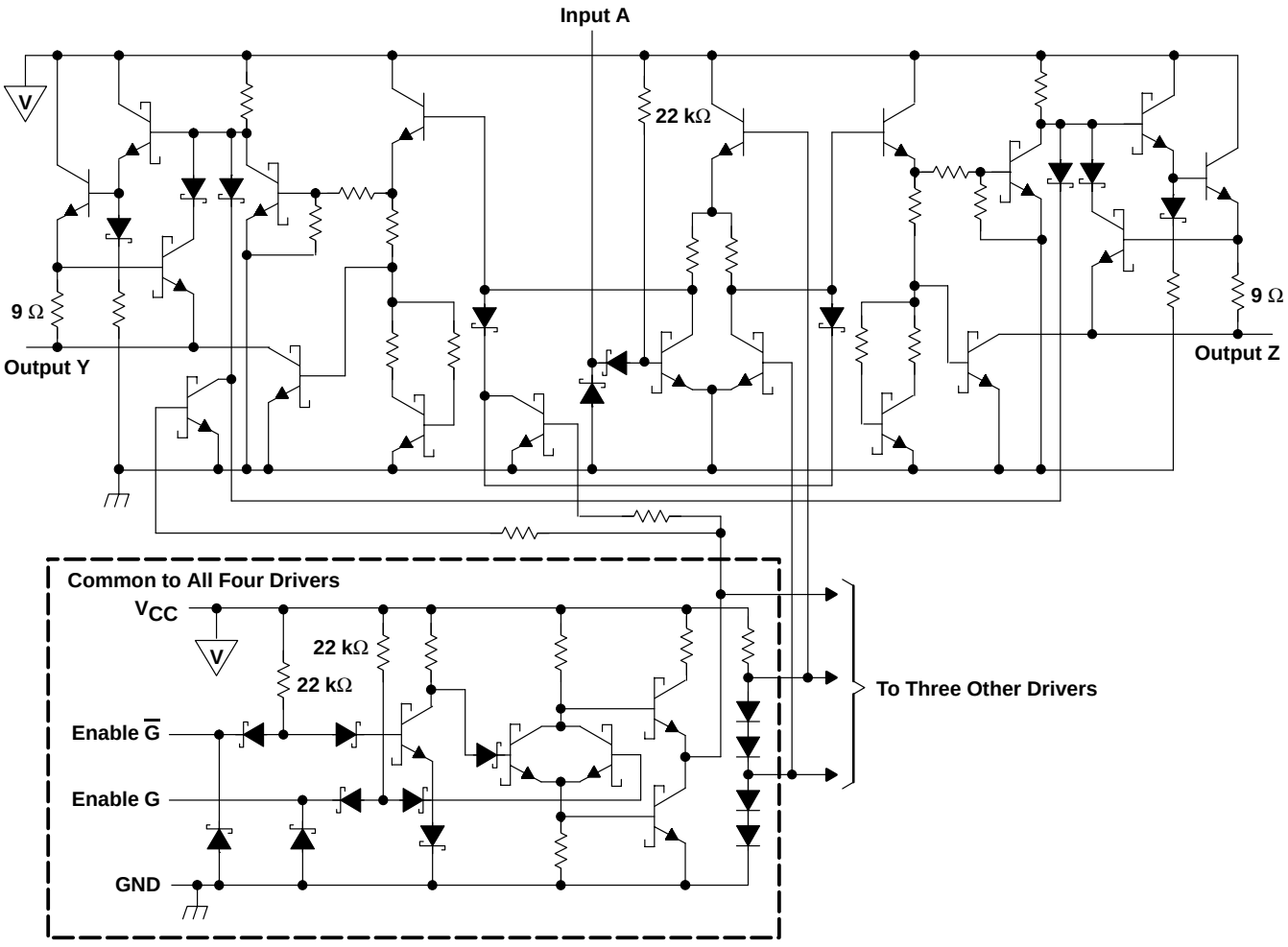
INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Output off-state voltage . . . . . 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network GND.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R\theta_{JA}$). Thermal resistances are not production tested and the values given are for informational purposes only.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	AM26LS31C	4.75	5	5.25	V
		AM26LS31M	4.5	5	5.5	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	AM26LS31C	0		70	°C
		AM26LS31M	–55		125	

electrical characteristics over operating free-air temperature range (unless otherwise noted)†

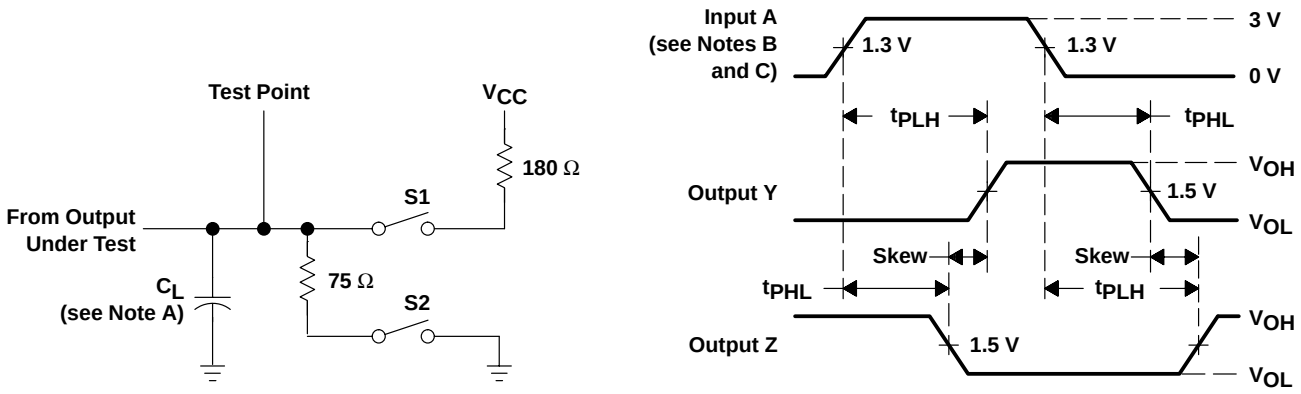
PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18 mA			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –20 mA	T_A = –55°C	2.4			V
			All other temperatures	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 20 mA			0.5	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MIN	V_O = 0.5 V			–20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			–0.36	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		–30		–150	mA
I_{CC}	Supply current	V_{CC} = MAX,	All outputs disabled		32	80	mA

† For C suffix devices, V_{CC} MIN = 4.75 V and V_{CC} MAX = 5.25 V. For M suffix devices, V_{CC} MIN = 4.5 V and V_{CC} MAX = 5.5 V.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

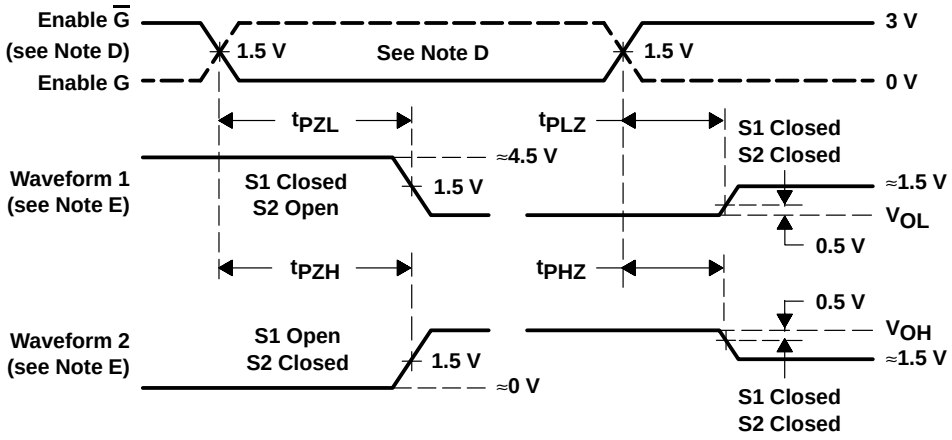
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF,	S1 and S2 open		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output				14	20	
t_{PZH}	Output enable time to high level	C_L = 30 pF	R_L = 75 Ω		25	40	ns
t_{PZL}	Output enable time to low level		R_L = 180 Ω		37	45	
t_{PHZ}	Output disable time from high level	C_L = 10 pF,	S1 and S2 closed		21	30	ns
t_{PLZ}	Output disable time from low level				23	35	
	Output-to-output skew	C_L = 30 pF,	S1 and S2 open		1	6	ns

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES AND SKEW

TEST CIRCUIT



ENABLE AND DISABLE TIME WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 15$ ns, $t_f \le 6$ ns.
C. When measuring propagation delay times and skew, switches S1 and S2 are open.
D. Each enable is tested separately.
E. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

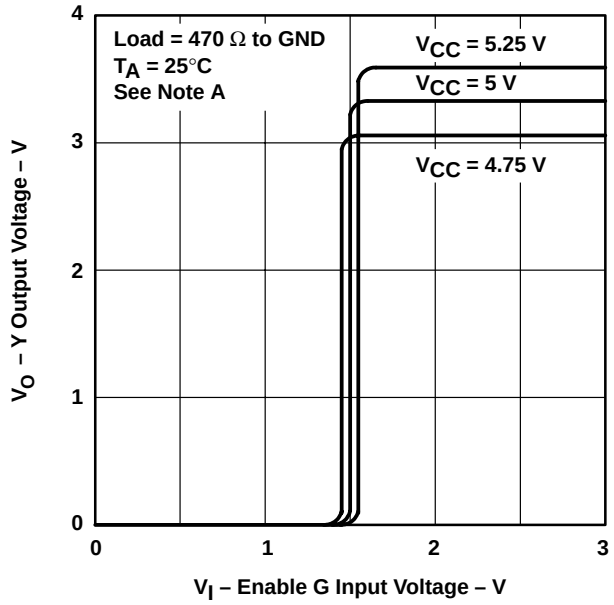


Figure 2

OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

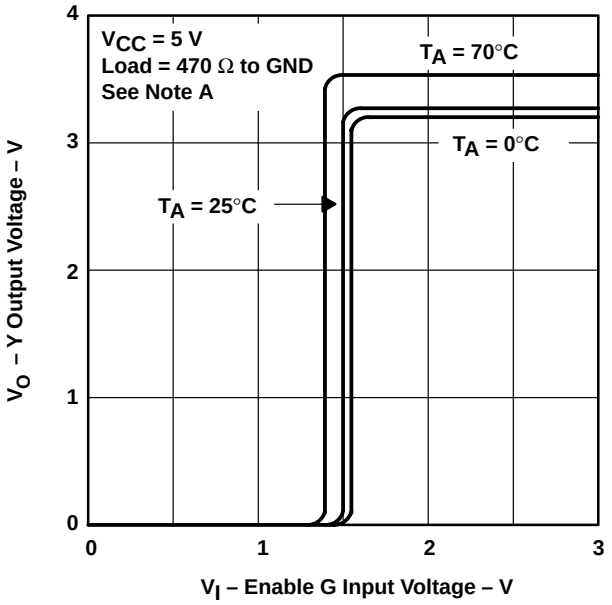


Figure 3

OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

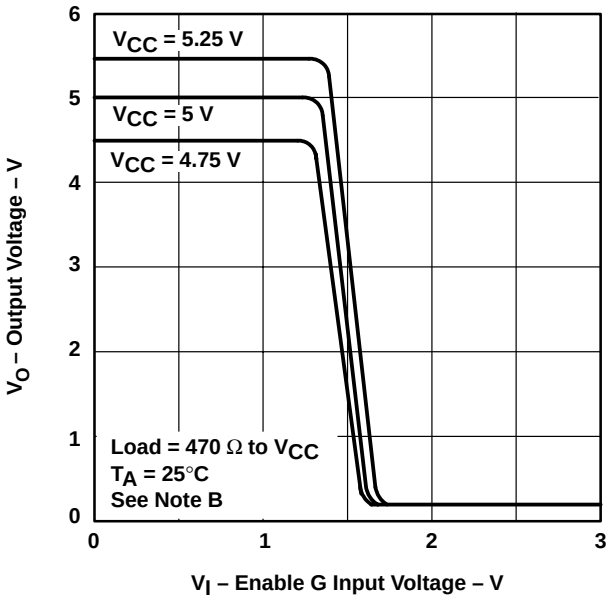


Figure 4

OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

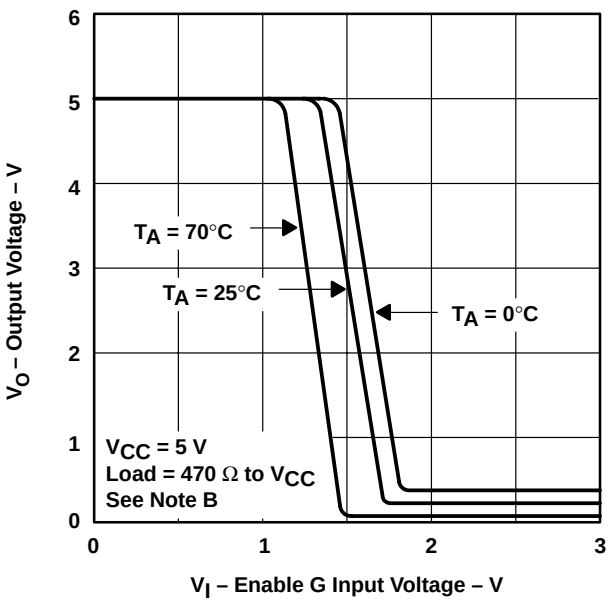


Figure 5

NOTES: A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.
B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

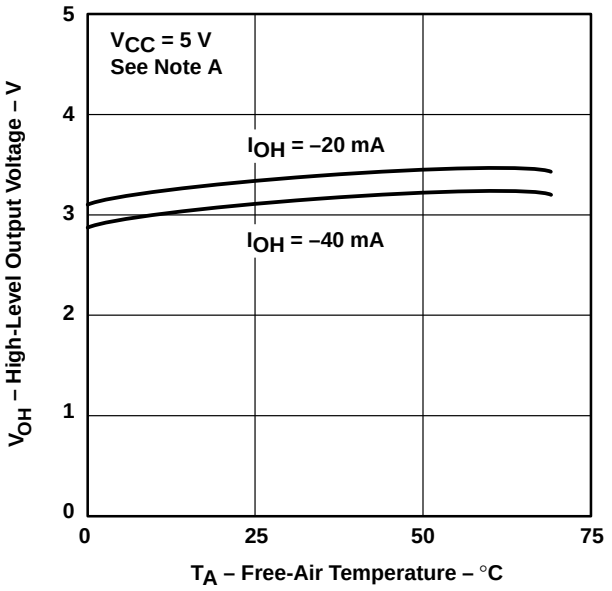


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

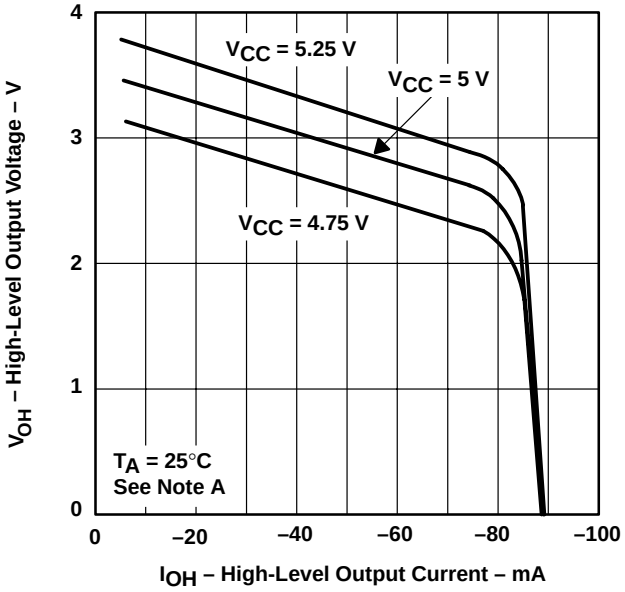


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

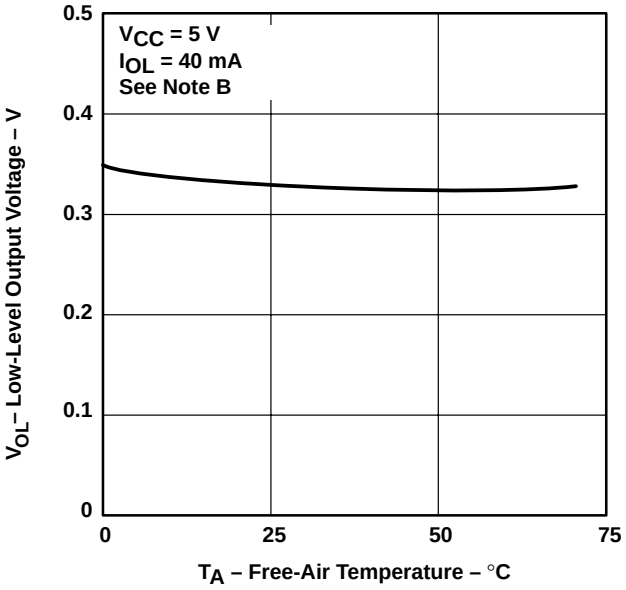


Figure 8

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

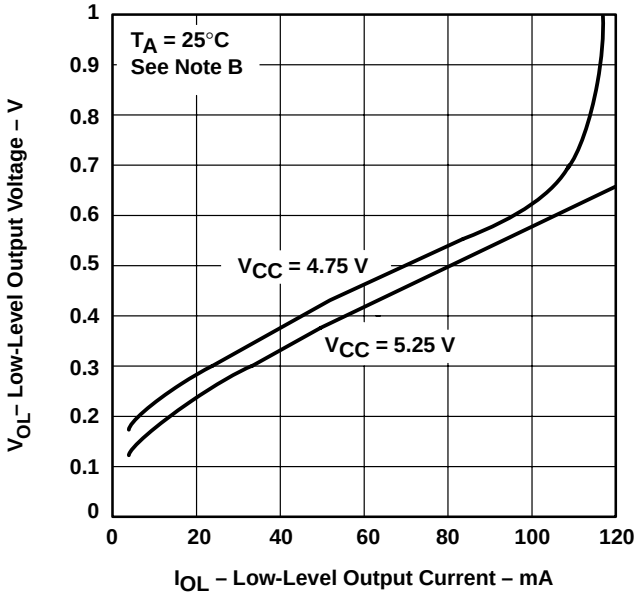


Figure 9

NOTES: A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.
B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z inputs.

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

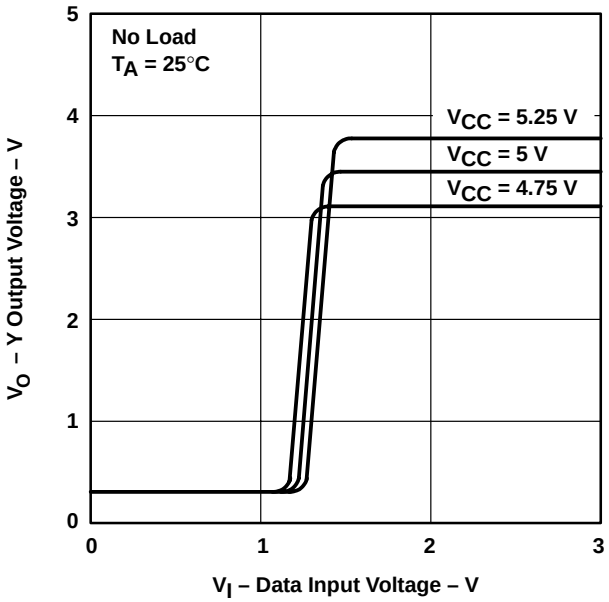


Figure 10

Y OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

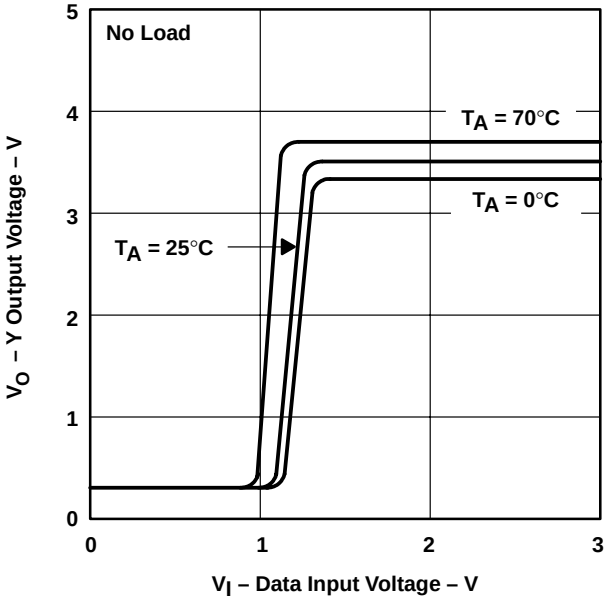


Figure 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
AM26LS31CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS31CDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS31CDBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS31CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS31CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS31CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS31CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
AM26LS31CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS31CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

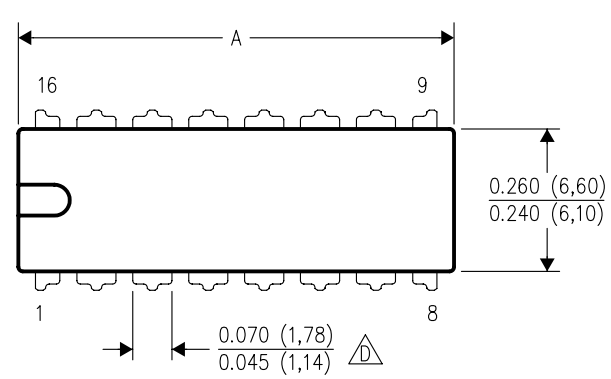
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

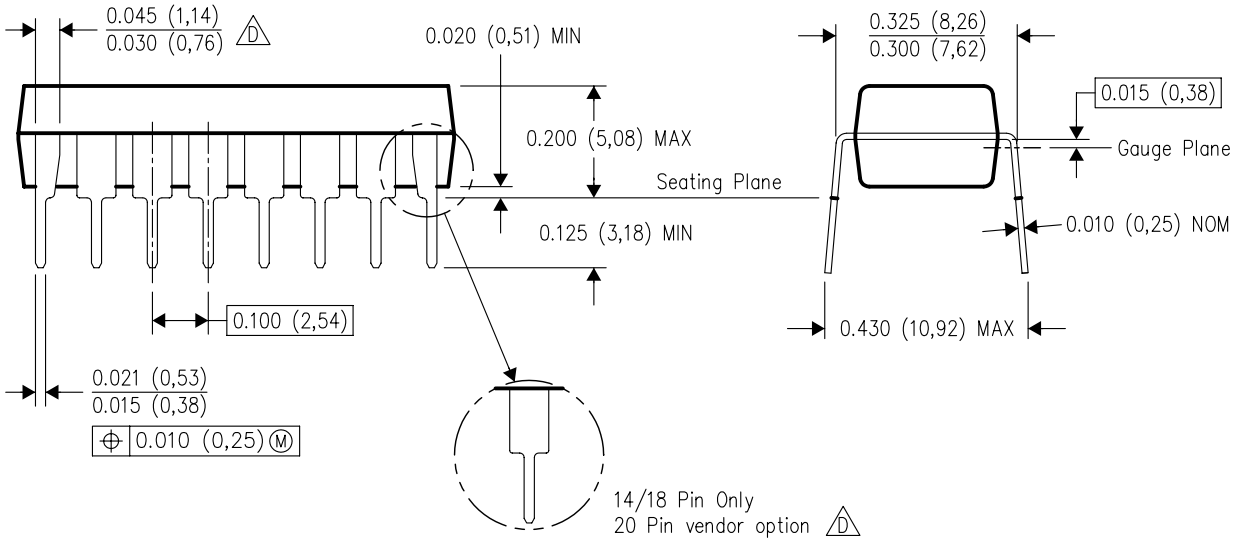
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



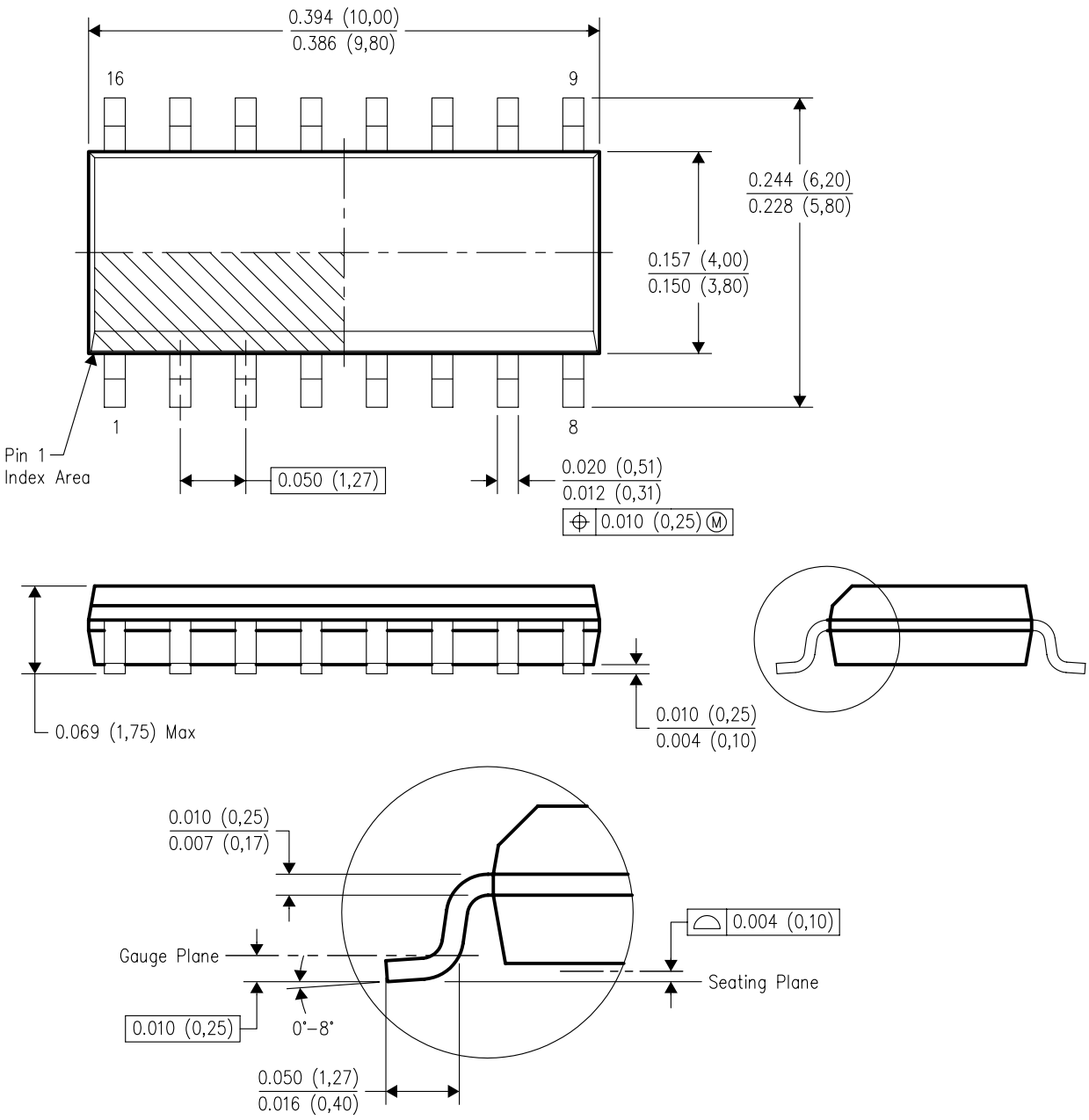
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

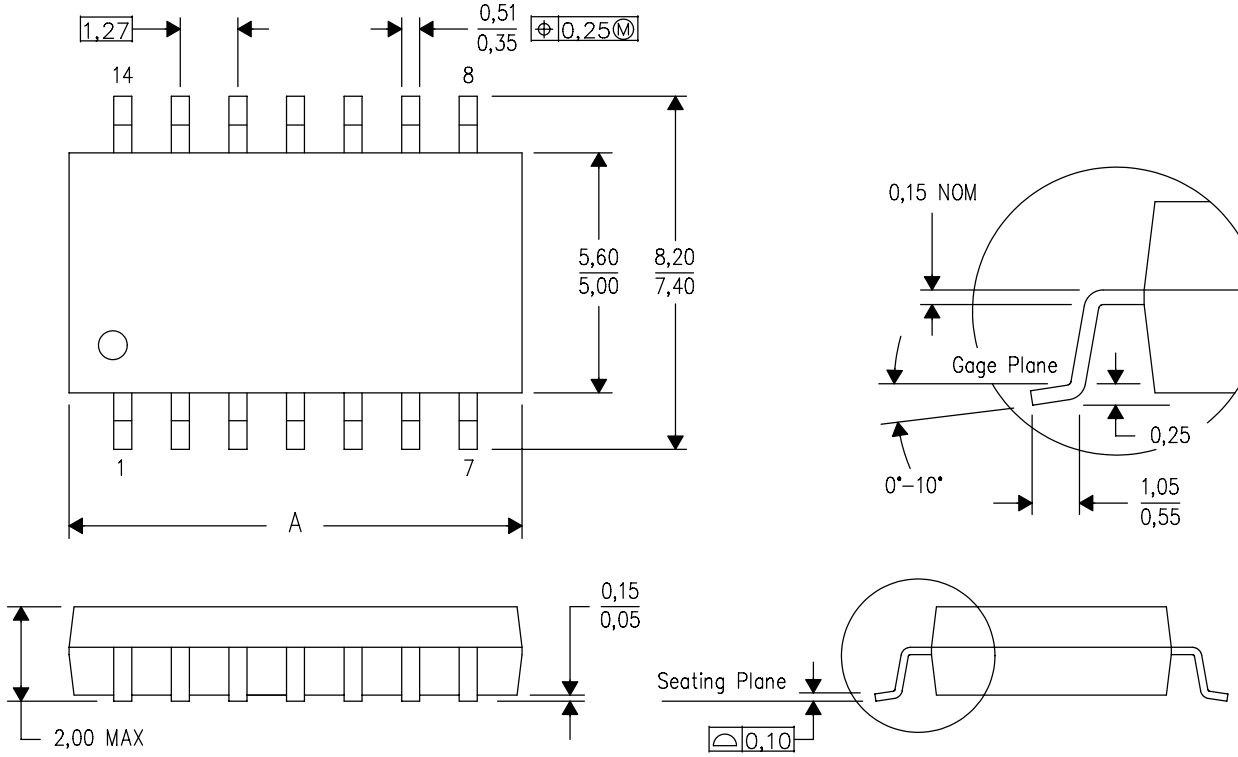


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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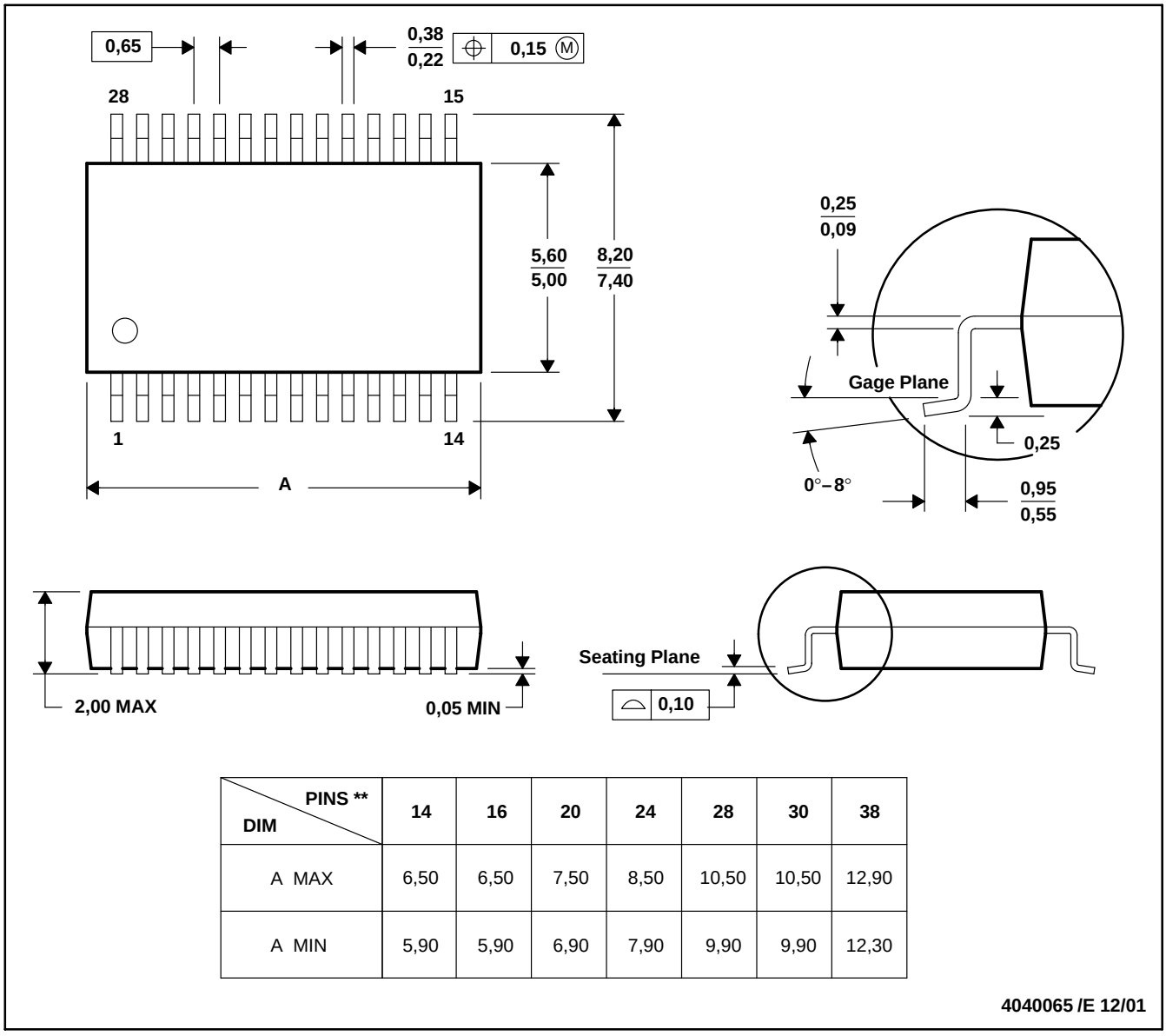
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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