



16-BIT 250-KSPS SERIAL CMOS SAMPLING ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 250-kHz Sampling Rate
- 4-V, 5-V, 10 V, ± 3.33 -V, ± 5 -V, and ± 10 -V Input Ranges
- ± 2.0 LSB Max INL
- ± 1 LSB Max DNL, 16-Bit No Missing Codes
- SPI Compatible Serial Output with Daisy-Chain (TAG) Feature
- Single 5-V Supply
- Pin-Compatible With ADS7809 (Low Speed) and 12-Bit ADS8508/7808
- Uses Internal or External Reference
- 70-mW Typ Power Dissipation at 250 KSPS
- 20-Pin SO and 28-Pin SSOP Packages
- Simple DSP Interface

APPLICATIONS

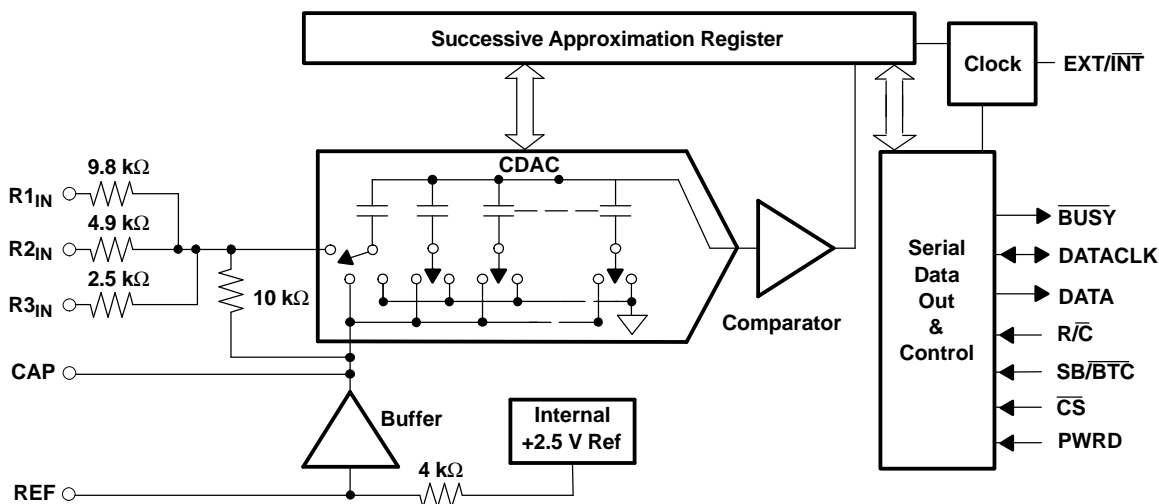
- Industrial Process Control
- Data Acquisition Systems
- Digital Signal Processing
- Medical Equipment
- Instrumentation

DESCRIPTION

The ADS8509 is a complete 16-bit sampling analog-to-digital (A/D) converter using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, successive approximation register (SAR) A/D converter with sample-and-hold, reference, clock, and a serial data interface. Data can be output using the internal clock or can be synchronized to an external data clock. The ADS8509 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS8509 is specified at a 250-kHz sampling rate over the full temperature range. Precision resistors provide various input ranges including ± 10 V and 0 V to 5 V, while the innovative design allows operation from a single +5-V supply with power dissipation under 100 mW.

The ADS8509 is available in 20-pin SO and 28-pin SSOP packages, both fully specified for operation over the industrial -40°C to 85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGE/ORDERING INFORMATION⁽¹⁾

| PRODUCT | MINIMUM RELATIVE ACCURACY (LSB) | NO MISSING CODE | MINIMUM SINAD (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE LEAD | PACKAGE DESIGNATOR | ORDERING NUMBER | TRANSPORT MEDIA, QTY |
|-----------|---------------------------------|-----------------|--------------------|---------------------------------|--------------|--------------------|-----------------|----------------------|
| ADS8509IB | ±2 | 16 | 85 | -40°C to 85°C | SO-20 | DW | ADS8509IBDW | Tube, 25 |
| | | | | | | | ADS8509IBDWR | Tape and Reel, 2000 |
| | | | | | SSOP-28 | DB | ADS8509IBDB | Tube, 50 |
| | | | | | | | ADS8509IBDBR | Tape and Reel, 2000 |
| ADS8509I | ±3 | 15 | 83 | -40°C to 85°C | SO-20 | DW | ADS8509IDW | Tube, 25 |
| | | | | | | | ADS8509IDWR | Tape and Reel, 2000 |
| | | | | | SSOP-28 | DB | ADS8509IDB | Tube, 50 |
| | | | | | | | ADS8509IDBR | Tape and Reel, 2000 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | UNIT |
|---|--------------------------------------|--|
| Analog inputs | R1 _{IN} | ±25 V |
| | R2 _{IN} | ±25 V |
| | R3 _{IN} | ±25 V |
| | REF | +V _{ANA} + 0.3 V to AGND2 - 0.3 V |
| Ground voltage differences | DGND, AGND2 | ±0.3 V |
| | V _{ANA} | 6 V |
| | V _{DIG} to V _{ANA} | 0.3 V |
| | V _{DIG} | 6 V |
| Digital inputs | | -0.3 V to +V _{DIG} + 0.3 V |
| Maximum junction temperature | | 165°C |
| Storage temperature range | | -65°C to 150°C |
| Internal power dissipation | | 700 mW |
| Lead temperature (soldering, 1.6 mm from case 10 seconds) | | 260°C |

(1) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

At $T_A = -40^\circ\text{C}$ to 85°C , $f_s = 250\text{ kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = 5\text{ V}$, using internal reference and 0.1%, 0.25 W fixed resistors (See Figure 29 and Figure 30) (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | ADS8509I | | | ADS8509IB | | | UNIT | |
|------------------------------------|---|--|------|-----|-----------|-----|-----|--------------------|----|
| | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| Resolution | | | | 16 | | | 16 | Bits | |
| ANALOG INPUT | | | | | | | | | |
| Voltage ranges ⁽¹⁾ | | | | | | | | | |
| Impedance ⁽¹⁾ | | | | | | | | | |
| Capacitance | | | 50 | | | 50 | | pF | |
| THROUGHPUT SPEED | | | | | | | | | |
| Conversion cycle | Acquire and convert | | | 4 | | | 4 | μs | |
| Throughput rate | | 250 | | | 250 | | | kHz | |
| DC ACCURACY | | | | | | | | | |
| INL | Integral linearity error | | -3 | 3 | -2 | | 2 | LSB ⁽²⁾ | |
| DNL | Differential linearity error | | -2 | 2 | -1 | | 1 | LSB | |
| | No missing codes | | 15 | | 16 | | | Bits | |
| | Transition noise ⁽³⁾ | | 1 | | 1 | | | LSB | |
| Full-scale error ⁽⁴⁾⁽⁵⁾ | ±10 V range | Int. Ref. with 0.1% external fixed resistors | -0.5 | 0.5 | -0.5 | | 0.5 | %FSR | |
| | All other ranges | | -0.5 | 0.5 | -0.5 | 0.5 | | | |
| | Full-scale error drift | Int. Ref. | ±7 | | ±7 | | | ppm/°C | |
| Full-scale error ⁽⁴⁾⁽⁵⁾ | ±10 V range | Ext. Ref. with 0.1% external fixed resistors | -0.5 | 0.5 | -0.5 | | 0.5 | %FSR | |
| | All other ranges | | -0.5 | 0.5 | -0.5 | 0.5 | | | |
| | Full-scale error drift | Ext. Ref. | ±2 | | ±2 | | | ppm/°C | |
| | Bipolar zero error ⁽⁴⁾ | | -10 | 10 | -5 | | 5 | mV | |
| | Bipolar zero error drift | | ±0.4 | | ±0.4 | | | ppm/°C | |
| Unipolar zero error ⁽⁴⁾ | 10 V range | | -5 | 5 | -5 | | 5 | mV | |
| | 4 V and 5 V range | | -3 | 3 | -3 | | 3 | | |
| | Unipolar zero error drift | | ±2 | | ±2 | | | ppm/°C | |
| | Recovery to rated accuracy after power down | 1-μF Capacitor to CAP | 1 | | 1 | | | ms | |
| | Power supply sensitivity ($V_{\text{DIG}} = V_{\text{ANA}} = V_{\text{D}}$) | +4.75 V < V_{D} < +5.25 V | -8 | 8 | -8 | | 8 | LSB | |
| AC ACCURACY | | | | | | | | | |
| SFDR | Spurious-free dynamic range | $f_1 = 20\text{ kHz}$ | 90 | 99 | | 95 | 99 | dB ⁽⁶⁾ | |
| THD | Total harmonic distortion | $f_1 = 20\text{ kHz}$ | | -98 | -90 | | -98 | -93 | dB |
| SINAD | Signal-to-(noise+distortion) | $f_1 = 20\text{ kHz}$ | 83 | 88 | | 85 | 88 | dB | |
| | | -60-dB Input | | 30 | | 32 | | dB | |
| SNR | Signal-to-noise ratio | $f_1 = 20\text{ kHz}$ | 83 | 88 | | 86 | 88 | dB | |
| | Full-power bandwidth ⁽⁷⁾ | | 500 | | 500 | | | kHz | |
| SAMPLING DYNAMICS | | | | | | | | | |
| | Aperture delay | | 5 | | 5 | | | ns | |
| | Transient response | FS Step | | | 2 | | 2 | μs | |
| | Overvoltage recovery ⁽⁸⁾ | | 150 | | 150 | | | ns | |

(1) ±10 V, 0 V to 5 V, etc. (see Table 3)

(2) LSB means least significant bit. For the ±10-V input range, one LSB is 305 μV.

(3) Typical rms noise at worst case transitions and temperatures.

(4) As measured with fixed resistors shown in Figure 29 and Figure 30. Adjustable to zero with external potentiometer. Factory calibrated with 0.1%, 0.25 W resistors.

(5) For bipolar input ranges, full-scale error is the worst case of -full-scale or +full-scale uncalibrated deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full-scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.

(6) All specifications in dB are referred to a full-scale ±10-V input.

(7) Full-power bandwidth is defined as the full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB.

(8) Recovers to specified performance after 2 x FS input overvoltage.

ELECTRICAL CHARACTERISTICS (continued)

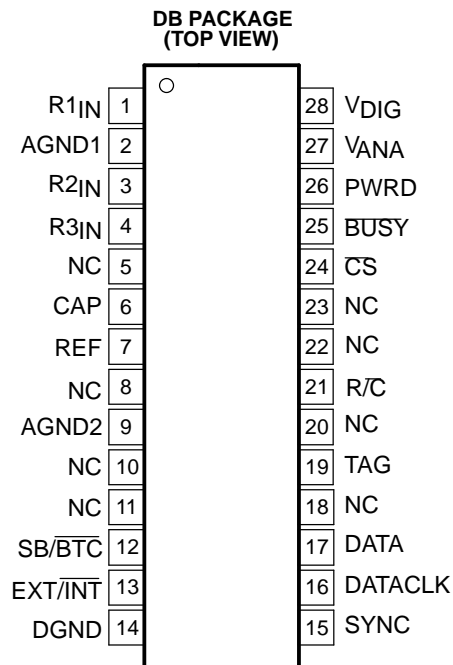
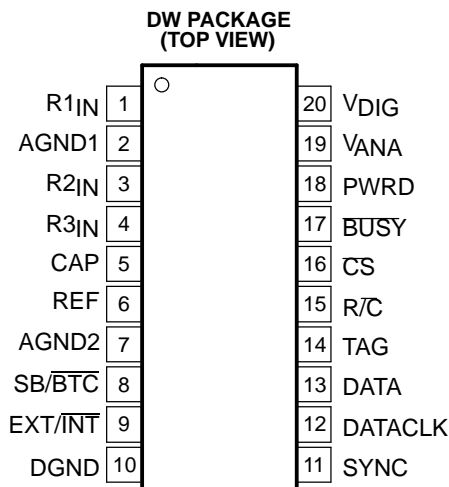
At $T_A = -40^{\circ}\text{C}$ to 85°C , $f_s = 250\text{ kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = 5\text{ V}$, using internal reference and 0.1%, 0.25 W fixed resistors (See Figure 29 and Figure 30) (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | ADS8509I | | | ADS8509IB | | | UNIT |
|--|---|--|-----|---------------------------------|-----------|-----|---------------------------------|-------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| REFERENCE | | | | | | | | |
| Internal reference voltage | No load | 2.48 | 2.5 | 2.52 | 2.48 | 2.5 | 2.52 | V |
| Internal reference source current (must use external buffer) | | 1 | | | 1 | | | μA |
| Internal reference drift | | 8 | | | 8 | | | ppm/ $^{\circ}\text{C}$ |
| External reference voltage range for specified linearity | | 2.3 | 2.5 | 2.7 | 2.3 | 2.5 | 2.7 | V |
| External reference current drain | Ext. 2.5-V Ref. | 100 | | | 100 | | | μA |
| DIGITAL INPUTS | | | | | | | | |
| Logic levels | | | | | | | | |
| V_{IL} | Low-level input voltage | -0.3 | | 0.8 | -0.3 | | 0.8 | V |
| V_{IH} | High-level input voltage | 2.0 | | $V_{\text{DIG}} + 0.3\text{ V}$ | 2.0 | | $V_{\text{DIG}} + 0.3\text{ V}$ | V |
| I_{IL} | Low-level input current | $V_{\text{IL}} = 0\text{ V}$ | | ± 10 | | | ± 10 | μA |
| I_{IH} | High-level input current | $V_{\text{IH}} = 5\text{ V}$ | | ± 10 | | | ± 10 | μA |
| DIGITAL OUTPUTS | | | | | | | | |
| Data format (Serial 16-bits) | | | | | | | | |
| Data coding (Binary 2's complement or straight binary) | | | | | | | | |
| Pipeline delay (Conversion results only available after completed conversion.) | | | | | | | | |
| Data clock (Selectable for internal or external data clock) | | | | | | | | |
| Internal clock (output only when transmitting data) | EXT/INT Low | 9 | | | 9 | | | MHz |
| External clock (can run continually but not recommended for optimum performance) | EXT/INT High | 0.1 | | 26 | 0.1 | | 26 | MHz |
| V_{OL} | Low-level output voltage | $I_{\text{SINK}} = 1.6\text{ mA}$ | | 0.4 | | | 0.4 | V |
| V_{OH} | High-level output voltage | $I_{\text{SOURCE}} = 500\text{ }\mu\text{A}$ | | 4 | | | 4 | V |
| Leakage current | Hi-Z state, $V_{\text{OUT}} = 0\text{ V}$ to V_{DIG} | ± 5 | | | ± 5 | | | μA |
| Output capacitance | Hi-Z state | 15 | | | 15 | | | pF |
| POWER SUPPLIES | | | | | | | | |
| V_{DIG} | Digital input voltage | 4.75 | 5 | 5.25 | 4.75 | 5 | 5.25 | V |
| V_{ANA} | Analog input voltage | 4.75 | 5 | 5.25 | 4.75 | 5 | 5.25 | V |
| I_{DIG} | Digital input current | 4 | | | 4 | | | mA |
| I_{ANA} | Analog input current | 10 | | | 10 | | | mA |
| POWER DISSIPATION | | | | | | | | |
| PWRD Low | $f_s = 250\text{ kHz}$ | 70 | | 100 | 70 | | 100 | mW |
| PWRD High | | 50 | | | 50 | | | μW |
| TEMPERATURE RANGE | | | | | | | | |
| Specified performance | | -40 | | 85 | -40 | | 85 | $^{\circ}\text{C}$ |
| Derated performance ⁽⁹⁾ | | -55 | | 125 | -55 | | 125 | $^{\circ}\text{C}$ |
| Storage | | -65 | | 150 | -65 | | 150 | $^{\circ}\text{C}$ |
| THERMAL RESISTANCE (θ_{JA}) | | | | | | | | |
| SSOP | | 62 | | | 62 | | | $^{\circ}\text{C/W}$ |
| SO | | 46 | | | 46 | | | $^{\circ}\text{C/W}$ |

(9) The internal reference may not be started correctly beyond the industrial temperature range (-40°C to 85°C), therefore use of an external reference is recommended.

TIMING REQUIREMENTS, $T_A = -40^{\circ}\text{C}$ to 85°C

| PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------------------------|--|-----|--------------|-----|---------------|
| t_{w1} | Pulse duration, convert | 40 | | | ns |
| t_{d1} | Delay time, $\overline{\text{BUSY}}$ from $\overline{\text{R/C}}$ low | | 6 | 20 | ns |
| t_{w2} | Pulse duration, $\overline{\text{BUSY}}$ low | | | 2.2 | μs |
| t_{d2} | Delay time, $\overline{\text{BUSY}}$, after end of conversion | | 5 | | ns |
| t_{d3} | Delay time, aperture | | 5 | | ns |
| t_{conv} | Conversion time | | | 2.2 | μs |
| t_{acq} | Acquisition time | 1.8 | | | μs |
| $t_{\text{conv}} + t_{\text{acq}}$ | Cycle time | | | 4 | μs |
| t_{d4} | Delay time, $\overline{\text{R/C}}$ Low to internal DATACLK output | | 270 | | ns |
| t_{c1} | Cycle time, internal DATACLK | | 110 | | ns |
| t_{d5} | Delay time, data valid to internal DATACLK high | 15 | 35 | | ns |
| t_{d6} | Delay time, data valid after internal DATACLK low | 20 | 35 | | ns |
| t_{c2} | Cycle time, external DATACLK | 35 | | | ns |
| t_{w3} | Pulse duration, external DATACLK high | 15 | | | ns |
| t_{w4} | Pulse duration, external DATACLK low | 15 | | | ns |
| t_{su1} | Setup time, $\overline{\text{R/C}}$ rise/fall to external DATACLK high | 15 | $t_{c2} + 5$ | | ns |
| t_{su2} | Setup time, $\overline{\text{R/C}}$ transition to $\overline{\text{CS}}$ transition | 10 | | | ns |
| t_{d7} | Delay time, SYNC, after external DATACLK high | 3 | | 35 | ns |
| t_{d8} | Delay time, data valid | 2 | | 20 | ns |
| t_{d9} | Delay time, $\overline{\text{CS}}$ to rising edge | 10 | | | ns |
| t_{d10} | Delay time, previous data available after $\overline{\text{CS}}$, $\overline{\text{R/C}}$ low | 2 | | | μs |
| t_{su3} | Setup time, $\overline{\text{BUSY}}$ transition to first external DATACLK | 5 | | | ns |
| t_{d11} | Delay time, final external DATACLK to $\overline{\text{BUSY}}$ falling edge | | | 1 | μs |
| t_{su3} | Setup time, TAG valid | 0 | | | ns |
| t_{h1} | Hold time, TAG valid | 2 | | | ns |



Terminal Functions

| TERMINAL | | | | DESCRIPTION |
|------------------|------------------------------|--------|-----|---|
| NAME | DB NO. | DW NO. | I/O | |
| AGND1 | 2 | 2 | – | Analog ground. Used internally as ground reference point. Minimal current flow. |
| AGND2 | 9 | 7 | – | Analog ground |
| BUSY | 25 | 17 | O | Busy output. Falls when a conversion is started, and remains low until the conversion is completed and the data is latched into the output shift register. |
| CAP | 6 | 5 | – | Reference buffer capacitor. 2.2- μ F Tantalum to ground. |
| \overline{CS} | 24 | 16 | – | Chip select. Internally ORed with R/\overline{C} . |
| DATA | 17 | 13 | O | Serial data output. Data is synchronized to DATACLK, with the format determined by the level of SB/BTC. In the external clock mode, after 16 bits of data, the ADS8509 outputs the level input on TAG as long as \overline{CS} is low and R/\overline{C} is high (see Figure 8 and Figure 9). If EXT/INT is low, data is valid on both the rising and falling edges of DATACLK, and between conversions DATA stays at the level of the TAG input when the conversion was started. |
| DATACLK | 16 | 12 | I/O | Either an input or an output depending on the EXT/INT level. Output data is synchronized to this clock. If EXT/INT is low, DATACLK transmits 16 pulses after each conversion, and then remains low between conversions. |
| DGND | 14 | 10 | – | Digital ground |
| EXT/INT | 13 | 9 | – | Selects external or internal clock for transmitting data. If high, data is output synchronized to the clock input on DATACLK. If low, a convert command initiates the transmission of the data from the previous conversion, along with 16-clock pulses output on DATACLK. |
| NC | 5, 8, 10, 11, 18, 20, 22, 23 | – | – | No connect |
| PWRD | 26 | 18 | I | Power down input. If high, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register. |
| R/\overline{C} | 21 | 15 | I | Read/convert input. With \overline{CS} low, a falling edge on R/\overline{C} puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/INT is low, this also initiates the transmission of the data results from the previous conversion. If EXT/INT is high, a rising edge on R/\overline{C} with \overline{CS} low, or a falling edge on \overline{CS} with R/\overline{C} high, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion. |
| REF | 7 | 6 | I/O | Reference input/output. Outputs internal 2.5-V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2- μ F tantalum capacitor. |
| R1 _{IN} | 1 | 1 | I | Analog input. See Table 3 for input range connections. |
| R2 _{IN} | 3 | 3 | I | Analog input. See Table 3 for input range connections. |
| R3 _{IN} | 4 | 4 | I | Analog input. See Table 3 for input range connections. |
| SB/BTC | 12 | 8 | O | Select straight binary or binary 2's complement data output format. If high, data is output in a straight binary format. If low, data is output in a binary 2's complement format. |
| SYNC | 15 | 11 | O | Sync output. This pin is used to supply a data synchronization pulse when the EXT level is high and at least one external clock pulse has occurred when not in the read mode. See the external clock modes descriptions. |
| TAG | 19 | 14 | I | Tag input for use in the external clock mode. If EXT is high, digital data input from TAG is output on DATA with a delay that is dependent on the external clock mode. See Figure 8 and Figure 9. |
| V _{ANA} | 27 | 19 | I | Analog supply input. Nominally +5 V. Connect directly to pin 20, and decouple to ground with 0.1- μ F ceramic and 10- μ F tantalum capacitors. |
| V _{DIG} | 28 | 20 | I | Digital supply input. Nominally +5 V. Connect directly to pin 19. Must be $\leq V_{ANA}$. |

PARAMETER MEASUREMENT INFORMATION

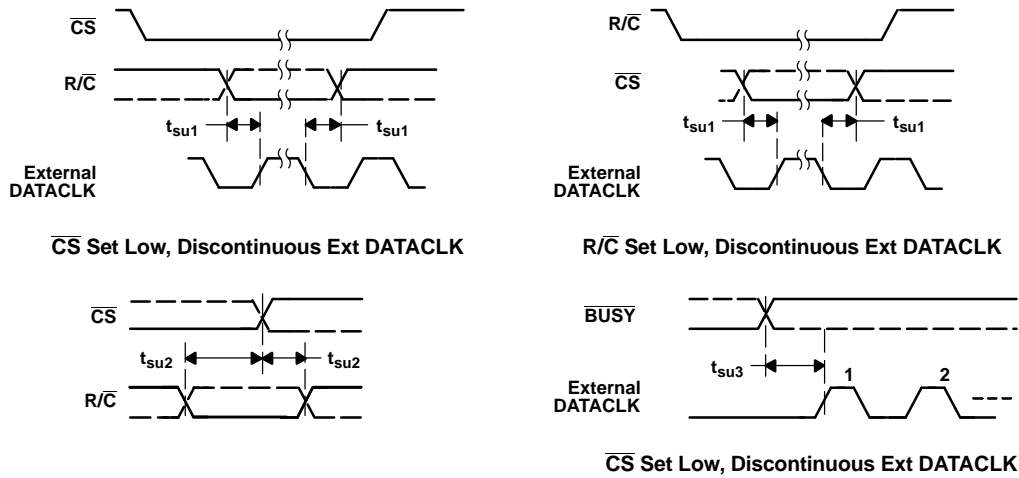


Figure 1. Critical Timing

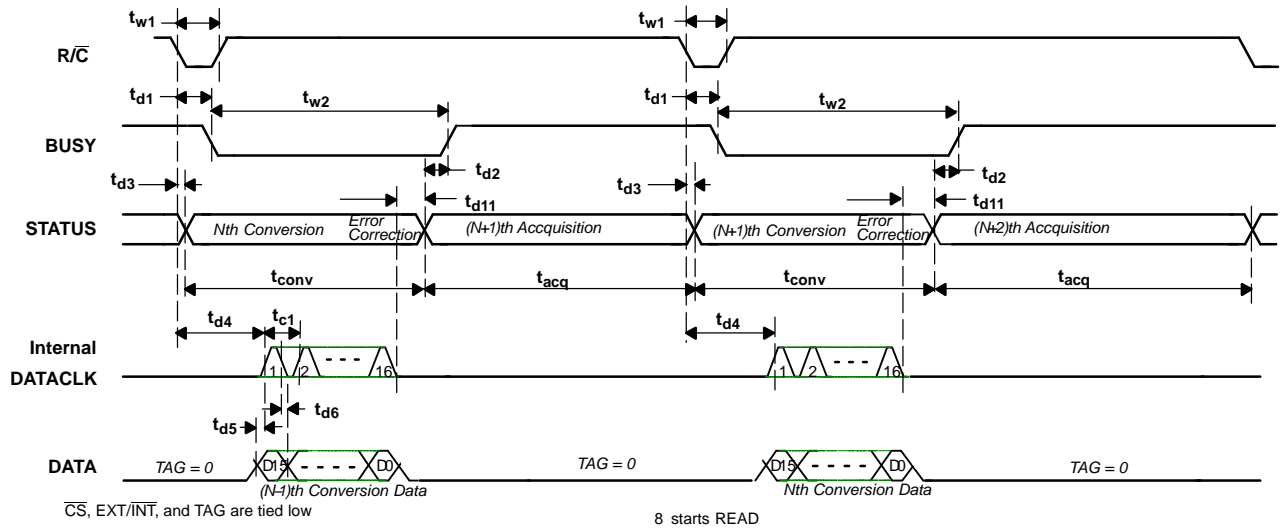


Figure 2. Basic Conversion Timing - Internal DATACLK (Read Previous Data During Conversion)

PARAMETER MEASUREMENT INFORMATION (continued)

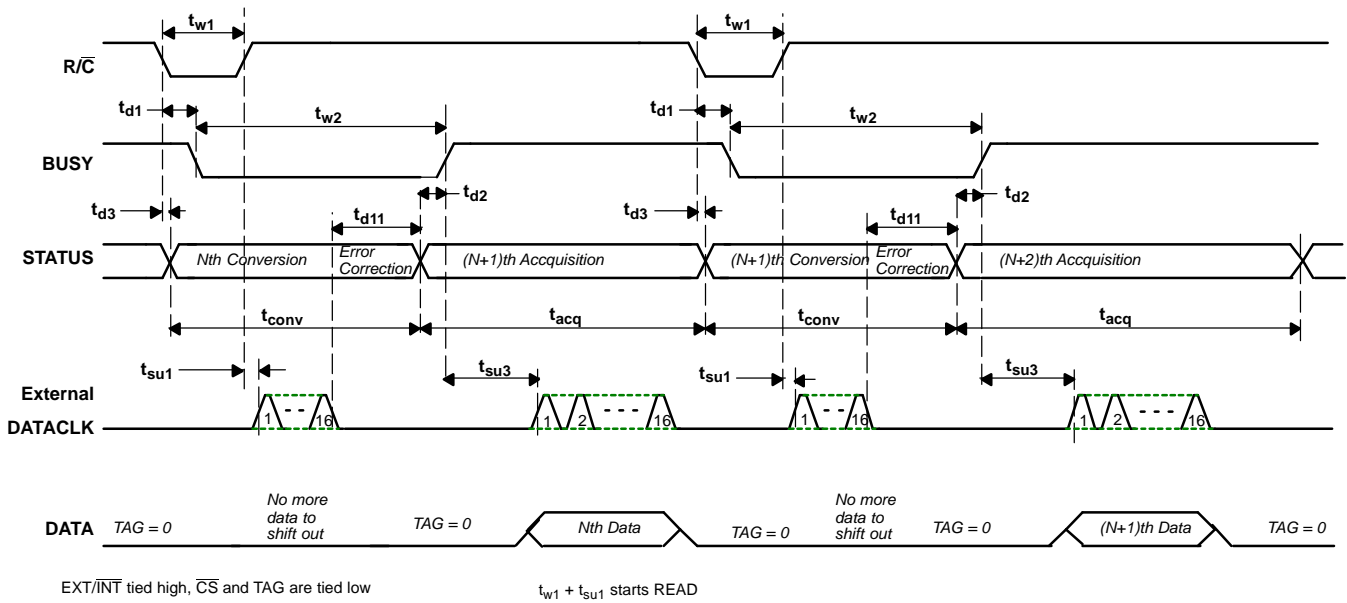


Figure 3. Basic Conversion Timing - External DATACLK

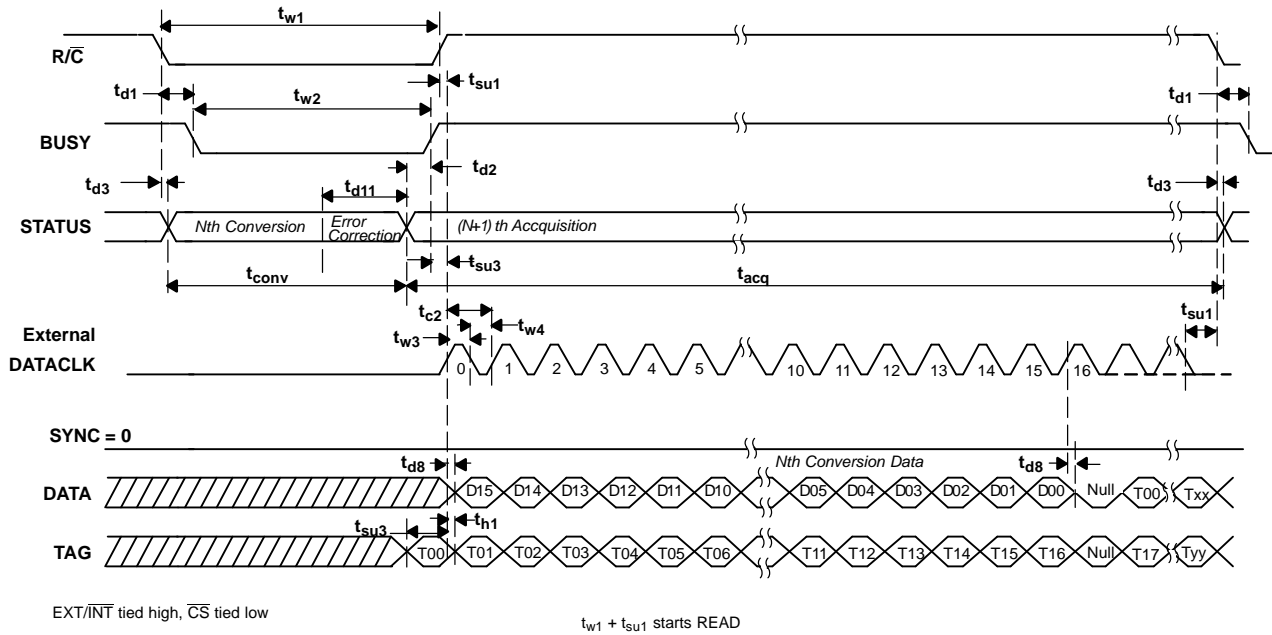


Figure 4. Read After Conversion (Discontinuous External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)

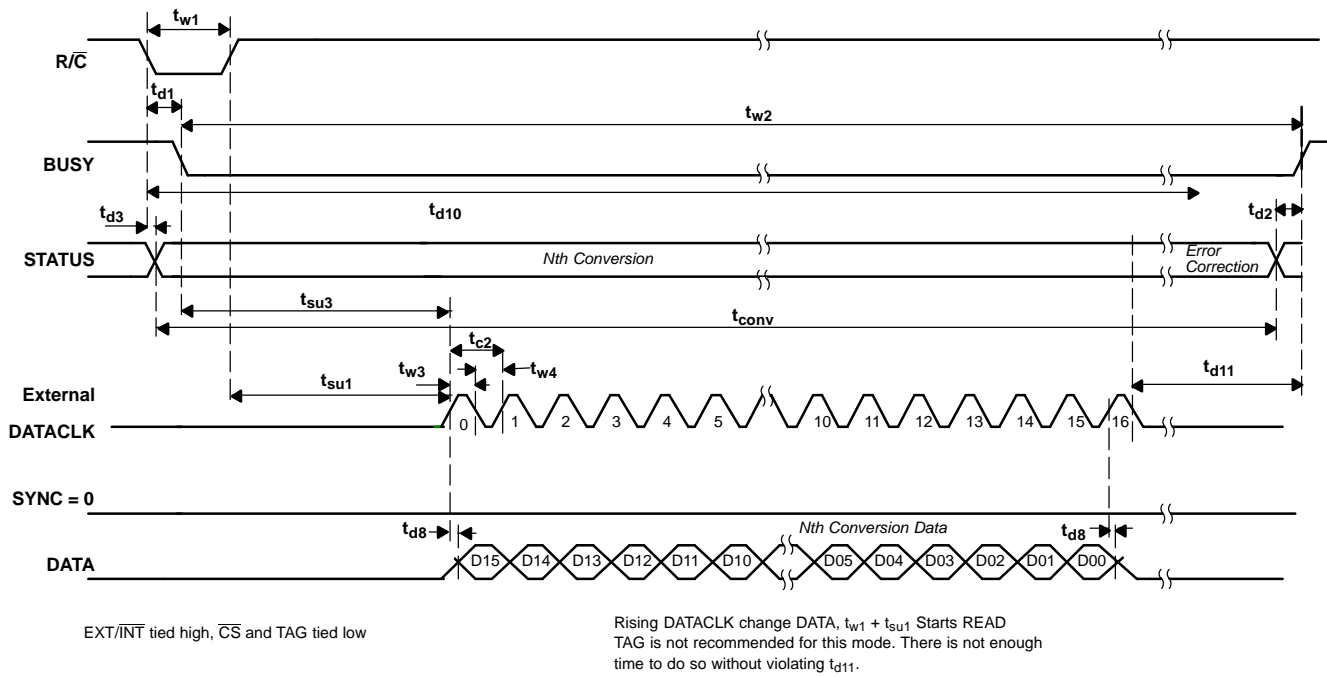


Figure 5. Read During Conversion (Discontinuous External DATACLK)

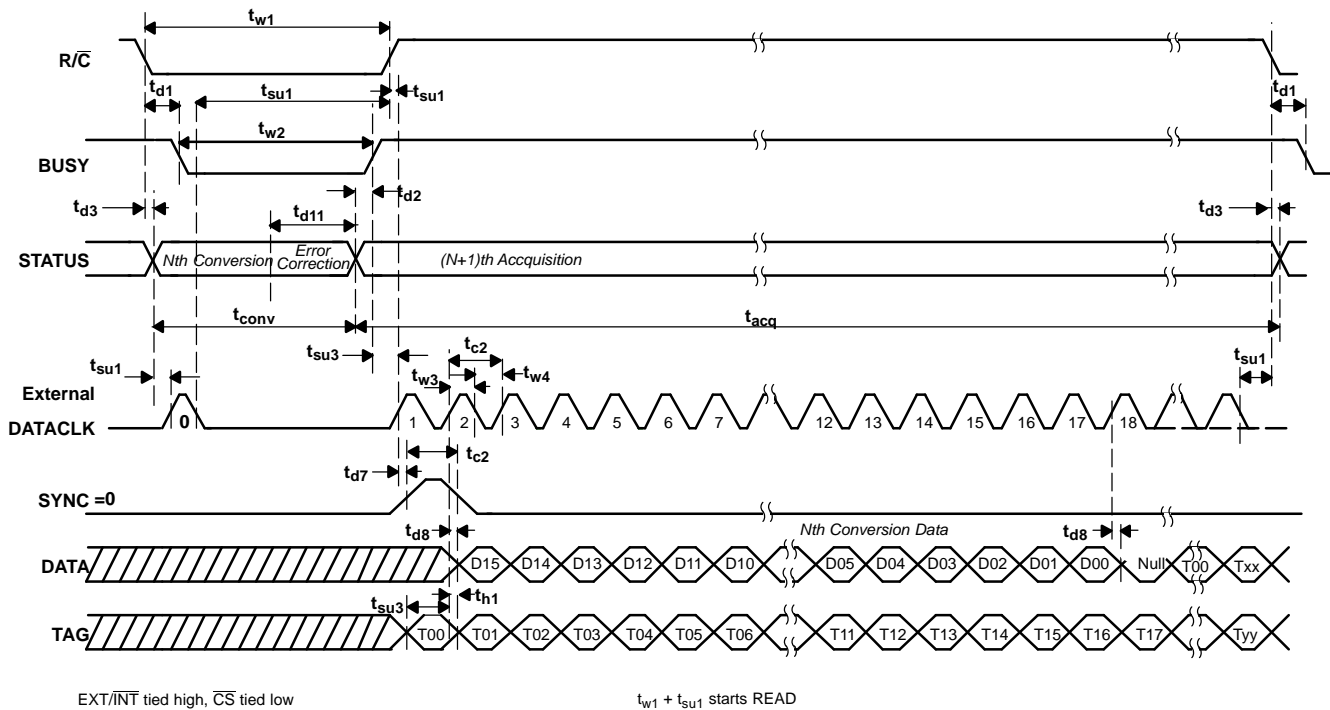
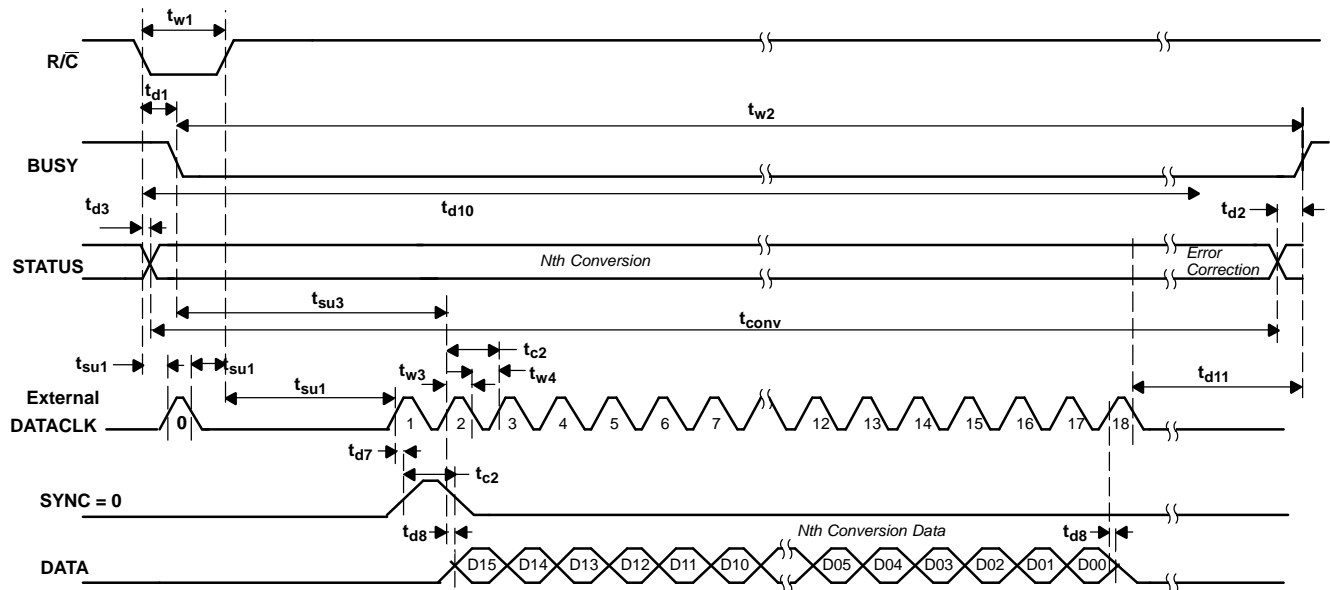


Figure 6. Read After Conversion With SYNC (Discontinuous External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)



EXT/ \overline{INT} tied high, \overline{CS} and TAG tied low

$t_{w1} + t_{su1}$ Starts READ
TAG is not recommended for this mode. There is not enough time to do so without violating t_{d11} .

Figure 7. Read During Conversion With SYNC (Discontinuous External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)

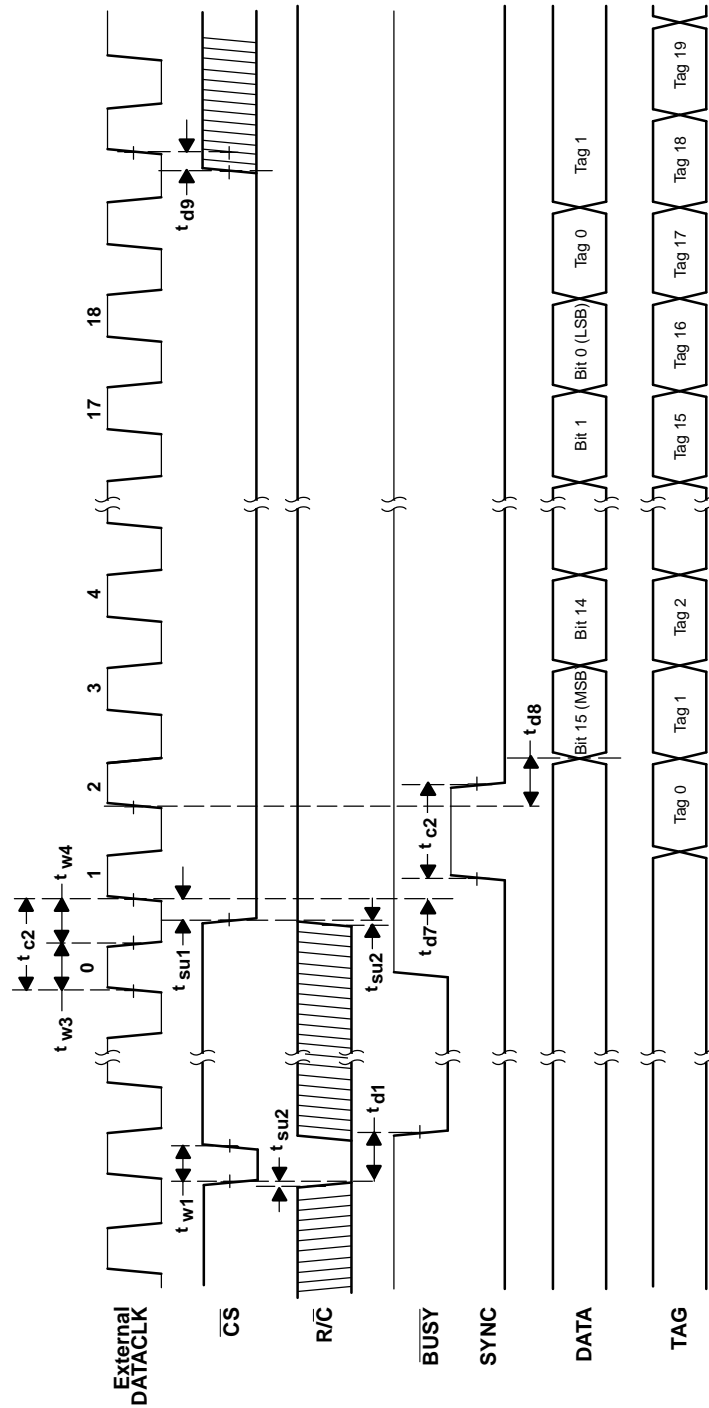


Figure 8. Conversion and Read Timing with Continuous External DATACLK (EXT/INT Tied High) Read After Conversions (Not Recommended)

PARAMETER MEASUREMENT INFORMATION (continued)

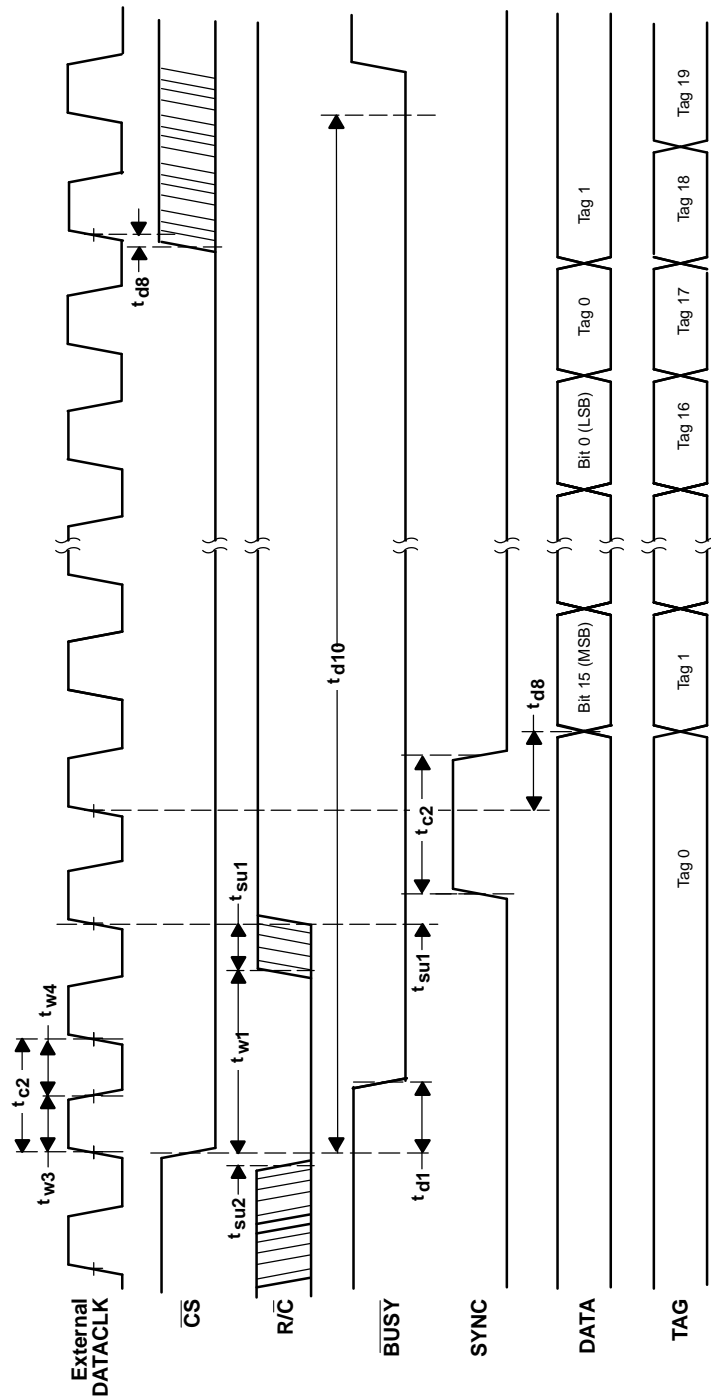


Figure 9. Conversion and Read Timing with Continuous External DATACLK (EXT/INT Tied High) Read Previous Conversion Results During Conversion (Not Recommended)

TYPICAL CHARACTERISTICS

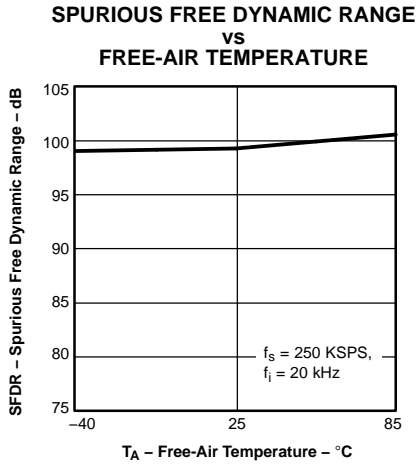


Figure 10.

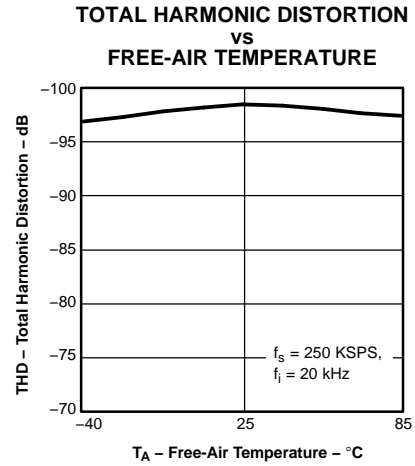


Figure 11.

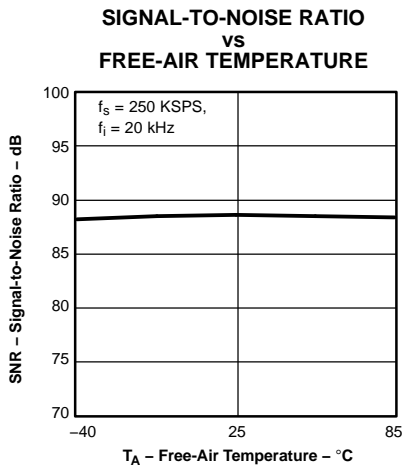


Figure 12.

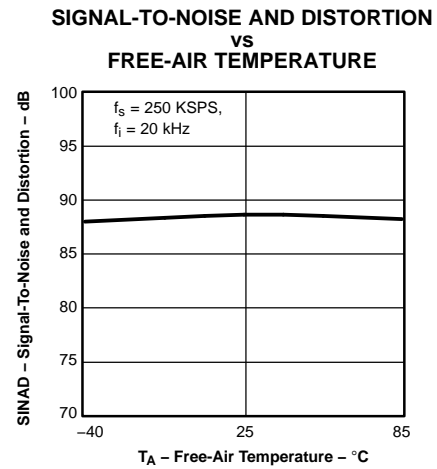


Figure 13.

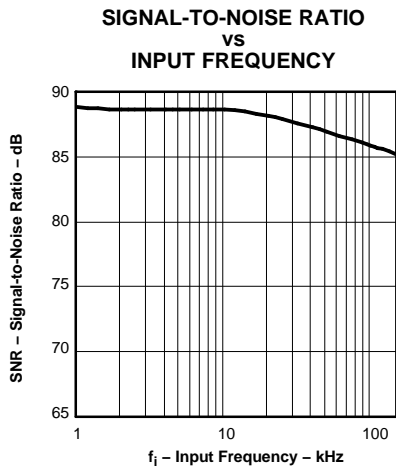


Figure 14.

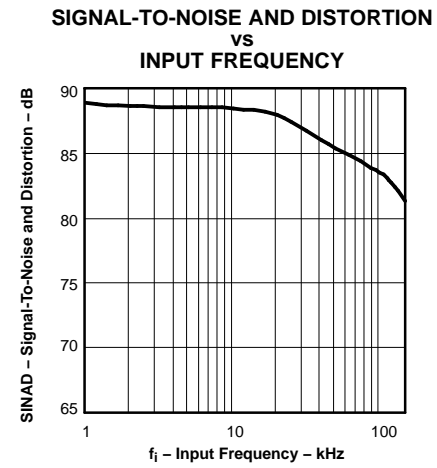


Figure 15.

TYPICAL CHARACTERISTICS (continued)

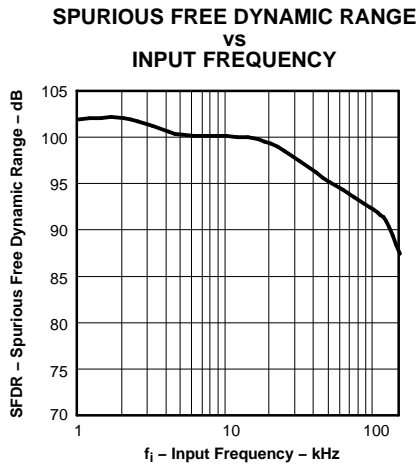


Figure 16.

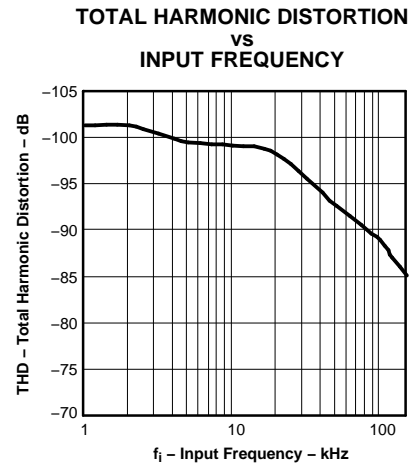


Figure 17.

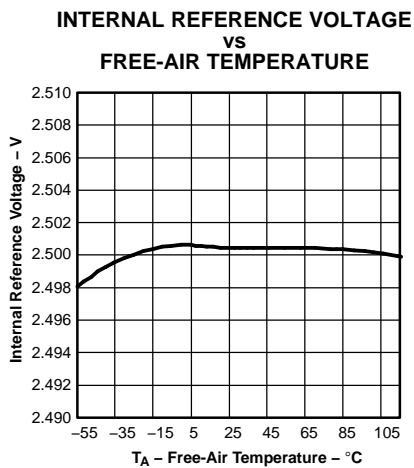


Figure 18.

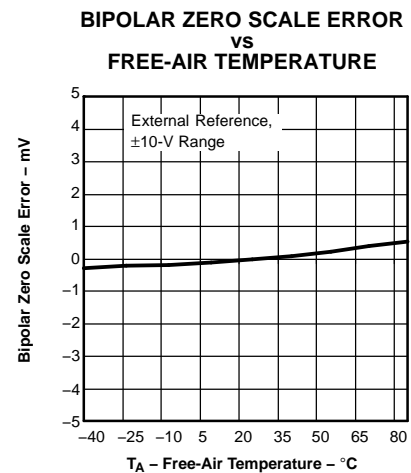


Figure 19.

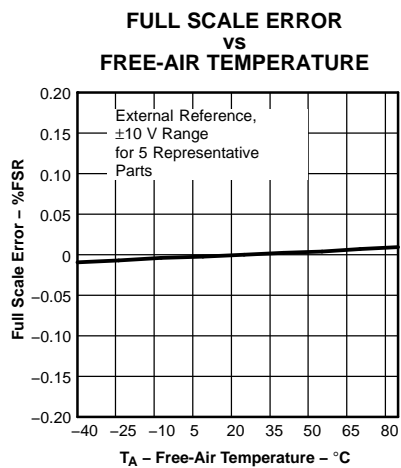


Figure 20.

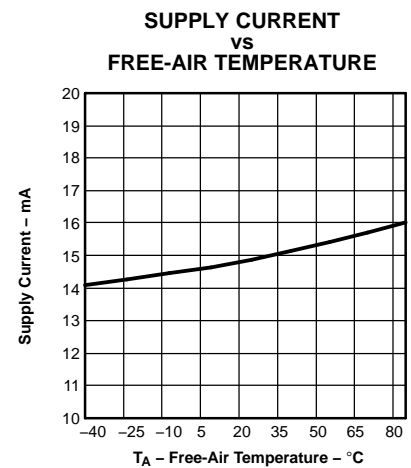


Figure 21.

TYPICAL CHARACTERISTICS (continued)

HISTOGRAM

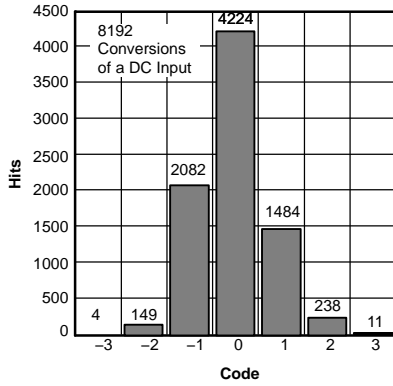


Figure 22.

PERFORMANCE VS CAP PIN CAPACITOR ESR

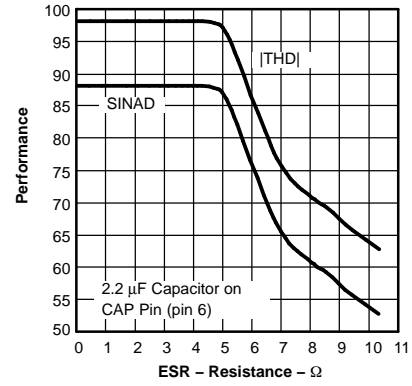


Figure 23.

INTEGRAL NONLINEARITY

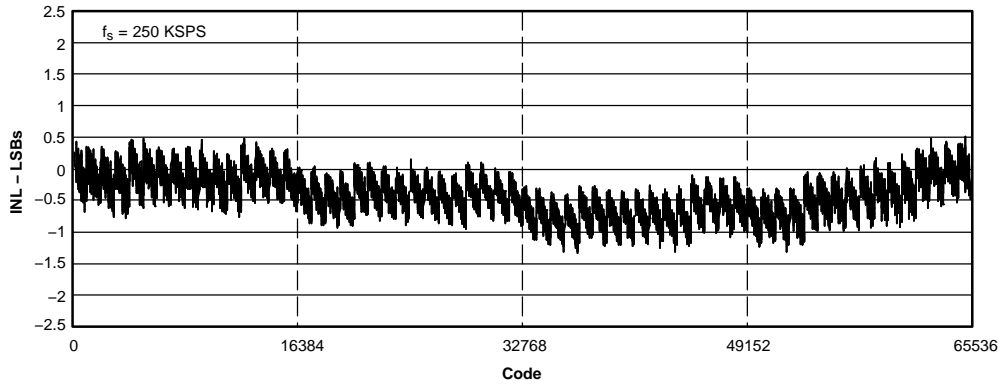


Figure 24.

DIFFERENTIAL NONLINEARITY

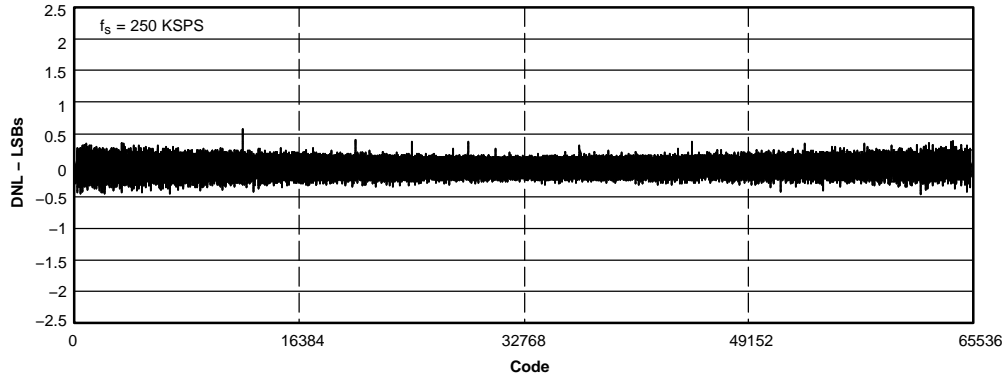


Figure 25.

TYPICAL CHARACTERISTICS (continued)

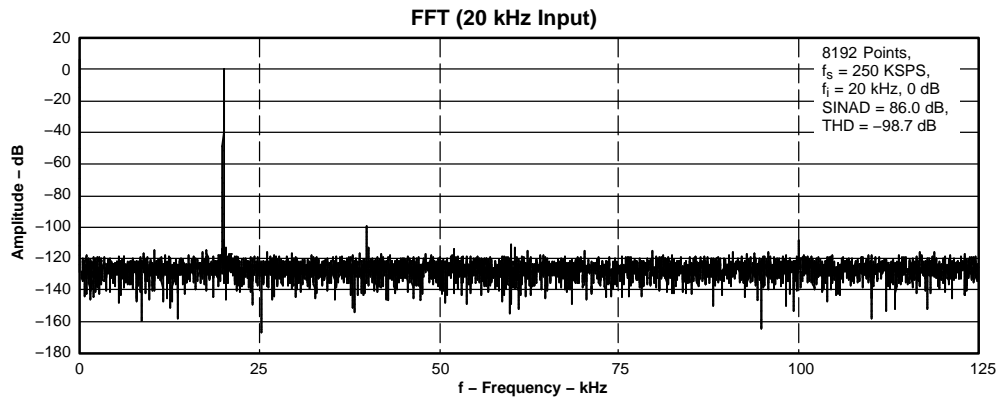


Figure 26.

BASIC OPERATION

Two signals control conversion in the ADS8509: \overline{CS} and R/\overline{C} . These two signals are internally ORed together. To start a conversion the chip must be selected, \overline{CS} low, and the conversion signal must be active, R/\overline{C} low. Either signal can be brought low first. Conversion starts on the falling edge of the second signal. \overline{BUSY} goes low when conversion starts and returns high after the data from that conversion is shifted into the internal storage register. Sampling begins when \overline{BUSY} goes high.

To reduce the number of control pins \overline{CS} can be tied low permanently. The R/\overline{C} pin now controls conversion and data reading exclusively. In the external clock mode this means that the ADS8509 will clock out data whenever R/\overline{C} is brought high and the external clock is active. In the internal clock mode data is clocked out every convert cycle regardless of the states of \overline{CS} and R/\overline{C} . The ADS8509 provides a TAG input for cascading multiple converters together.

READING DATA

The conversion result is available as soon as \overline{BUSY} returns to high therefore, data always represents the conversion previously completed even when it is read during a conversion. The ADS8509 outputs serial data in either straight binary or binary two's complement format. The SB/\overline{BTC} pin controls the format. Data is shifted out MSB first. The first conversion immediately following a power-up will not produce a valid conversion result.

Data can be clocked out with either the internally generated clock or with an external clock. The EXT/\overline{INT} pin controls this function. If external clock is used the TAG input can be used to daisy-chain multiple ADS8509 data pins together.

INTERNAL DATACLK

In the internal clock mode data for the previous conversion is clocked out during each conversion period. The internal data clock is synchronized to the internal conversion clock so that it does not interfere with the conversion process.

The DATACLK pin becomes an output when EXT/\overline{INT} is low. 16 clock pulses are generated at the beginning of each conversion after timing t_8 is satisfied, i.e. you can only read previous conversion result during conversion. DATACLK returns to low when it is inactive. The 16 bits of serial data are shifted out the DATA pin synchronous to this clock with each bit available on a rising and then a falling edge. DATA pin returns to the state of TAG pin input sensed at the start of transmission.

EXTERNAL DATACLK

The external clock mode offers several ways to retrieve conversion results. However, since the external clock cannot be synchronized to the internal conversion clock care must be taken to avoid corrupting the data.

When $\overline{\text{EXT/INT}}$ is set high, the $\overline{\text{R/C}}$ and $\overline{\text{CS}}$ signals control the read state. When the read state is initiated the result from the previously completed conversion is shifted out the DATA pin synchronous to the external clock that is connected to the DATACLK pin. Each bit is available on a falling and then a rising edge. The maximum external clock speed of 28.5 MHz allows data shifted out quickly either at the beginning of conversion or the beginning of sampling.

There are several modes of operation available when using an external clock. It is recommended that the external clock run only while reading data. This is the discontinuous clock mode. Since the external clock is not synchronized to the internal clock that controls conversion slight changes in the external clock can cause conflicts that can corrupt the conversion process. Specifications with a continuously running external clock cannot be guaranteed. It is especially important that the external clock does not run during the second half of the conversion cycle (approximately the time period specified by t_{d11} , see timing table).

In the discontinuous clock mode data can be read during conversion or during sampling, with or without a SYNC pulse. Data read during a conversion must meet the t_{d11} timing specification. Data read during sampling must be complete before starting a conversion.

Whether reading during sampling or during conversion a SYNC pulse is generated whenever at least one rising edge of the external clock occurs while the part is not in the read state. In the *discontinuous external clock with SYNC* mode a SYNC pulse follows the first rising edge after the read command. The data is shifted out after the SYNC pulse. The first rising clock edge after the read command generates a SYNC pulse. The SYNC pulse can be detected on the next falling edge and then the next rising edge. Successively, each bit can be read first on the falling edge and then on the next rising edge. Thus 17 clock pulses after the read command are required to read on the falling edge. 18 clock pulses are necessary to read on the rising edge.

Table 2. DATACLK Pulses

| DESCRIPTION | DATACLK PULSES REQUIRED | |
|---------------------------------|-------------------------|--------------|
| | WITH SYNC | WITHOUT SYNC |
| Read on falling edge of DATACLK | 17 | 16 |
| Read on rising edge of DATACLK | 18 | 17 |

If the clock is entirely inactive when not in the read state no SYNC pulse is generated. In this case the first rising clock edge shifts out the MSB. The MSB can be read on the first falling edge or on the next rising edge. In this *discontinuous external clock mode with no SYNC*, 16 clocks are necessary to read the data on the falling edge and 17 clocks for reading on the rising edge. Data always represents the conversion already completed.

TAG FEATURE

The TAG feature allows the data from multiple ADS8509 converters to be read on a single serial line. The converters are cascaded together using the DATA pins as outputs and the TAG pins as inputs as illustrated in [Figure 27](#). The DATA pin of the last converter drives the processor's serial data input. Data is then shifted through each converter, synchronous to the externally supplied data clock, onto the serial data line. The internal clock cannot be used for this configuration.

The preferred timing uses the discontinuous, external, data clock during the sampling period. Data must be read during the sampling period because there is not sufficient time to read data from multiple converters during a conversion period without violating the t_{d11} constraint (see the EXTERNAL DATA CLOCK section). The sampling period must be sufficiently long to allow all data words to be read before starting a new conversion.

Note, in [Figure 27](#), that a NULL bit separates the data word from each converter. The state of the DATA pin at the end of a READ cycle reflects the state of the TAG pin at the start of the cycle. This is true in all READ modes, including the internal clock mode. For example, when a single converter is used in the internal clock mode the state of the TAG pin determines the state of the DATA pin after all 16 bits have shifted out. When multiple converters are cascaded together this state forms the NULL bit that separates the words. Thus, with the TAG pin of the first converter grounded as shown in [Figure 27](#) the NULL bit becomes a zero between each data word.

Table 3. Input Range Connections (see Figure 29 and Figure 30 for complete information)

| ANALOG INPUT RANGE | CONNECT R1 _{IN} VIA 200 Ω TO | CONNECT R2 _{IN} VIA 100 Ω TO | CONNECT R3 TO | IMPEDANCE |
|--------------------|---------------------------------------|---------------------------------------|-----------------|-----------|
| ±10 V | V _{IN} | AGND | CAP | 11.5 kΩ |
| ±5 V | AGND | V _{IN} | CAP | 6.7 kΩ |
| ±3.33 V | V _{IN} | V _{IN} | CAP | 5.4 kΩ |
| 0 V to 10 V | AGND | V _{IN} | AGND | 6.7 kΩ |
| 0 V to 5 V | AGND | AGND | V _{IN} | 5.0 kΩ |
| 0 V to 4 V | V _{IN} | AGND | V _{IN} | 5.4 kΩ |

Table 4. Control Truth Table

| SPECIFIC FUNCTION | CS | R/C | BUSY | EXT/INT | DATACLK | PWRD | SB/BTC | OPERATION |
|--|-------|-------|-------|---------|---------|------|--------|--|
| Initiate conversion and output data using internal clock | 1 > 0 | 0 | 1 | 0 | Output | 0 | x | Initiates conversion <i>n</i> . Data from conversion <i>n</i> - 1 clocked out on DATA synchronized to 16 clock pulses output on DATACLK. |
| | 0 | 1 > 0 | 1 | 0 | Output | 0 | x | |
| Initiate conversion and output data using external clock | 1 > 0 | 0 | 1 | 1 | Input | 0 | x | Initiates conversion <i>n</i> . |
| | 0 | 1 > 0 | 1 | 1 | Input | 0 | x | Initiates conversion <i>n</i> . |
| | 1 > 0 | 1 | 1 | 1 | Input | x | x | Outputs data with or without SYNC pulse. See section Reading Data. |
| | 1 > 0 | 1 | 0 | 1 | Input | 0 | x | Outputs data with or without SYNC pulse. See section Reading Data. |
| | 0 | 0 > 1 | 0 | 1 | Input | 0 | x | Outputs data with or without SYNC pulse. See section Reading Data. |
| No actions | 0 | 0 | 0 > 1 | x | x | 0 | x | This is an acceptable condition. |
| Power down | x | x | x | x | x | 0 | x | Analog circuitry powered. Conversion can proceed.. |
| | x | x | x | x | x | 1 | x | Analog circuitry disabled. Data from previous conversion maintained in output registers. |
| Selecting output format | x | x | x | x | x | x | 0 | Serial data is output in binary 2s complement format. |
| | x | x | x | x | x | x | 1 | Serial data is output in straight binary format. |

Table 5. Output Codes and Ideal Input Voltages

| DESCRIPTION | ANALOG INPUT | | | | | | DIGITAL OUTPUT | | | |
|-----------------------------|--------------|------------|-------------|-------------|------------|------------|-------------------------------------|----------|-------------------------------|----------|
| | | | | | | | BINARY 2's COMPLEMENTS (SB/BTC LOW) | | STRAIGHT BINARY (SB/BTC HIGH) | |
| | | | | | | | BINARY CODE | HEX CODE | BINARY CODE | HEX CODE |
| Full-scale range | ±10 | ±5 | ±3.33 V | 0 V to 10 V | 0 V to 5 V | 0 V to 4 V | | | | |
| Least significant bit (LSB) | 305 μV | 153 μV | 102 μV | 153 μV | 76 μV | 61 μV | | | | |
| Full scale (FS - 1LSB) | 9.999695 V | 4.999847 V | 3.333231 V | 9.999847 V | 4.999924 V | 3.999939 V | 0111 1111 1111 1111 | 7FFF | 1111 1111 1111 1111 | FFFF |
| Midscale | 0 V | 0 V | 0 V | 5 V | 2.5 V | 2 V | 0000 0000 0000 0000 | 0000 | 1000 0000 0000 0000 | 8000 |
| One LSB below midscale | -305 μV | 153 μV | ±102 μV | 4.999847 V | 2.499924 V | 1.999939 V | 1111 1111 1111 1111 | FFFF | 0111 1111 1111 1111 | 7FFF |
| -Full scale | -10 V | -5 V | -3.333333 V | 0 V | 0 V | 0 V | 1000 0000 0000 0000 | 8000 | 0000 0000 0000 0000 | 0000 |

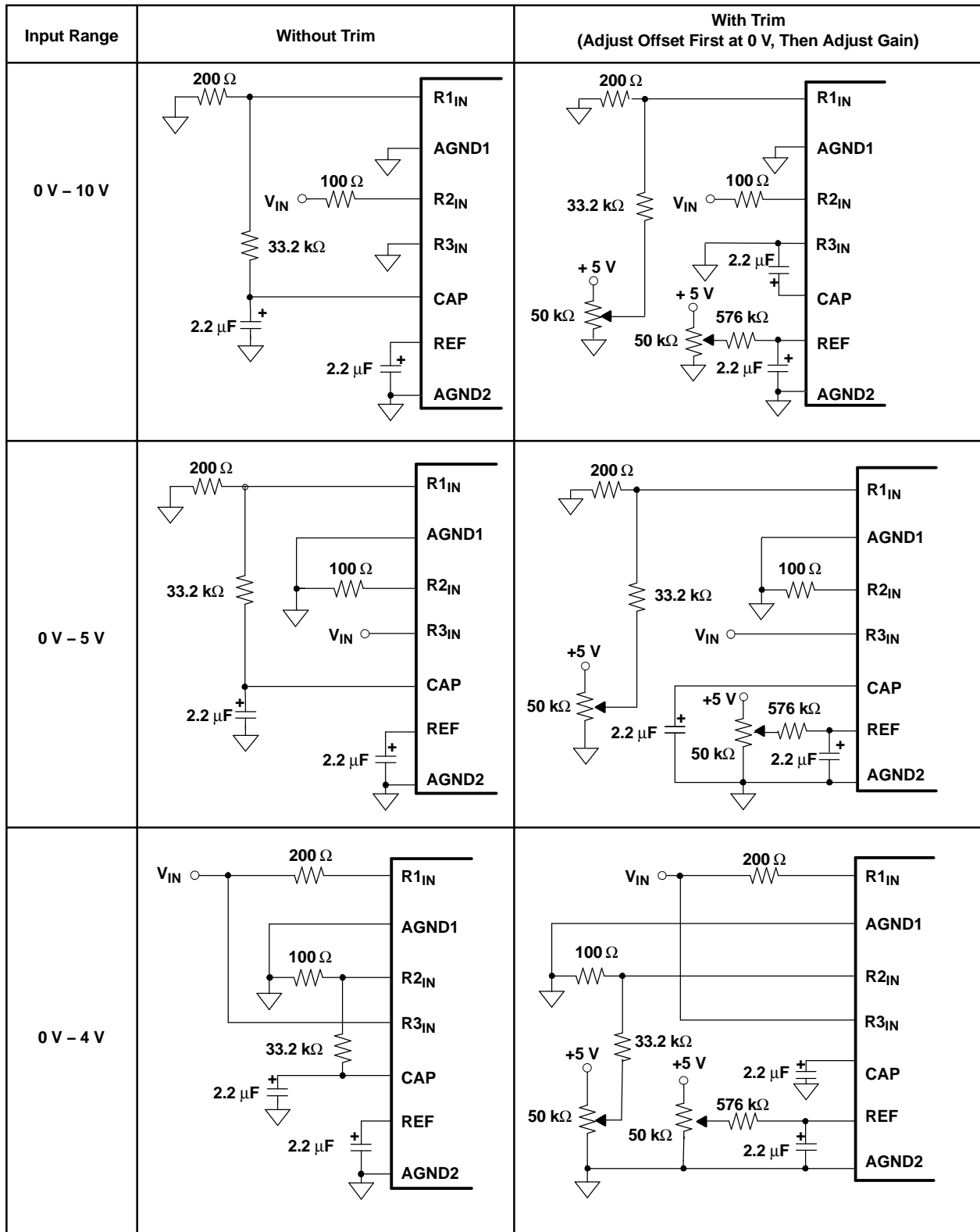


Figure 29. Offset/Gain Circuits for Unipolar Input Ranges

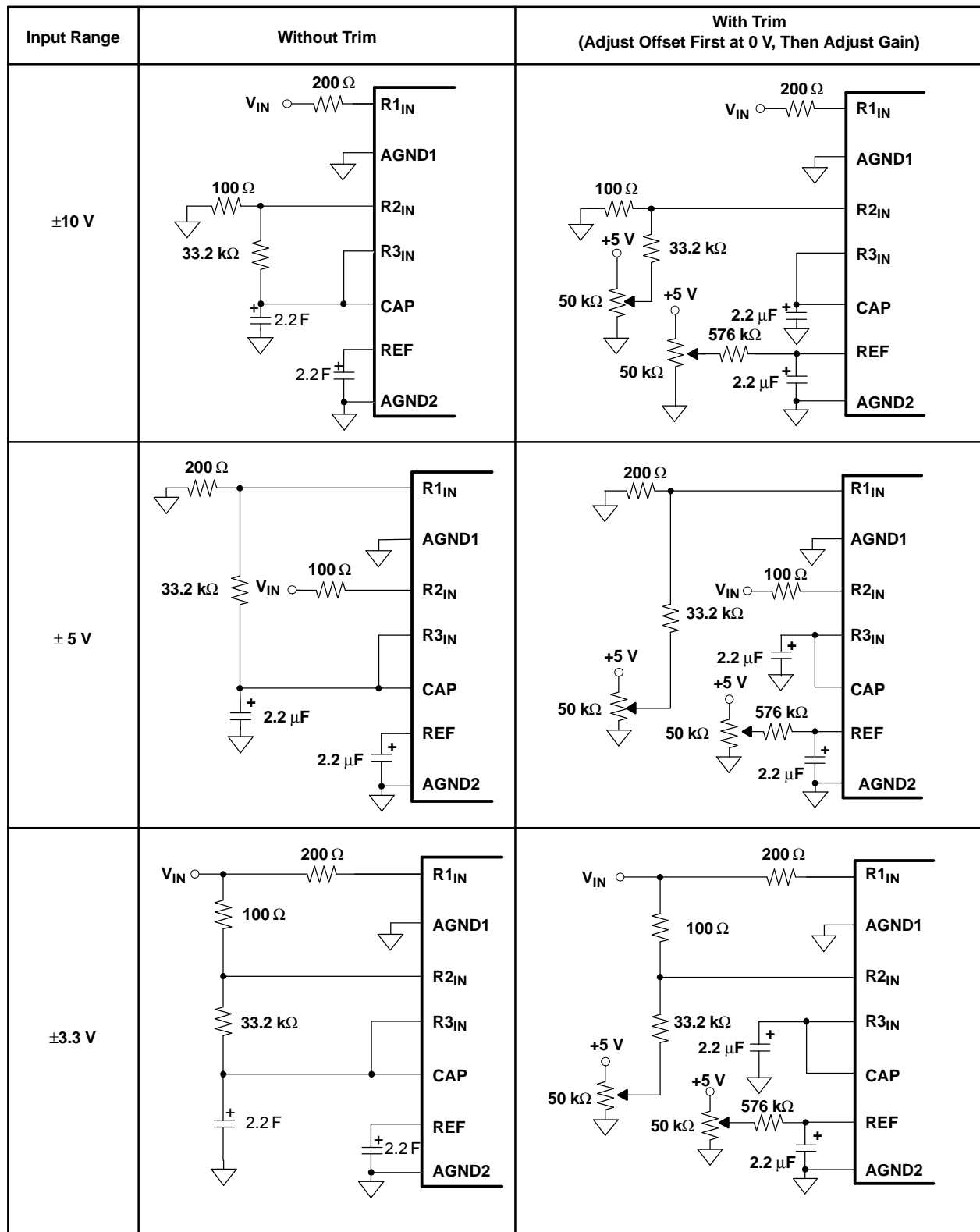


Figure 30. Offset/Gain Circuits for Bipolar Input Ranges

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| ADS8509IBDB | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IBDBG4 | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IBDBR | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IBDBRG4 | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IBDW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IBDWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IBDWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IBDWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IDB | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IDBG4 | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IDBR | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IDBRG4 | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IDW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IDWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IDWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8509IDWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

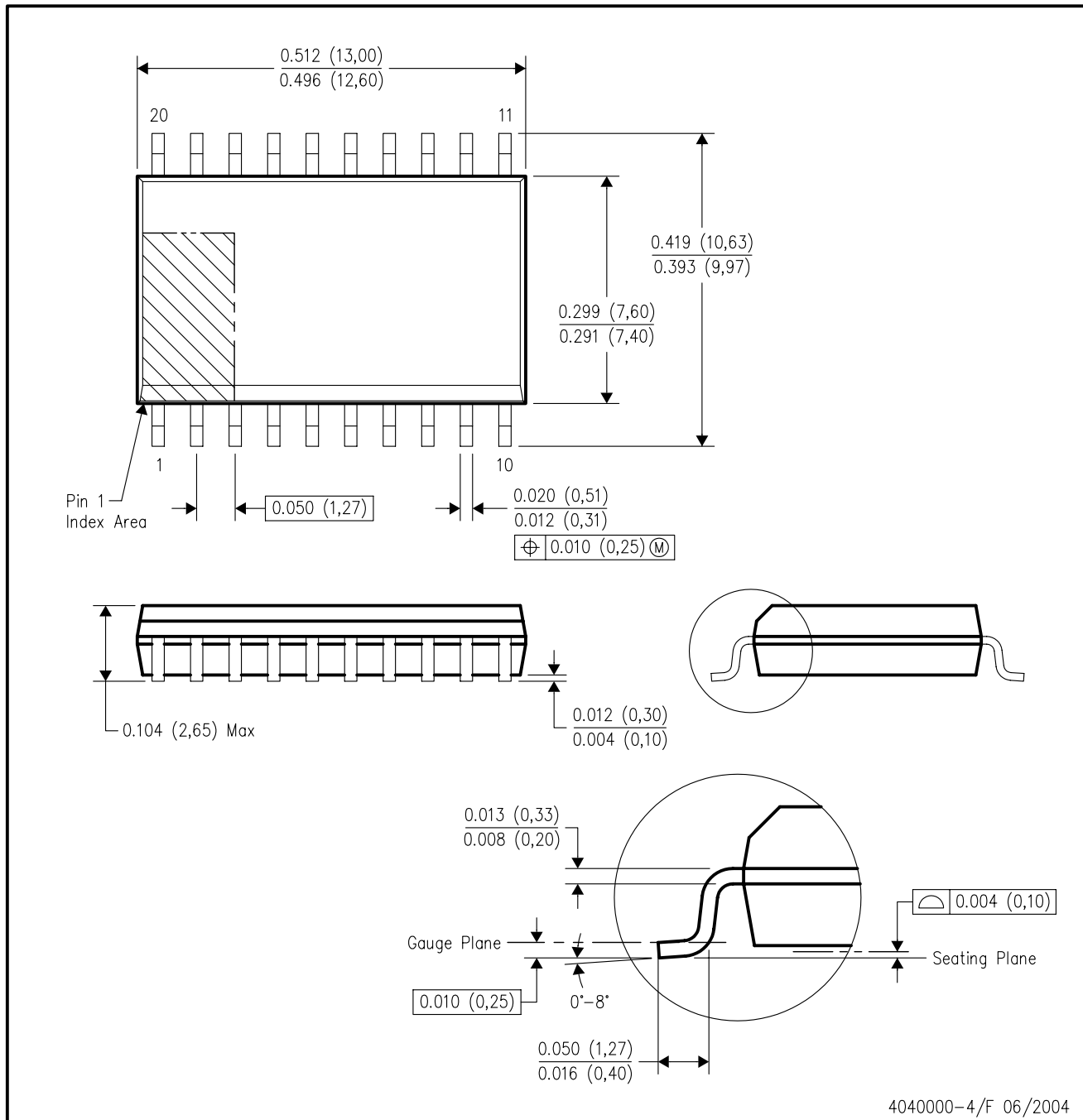
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



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 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

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Mailing Address: Texas Instruments
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