



10-Bit, 200-MSPS, 4-Channel and 12-Bit, 80-MSPS, 8-Channel Analog-to-Digital Converter

Check for Samples: [ADS5296](#)

FEATURES

- **Configurable Modes of Operation:**
 - 10-Bit, 200-MSPS, 4-Channel ADC
 - 12-Bit, 160-MSPS, 4-Channel ADC
 - 10-Bit, 100-MSPS, 8-Channel ADC
 - 12-Bit, 80-MSPS, 8-Channel ADC
- **Designed for Low Power:**
 - 70 mW per Channel at 80 MSPS (12-Bit, 8-Channel)
 - 157 mW per Channel at 200 MSPS (10-Bit, 4-Channel)
- **12-Bit, 80 MSPS:**
 - SNR: 70.3 dBFS
- **10-Bit, 200 MSPS:**
 - SNR: 61.4 dBFS
 - Interleaving Spur: > 60 dBc at 90 MHz
- **Serial LVDS One-Wire Interface:**
 - 10x Serialization up to 1000 Mbps Data Rate per Wire
 - 12x Serialization up to 960 Mbps Data Rate per Wire
- **Digital Processing Block:**
 - Programmable FIR Decimation Filter and Oversampling to Minimize Harmonic Interference
 - Programmable IIR High-Pass Filter to Minimize DC Offset
 - Programmable Digital Gain: 0 dB to 12 dB
- **Low-Frequency Noise Suppression Mode**
- **Programmable Mapping Between ADC Input Channels and LVDS Output Pins**
- **Channel Averaging Mode**
- **Variety of LVDS Test Patterns to Verify Data Capture by FPGA or Receiver**
- **Package: 9-mm × 9-mm QFN-64**

APPLICATIONS

- **Ultrasound Imaging**
- **Communication Applications**
- **Multichannel Data Acquisition**



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DESCRIPTION

The ADS5296 is a low-power, 12-bit, 8-channel, analog-to-digital converter (ADC) with sample rates up to 80 MSPS. However, the device can also be configured to operate as a 4-channel ADC running at 2x the sample rate by interleaving data from two ADC channels. In interleaving mode, the device accepts a double frequency input clock. Each ADC in a pair converts a common analog input signal at alternate rising edges of the 2x input clock. The device can either be configured as a 10-bit, 4-channel ADC with sample rates up to 200 MSPS or as a 12-bit, 4-channel ADC with sample rates up to 160 MSPS.

The data from each ADC within the interleaved pair is output in serial format over one LVDS pair up to a maximum data rate of 1 Gbps (10 bits at 100 MSPS). With interleaving disabled, the ADS5296 can also be operated as an 8-channel, 10-bit device with sample rates up to 100 MSPS.

Several digital functions commonly used in systems are included in the device. These functions include a low-frequency noise suppression (LFNS) mode, digital filtering options, and programmable mapping of LVDS output pins and analog input channels.

For low input frequency applications, the LFNS mode enables the suppression of noise at low frequencies and improves SNR in the 1-MHz band near dc by approximately 3 dB. Digital filtering options include low-pass, high-pass, and band-pass digital filters as well as dc offset removal filters.

Low power consumption and integration of multiple channels in a small package makes the device attractive for high channel count data acquisition systems. The device is available in a compact 9-mm × 9-mm QFN-64 package. The ADS5296 is specified over the –40°C to +85°C operating temperature range.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|---------|
| ADS5296RGCR | PREVIEW | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS5296 | |
| ADS5296RGCT | PREVIEW | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS5296 | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

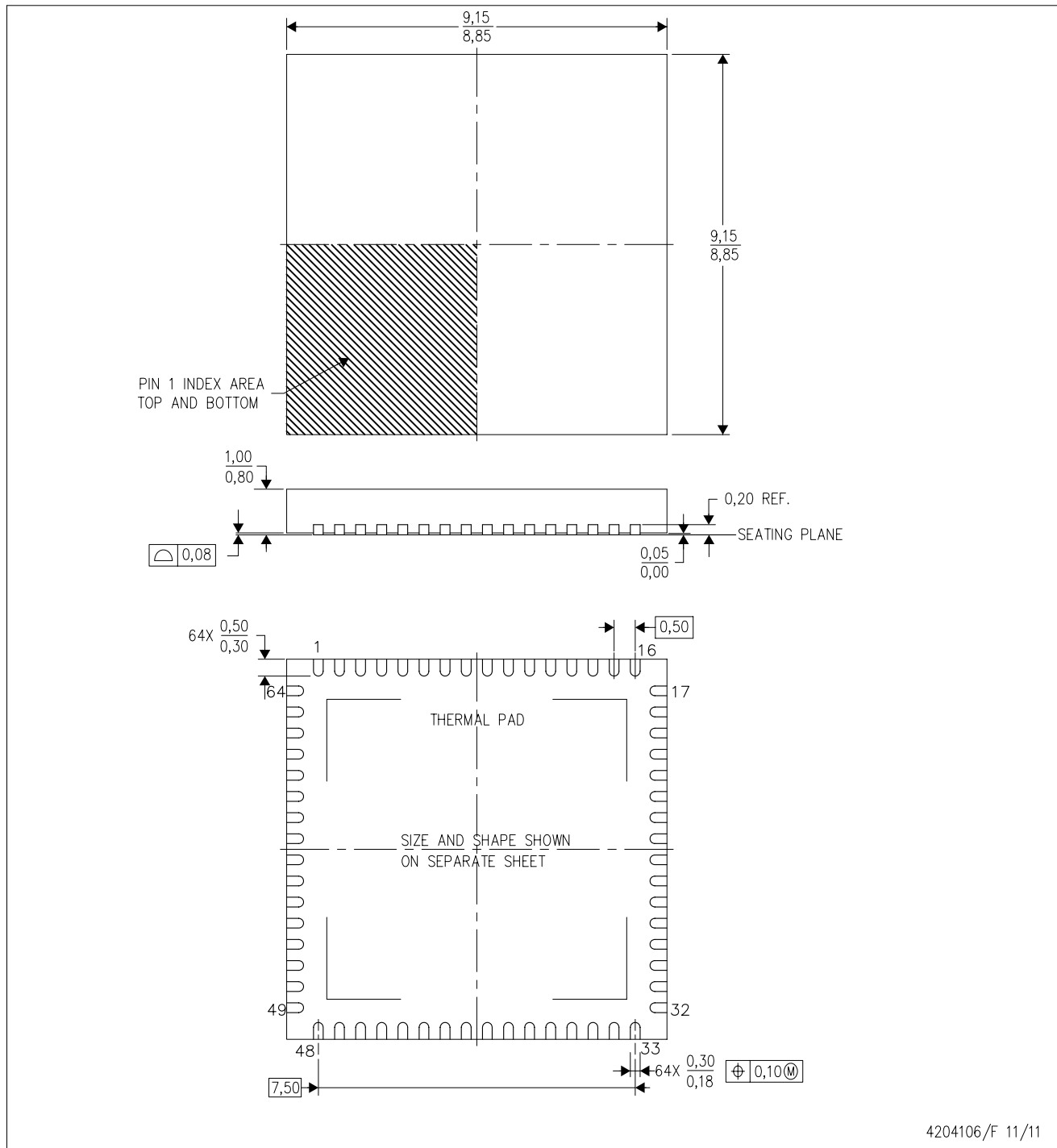
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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MECHANICAL DATA

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



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- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

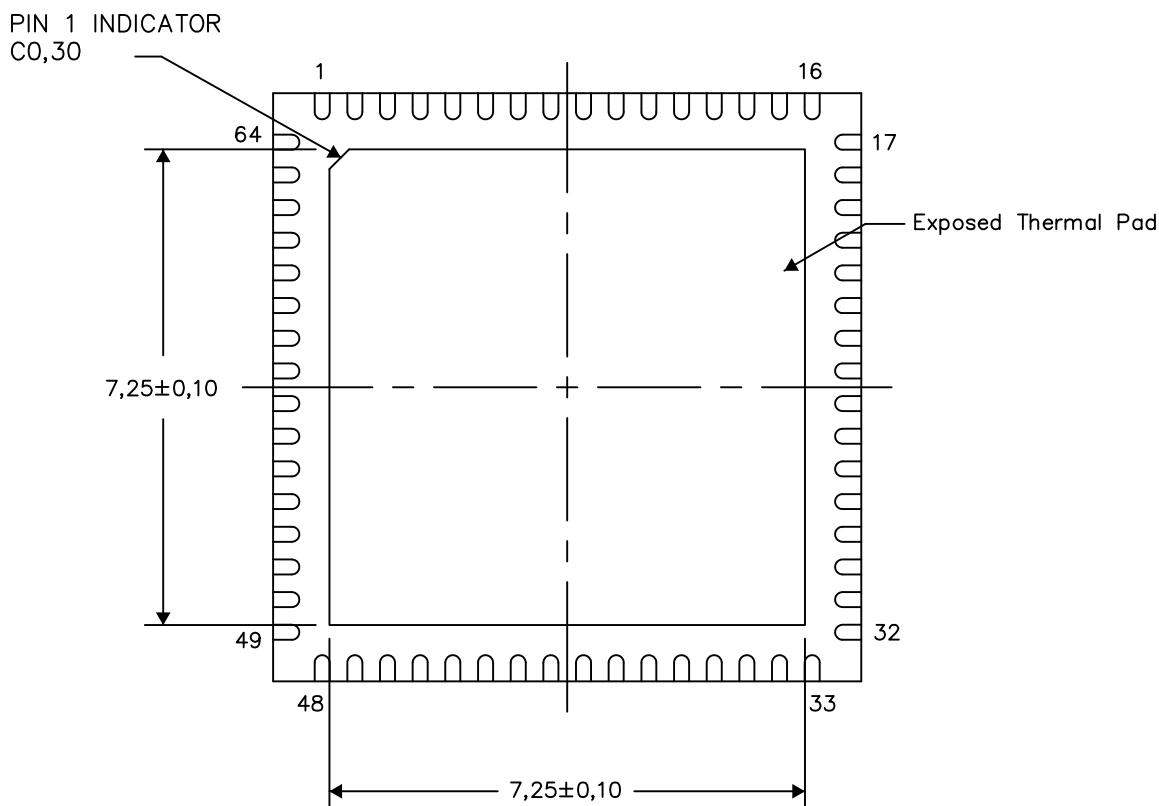
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

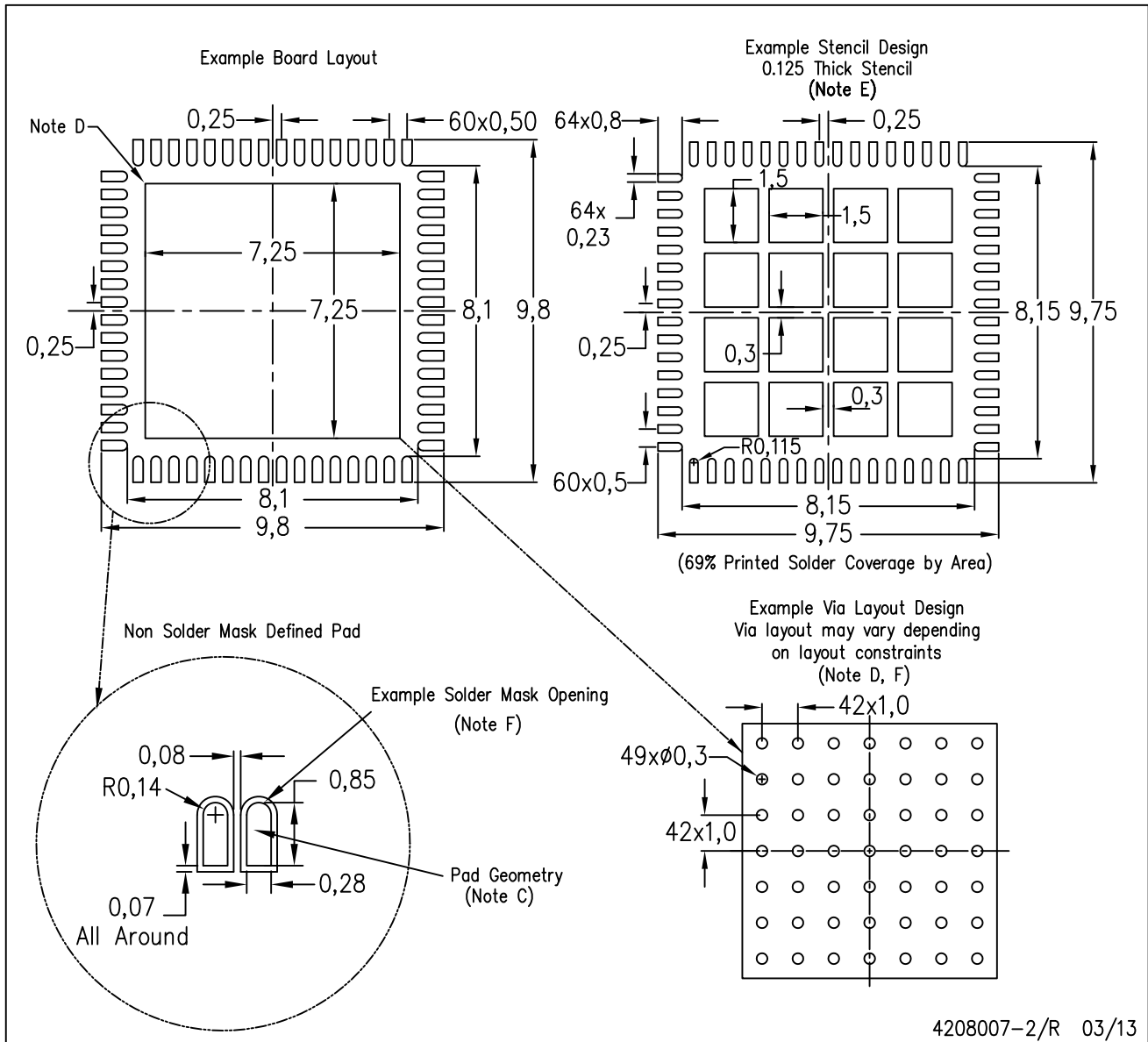


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NOTE: A. All linear dimensions are in millimeters

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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