



8-Channel, 24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 24 BITS NO MISSING CODES
- INL: 0.0012% of FSR (max)
- FULL-SCALE INPUT: $\pm 2V_{REF}$
- PGA FROM 1 TO 128
- 22 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)
- SINGLE CYCLE SETTLING MODE
- PROGRAMMABLE DATA OUTPUT RATES UP TO 1kHz
- ON-CHIP 1.25V/2.5V REFERENCE
- ON-CHIP CALIBRATION
- SPI COMPATIBLE
- POWER SUPPLY: 2.7V to 5.25V
- < 1mW POWER CONSUMPTION, $V_{DD} = 3V$

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTATION
- WEIGH SCALES
- PRESSURE TRANSDUCERS

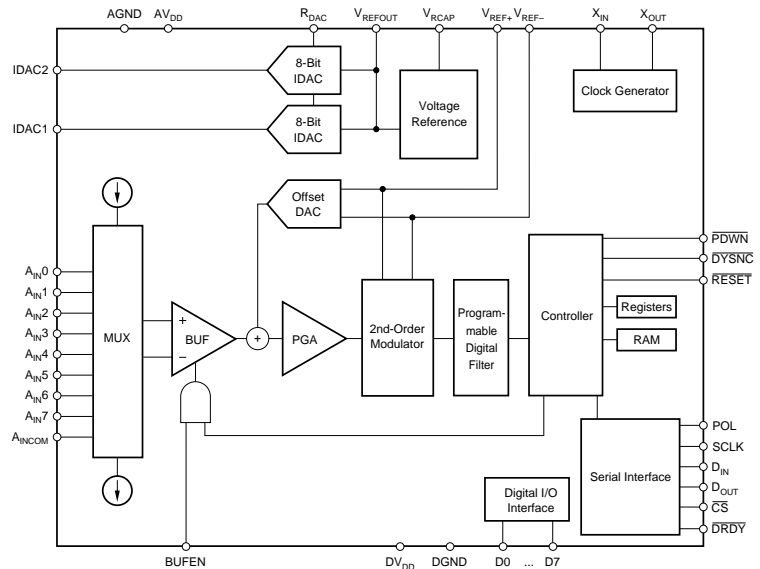
DESCRIPTION

The ADS1217 is a precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converter with 24-bit resolution operating from 2.7V to 5.25V supplies. The delta-sigma, A/D converter provides up to 24 bits of no missing code performance and effective resolution of 22 bits.

The eight input channels are multiplexed. Internal buffering can be selected to provide a very high input impedance for direct connection to transducers or low-level voltage signals. Burnout current sources are provided that allow for the detection of an open or shorted sensor. An 8-bit Digital-to-Analog Converter (DAC) provides an offset correction with a range of 50% of the FSR (Full-Scale Range).

The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 with an effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a 2nd-order, delta-sigma modulator and programmable sinc filter. The reference input is differential and can be used for ratiometric measurements. The onboard current DACs operate independently with the maximum current set by an external resistor.

The serial interface is SPI compatible. Eight bits of digital I/O are also provided that can be used for input or output. The ADS1217 is designed for high-resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|--|--------------------------------------|
| AV _{DD} to AGND | -0.3V to +6V |
| DV _{DD} to DGND | -0.3V to +6V |
| Input Current | 100mA, Momentary |
| Input Current | 10mA, Continuous |
| A _{IN} | GND -0.5V to AV _{DD} + 0.5V |
| AV _{DD} to DV _{DD} | -6V to +6V |
| AGND to DGND | -0.3V to +0.3V |
| Digital Input Voltage to GND | -0.3V to DV _{DD} + 0.3V |
| Digital Output Voltage to GND | -0.3V to DV _{DD} + 0.3V |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -60°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---------|--------------|--------------------|-----------------------------|-----------------|-----------------|---------------------------|
| ADS1217 | TQFP-48 | PFB | -40°C to +85°C | ADS1217 | ADS1217IPFBT | Tape and Reel, 250 |
| " | " | " | " | " | ADS1217IPFBR | Tape and Reel, 2000 |

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V

All specifications at -40°C to +85°C, AV_{DD} = +5V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, and V_{REF} = +2.5V, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1217 | | | UNITS |
|--|---|-------------|-----------------------------|------------------------|-------------------------|
| | | MIN | TYP | MAX | |
| ANALOG INPUT (A_{IN0} – A_{IN7}, A_{INCOM}) | | | | | |
| Full-Scale Input Voltage | (A _{IN+}) – (A _{IN-}) | | ±2V _{REF} /PGA | | V |
| Analog Input Voltage | Buffer OFF | AGND – 0.1 | | AV _{DD} + 0.1 | V |
| | Buffer ON | AGND + 0.05 | | AV _{DD} – 1.5 | V |
| Differential Input Impedance | Buffer OFF | | 10/PGA | | MΩ |
| Input Current | Buffer ON | | 0.5 | | nA |
| Bandwidth | | | | | |
| Fast Settling Filter | -3dB | | 0.469f _{DATA} | | Hz |
| Sinc ² Filter | -3dB | | 0.318f _{DATA} | | Hz |
| Sinc ³ Filter | -3dB | | 0.262f _{DATA} | | Hz |
| Programmable Gain Amplifier | User Selectable Gain Ranges | 1 | | 128 | |
| Burnout Current Sources | | | 2 | | μA |
| OFFSET DAC | | | | | |
| Offset DAC Range | | | ±V _{REF} /(PGA) | | V |
| Offset DAC Monotonicity | | 8 | | | Bits |
| Offset DAC Gain Error | | | ±1 | | % |
| Offset DAC Gain Error Drift | | | 1 | | ppm/°C |
| SYSTEM PERFORMANCE | | | | | |
| Resolution | Sinc ³ Filter | 24 | | 24 | Bits |
| No Missing Codes | End Point Fit, Differential Input, Buffer Off | | 0.0003 | 0.0012 | Bits |
| Integral Nonlinearity | Before Calibration | | 7.5 | | % of FSR ⁽¹⁾ |
| Offset Error | After Calibration | | 0.02 | | ppm of FSR |
| Offset Drift | | | 0.005 | | ppm of FSR/°C |
| Gain Error | | | 0.5 | | % |
| Gain Error Drift | | | | | ppm/°C |
| Common-Mode Rejection | at DC | 100 | | | dB |
| | f _{CM} = 60Hz, f _{DATA} = 10Hz | | 130 | | dB |
| | f _{CM} = 50Hz, f _{DATA} = 50Hz | | 120 | | dB |
| | f _{CM} = 60Hz, f _{DATA} = 60Hz | | 120 | | dB |
| Normal-Mode Rejection | f _{SIG} = 50Hz, f _{DATA} = 50Hz | | 100 | | dB |
| | f _{SIG} = 60Hz, f _{DATA} = 60Hz | | 100 | | dB |
| Output Noise | | | See Typical Characteristics | | dB |
| Power-Supply Rejection | at DC, dB = -20log(ΔV _{OUT} /ΔV _{DD}) ⁽²⁾ | 80 | 95 | | dB |

NOTES: (1) FSR is Full-Scale Range. (2) ΔV_{OUT} is change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V (Cont.)

All specifications at -40°C to +85°C, AV_{DD} = +5V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, and V_{REF} = +2.5V, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1217 | | | UNITS |
|--|--|----------------------------|-----------------------------|----------------------------|--------|
| | | MIN | TYP | MAX | |
| VOLTAGE REFERENCE INPUT | | | | | |
| Reference Input (V _{REF}) | V _{REF} = (V _{REF+}) - (V _{REF-}) | 0.1 | 2.5 | 2.6 | V |
| Negative Reference Input (V _{REF-}) | | AGND - 0.1 | | (V _{REF+}) - 0.1 | V |
| Positive Reference Input (V _{REF+}) | | (V _{REF-}) + 0.1 | | AV _{DD} + 0.1 | V |
| Common-Mode Rejection | at DC | | 120 | | dB |
| Common-Mode Rejection | f _{VREFCM} = 60Hz, f _{DATA} = 60Hz | | 120 | | dB |
| Bias Current ⁽³⁾ | V _{REF} = 2.5V, PGA = 1 | | 1.3 | | μA |
| ON-CHIP VOLTAGE REFERENCE | | | | | |
| Output Voltage | REF HI = 1 | 2.4 | 2.5 | 2.6 | V |
| | REF HI = 0 | | 1.25 | | V |
| Short-Circuit Current Source | | | 8 | | mA |
| Short-Circuit Current Sink | | | 50 | | μA |
| Drift | | | 15 | | ppm/°C |
| Noise | V _{RCAP} = 0.1μF, BW = 0.1Hz to 100Hz | | 10 | | μVrms |
| Output Impedance | Sourcing 100μA | | 3 | | Ω |
| Startup Time | | | 5 | | ms |
| IDAC | | | | | |
| Full-Scale Output Current | R _{DAC} = 150kΩ, Range = 1 | | 0.5 | | mA |
| | R _{DAC} = 150kΩ, Range = 2 | | 1 | | mA |
| | R _{DAC} = 150kΩ, Range = 3 | | 2 | | mA |
| | R _{DAC} = 15kΩ, Range = 3 | | 20 | | mA |
| Current Setting Resistance (R _{DAC}) | | 10 | | | kΩ |
| Monotonicity | R _{DAC} = 150kΩ | 8 | | | Bits |
| Compliance Voltage | | 0 | | AV _{DD} - 1 | V |
| Output Impedance | | | See Typical Characteristics | | |
| PSRR | V _{OUT} = AV _{DD} /2, Code > 16 | | 400 | | ppm/V |
| Gain Error | Individual IDAC | | 5 | | % |
| Gain Error Drift | Individual IDAC | | 75 | | ppm/°C |
| Gain Error Mismatch | Between IDACs, Same Range and Code | | 0.25 | | % |
| Gain Error Mismatch Drift | Between IDACs, Same Range and Code | | 15 | | ppm/°C |
| POWER-SUPPLY REQUIREMENTS | | | | | |
| Power-Supply Voltage | AV _{DD} | 4.75 | | 5.25 | V |
| Analog Current (I _{ADC} + I _{VREF} + I _{IDAC}) | PDWN = 0, or SLEEP | | 1 | | nA |
| A/D Converter Current (I _{ADC}) | PGA = 1, Buffer OFF | | 175 | 275 | μA |
| | PGA = 128, Buffer OFF | | 500 | 750 | μA |
| | PGA = 1, Buffer ON | | 250 | 350 | μA |
| | PGA = 128, Buffer ON | | 900 | 1375 | μA |
| V _{REF} Current (I _{VREF}) | | | 250 | 375 | μA |
| I _{IDAC} Current (I _{IDAC}) | Excludes Load Current | | 480 | 675 | μA |
| Digital Current | Normal Mode, DV _{DD} = 5V | | 180 | 275 | μA |
| | SLEEP Mode, DV _{DD} = 5V | | 150 | | μA |
| | Read Data Continuous Mode, DV _{DD} = 5V | | 230 | | μA |
| | PDWN = 0 | | 1 | | nA |
| Power Dissipation | PGA = 1, Buffer OFF, REFEN = 0, IDACs OFF, DV _{DD} = 5V | | 1.8 | 2.8 | mW |

NOTES: (1) FSR is Full-Scale Range. (2) ΔV_{OUT} is change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

ELECTRICAL CHARACTERISTICS: $AV_{DD} = 3V$ (Cont.)

All specifications at -40°C to $+85^{\circ}\text{C}$, $AV_{DD} = +3V$, $DV_{DD} = +2.7V$ to $5.25V$, $f_{MOD} = 19.2\text{kHz}$, $\text{PGA} = 1$, Buffer ON, $R_{DAC} = 75\text{k}\Omega$, $f_{DATA} = 10\text{Hz}$, and $V_{REF} = +1.25V$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1217 | | | UNITS |
|---|--|---------|--------------------------|---------------------------|--|
| | | MIN | TYP | MAX | |
| POWER-SUPPLY REQUIREMENTS | | | | | |
| Power-Supply Voltage | AV_{DD} | 2.7 | | 3.3 | V |
| Analog Current ($I_{ADC} + I_{VREF} + I_{DAC}$) | $\overline{\text{PDWN}} = 0$, or SLEEP PGA = 1, Buffer OFF | | 1 | | nA |
| A/D Converter Current (I_{ADC}) | PGA = 128, Buffer OFF PGA = 1, Buffer ON PGA = 128, Buffer ON | | 160 450 230 850 | 250 700 325 1325 | μA μA μA μA |
| V_{REF} Current (I_{VREF}) | | | 250 | 375 | μA |
| I_{DAC} Current (I_{DAC}) | Excludes Load Current | | 480 | 675 | μA |
| Digital Current | Normal Mode, $DV_{DD} = 3V$ SLEEP Mode, $DV_{DD} = 3V$ Read Data Continuous Mode, $DV_{DD} = 3V$ PDWN = 0 | | 90 75 113 1 | 200 | μA μA μA nA |
| Power Dissipation | PGA = 1, Buffer OFF, REFEN = 0, IDACs OFF, $DV_{DD} = 3V$ | | 0.8 | 1.4 | mW |

NOTES: (1) FSR is Full-Scale Range. (2) ΔV_{OUT} is change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

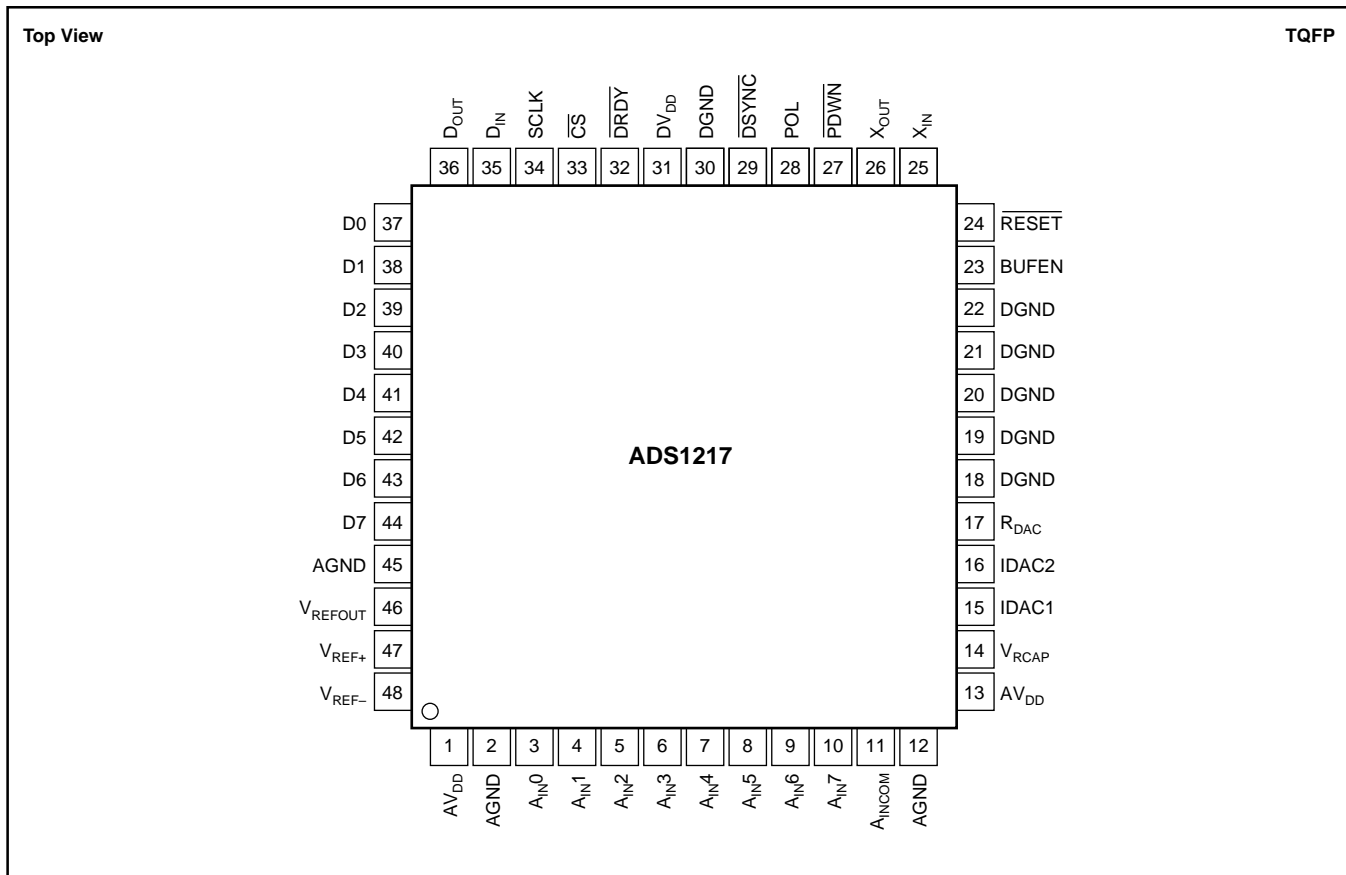
ELECTRICAL CHARACTERISTICS: Digital

All specifications at -40°C to $+85^{\circ}\text{C}$, and $DV_{DD} = +2.7V$ to $5.25V$.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-----------------------|----------------------|-----|----------------------|---------------|
| INPUT/OUTPUT | | | | | |
| Logic Level | | | | | |
| V_{IH} | | $0.8 \times DV_{DD}$ | | DV_{DD} | V |
| $V_{IL}^{(1)}$ | | DGND | | $0.2 \times DV_{DD}$ | V |
| V_{OH} | $I_{OH} = 1\text{mA}$ | $DV_{DD} - 0.4$ | | | V |
| V_{OL} | $I_{OL} = 1\text{mA}$ | DGND | | $DGND + 0.4$ | V |
| Input Leakage: I_{IN} | $0 < V_I < DV_{DD}$ | -10 | | 10 | μA |
| CLOCK RATES | | | | | |
| Master Clock Rate: f_{OSC} | | 1 | | 8 | MHz |
| Master Clock Period: t_{OSC} | $1/f_{OSC}$ | 125 | | 1000 | ns |

NOTE: (1) Maximum V_{IL} for X_{IN} is DGND + 0.05V.

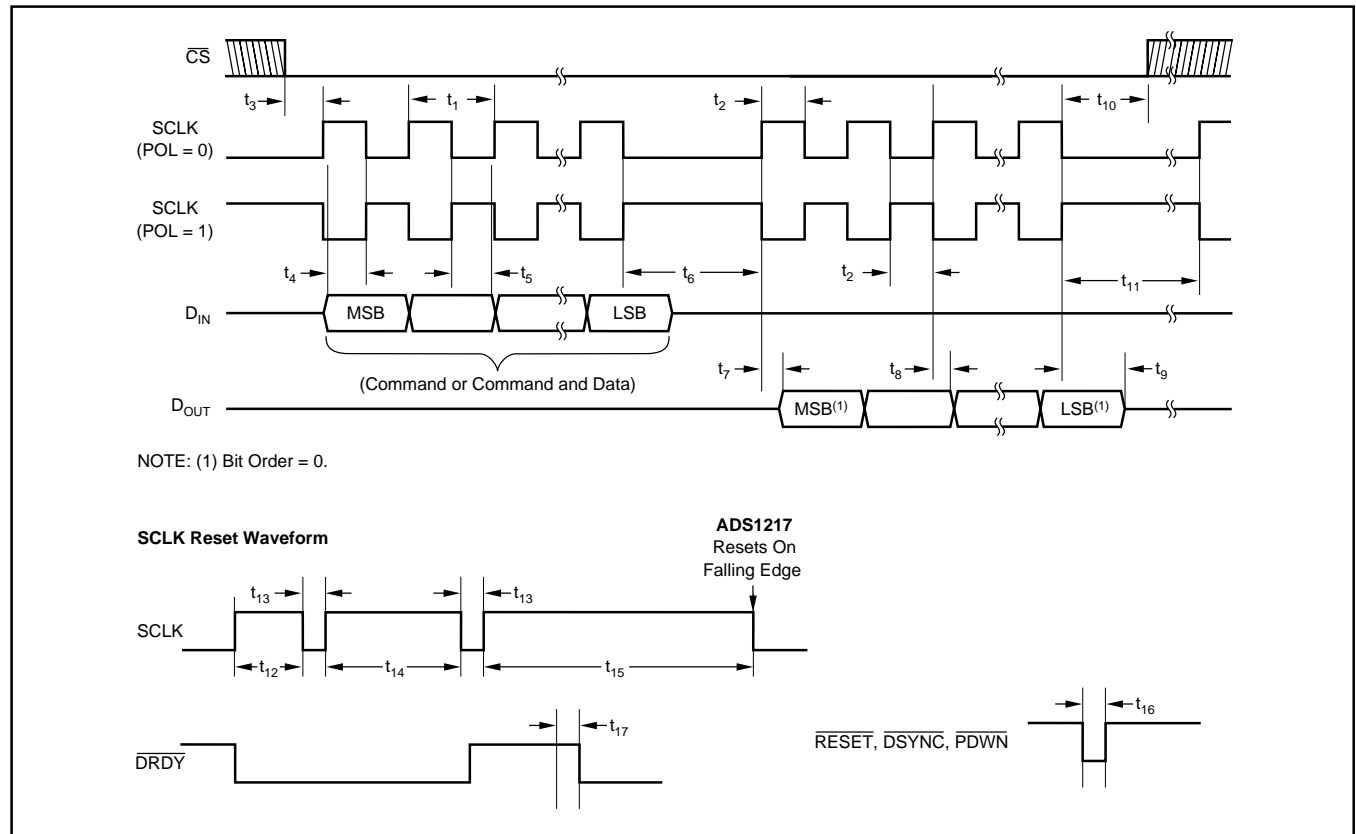
PIN CONFIGURATION



PIN DESCRIPTIONS

| PIN NUMBER | NAME | DESCRIPTION | PIN NUMBER | NAME | DESCRIPTION |
|------------|--------------------|--------------------------------------|------------|---------------------|---|
| 1 | AV _{DD} | Analog Power Supply | 25 | X _{IN} | Clock Input |
| 2 | AGND | Analog Ground | 26 | X _{OUT} | Clock Output, used with crystal or resonator. |
| 3 | A _{IN0} | Analog Input 0 | 27 | PDWN | Active LOW. Power Down. The power-down function shuts down the analog and digital circuits. |
| 4 | A _{IN1} | Analog Input 1 | | | |
| 5 | A _{IN2} | Analog Input 2 | 28 | POL | Serial Clock Polarity Input |
| 6 | A _{IN3} | Analog Input 3 | 29 | DSYNC | Active LOW, Synchronization Control Input |
| 7 | A _{IN4} | Analog Input 4 | 30 | DGND | Digital Ground |
| 8 | A _{IN5} | Analog Input 5 | 31 | DV _{DD} | Digital Power Supply |
| 9 | A _{IN6} | Analog Input 6 | 32 | DRDY | Active LOW, Data Ready Output |
| 10 | A _{IN7} | Analog Input 7 | 33 | CS | Active LOW, Chip Select Input |
| 11 | A _{INCOM} | Analog Input Common | 34 | SCLK | Serial Clock, Schmitt Trigger |
| 12 | AGND | Analog Ground | 35 | D _{IN} | Serial Data Input, Schmitt Trigger |
| 13 | AV _{DD} | Analog Power Supply | 36 | D _{OUT} | Serial Data Output |
| 14 | V _{RCAP} | V _{REFOUT} Bypass Capacitor | 37-44 | D0-D7 | Digital I/O 0-7 |
| 15 | IDAC1 | Current DAC1 Output | 45 | AGND | Analog Ground |
| 16 | IDAC2 | Current DAC2 Output | 46 | V _{REFOUT} | Voltage Reference Output |
| 17 | R _{DAC} | Current DAC Resistor | 47 | V _{REF+} | Positive Differential Reference Input |
| 18-22 | DGND | Digital Ground | 48 | V _{REF-} | Negative Differential Reference Input |
| 23 | BUFEN | Buffer Enable Input | | | |
| 24 | RESET | Active LOW, resets the entire chip. | | | |

TIMING DIAGRAMS



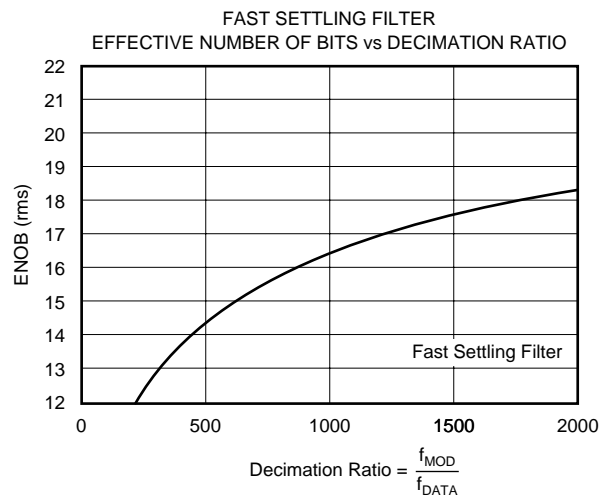
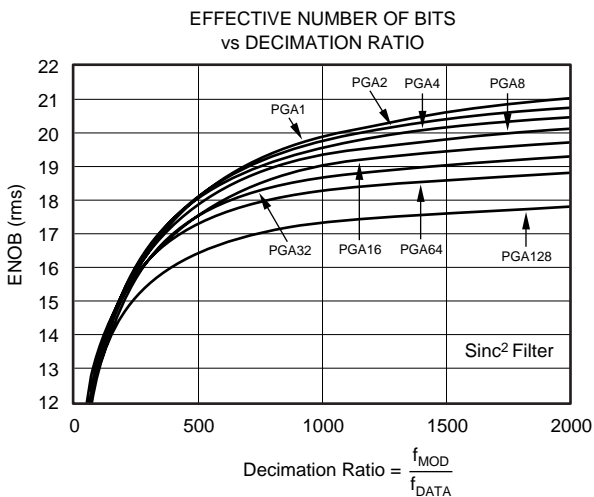
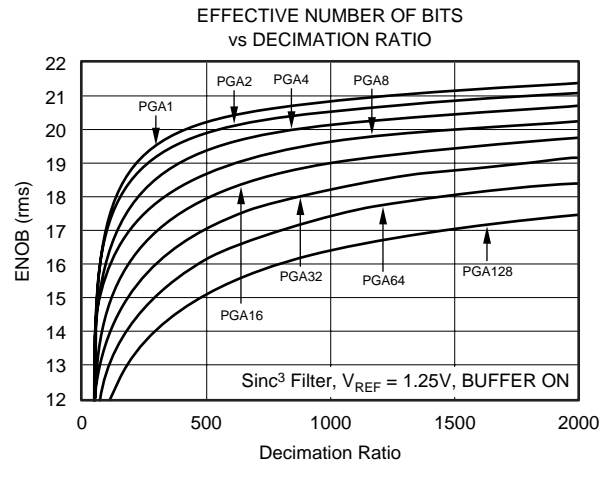
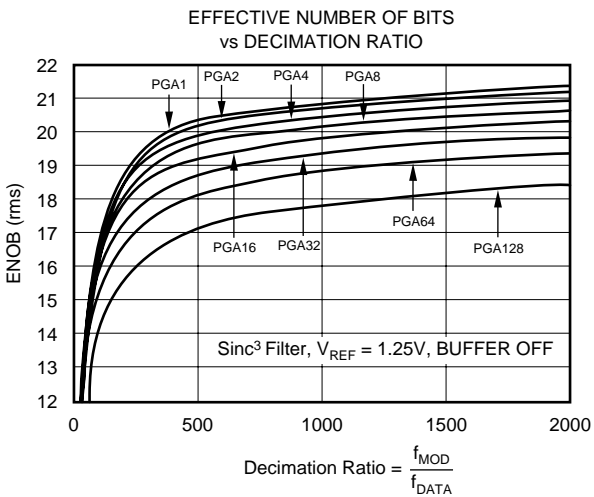
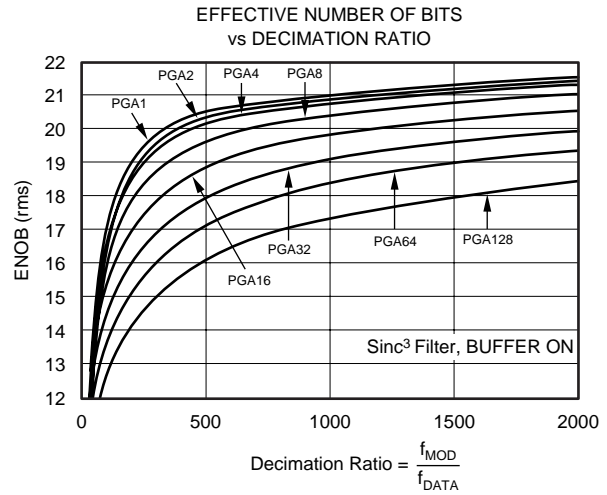
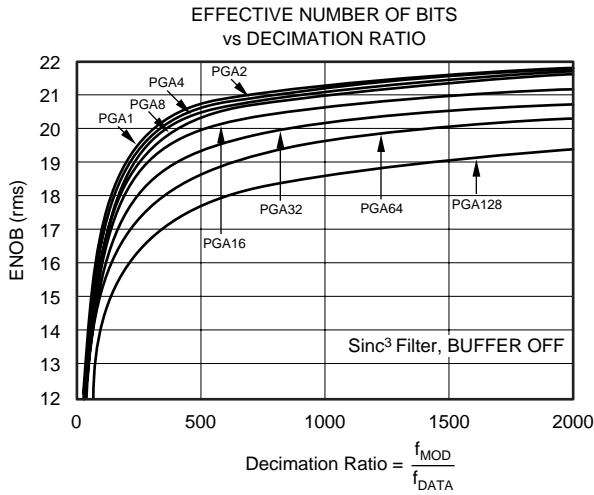
TIMING CHARACTERISTICS

| SPEC | DESCRIPTION | MIN | MAX | UNITS |
|-------------|---|------|------|--------------------------------|
| t_1 | SCLK Period | 4 | 3 | $\frac{t_{osc}}{DRDY}$ Periods |
| t_2 | SCLK Pulse Width, HIGH and LOW | 200 | | ns |
| t_3 | \overline{CS} LOW to First SCLK Edge; Setup Time ⁽¹⁾ | 0 | | ns |
| t_4 | D_{IN} Valid to SCLK Edge; Setup Time | 50 | | ns |
| t_5 | Valid D_{IN} to SCLK Edge; Hold Time | 50 | | ns |
| t_6 | Delay Between Last SCLK Edge for D_{IN} and First SCLK Edge for D_{OUT} : | | | |
| | RDATA, RDATA, RREG, WREG, RRAM, WRAM | 50 | | t_{osc} Periods |
| | CSREG, CSRAMX, CSRAM | 200 | | t_{osc} Periods |
| | CSARAM, CSARAMX | 1100 | | t_{osc} Periods |
| $t_7^{(2)}$ | SCLK Edge to Valid New D_{OUT} | | 50 | ns |
| $t_8^{(2)}$ | SCLK Edge to D_{OUT} , Hold Time | 0 | | ns |
| t_9 | Last SCLK Edge to D_{OUT} Tri-State NOTE: D_{OUT} goes tri-state immediately when \overline{CS} goes HIGH. | 6 | 10 | t_{osc} Periods |
| t_{10} | \overline{CS} LOW Time After Final SCLK Edge | 0 | | ns |
| t_{11} | Final SCLK Edge of One Op Code Until First Edge SCLK of Next Command: | | | t_{osc} Periods |
| | RREG, WREG, RRAM, WRAM, CSRAMX, CSARAMX, CSRAM, CSARAM, CSREG, DSYNC, SLEEP, RDATA, RDATA, STOPC | 4 | | t_{osc} Periods |
| | CREG, CRAM | 220 | | t_{osc} Periods |
| | CREGA | 1600 | | t_{osc} Periods |
| | SELFGCAL, SELFOCAL, SYSOCAL, SYSGCAL | 7 | | \overline{DRDY} Periods |
| | SELFCAL | 14 | | \overline{DRDY} Periods |
| | RESET (Input pin, command, or SCLK pattern) | 16 | | t_{osc} Periods |
| t_{12} | | 300 | 500 | t_{osc} Periods |
| t_{13} | | 5 | | t_{osc} Periods |
| t_{14} | | 550 | | t_{osc} Periods |
| t_{15} | | 1050 | 1250 | t_{osc} Periods |
| t_{16} | Pulse Width | 4 | | t_{osc} Periods |
| t_{17} | Data Not Valid | 4 | | t_{osc} Periods |

NOTES: (1) \overline{CS} may be tied LOW. (2) Load = 20pF.

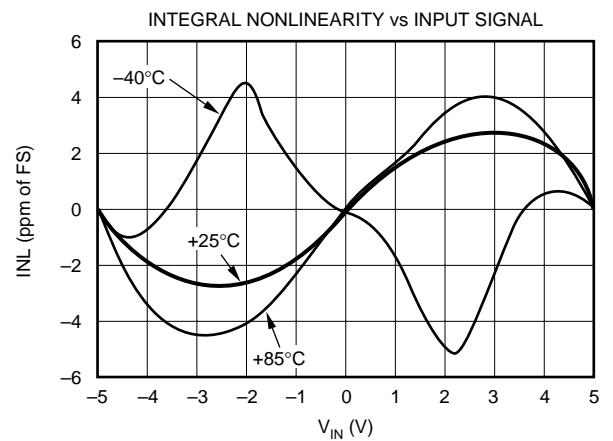
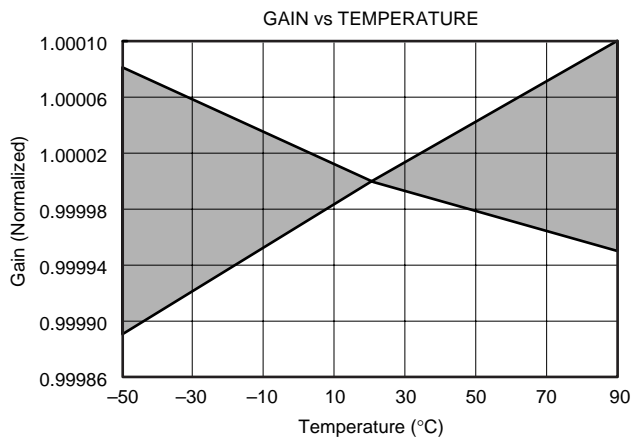
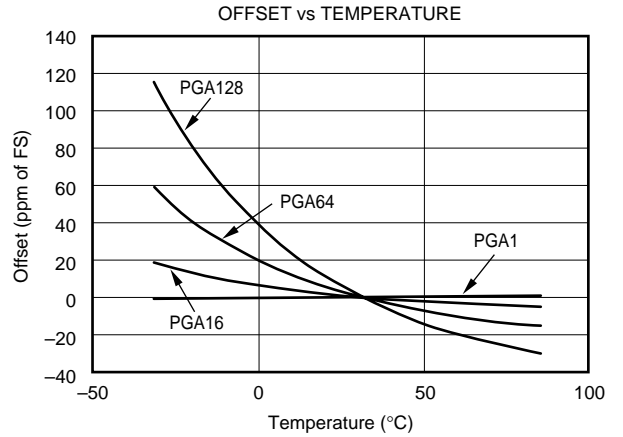
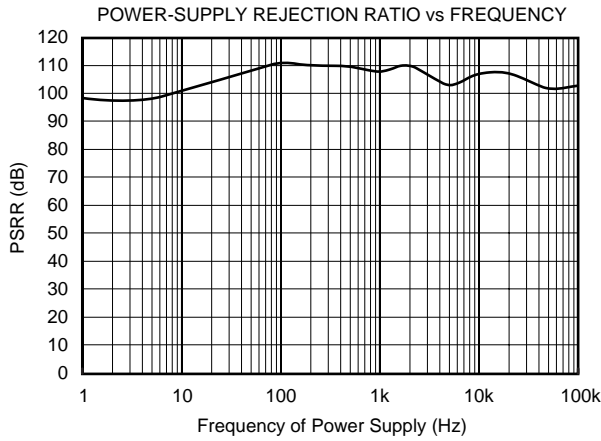
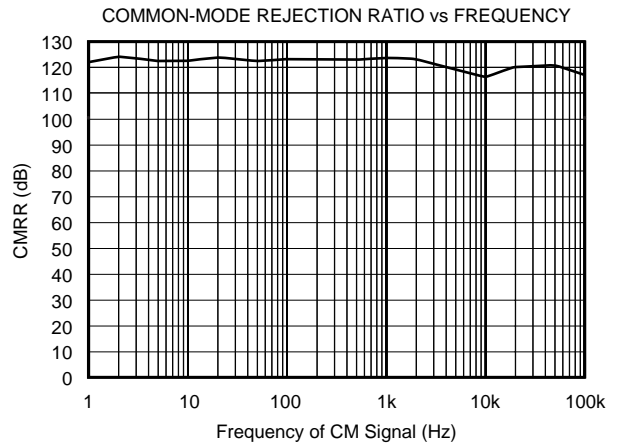
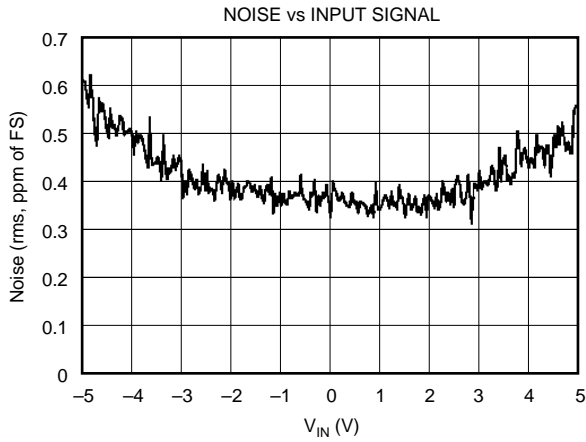
TYPICAL CHARACTERISTICS

$A_{V_{DD}} = +5V$, $DV_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $R_{DAC} = 150k\Omega$, $f_{DATA} = 10Hz$, and $V_{REF} = +2.5V$, unless otherwise specified.



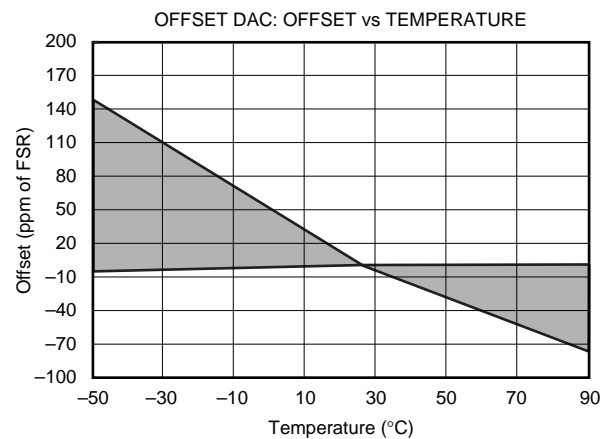
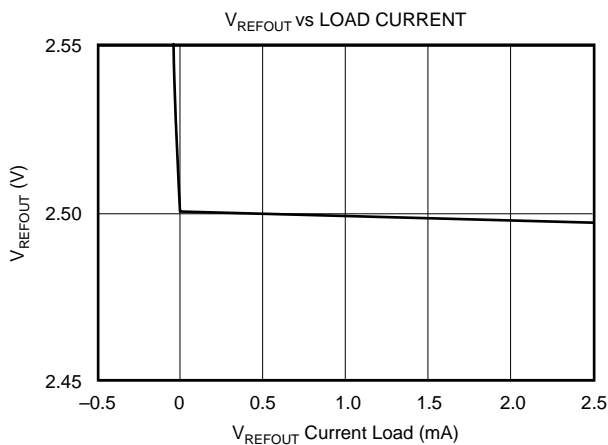
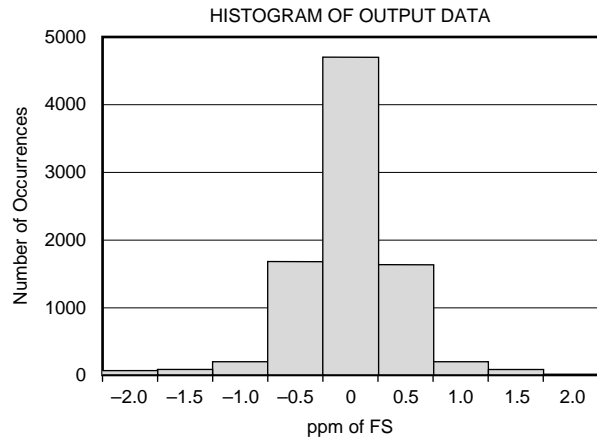
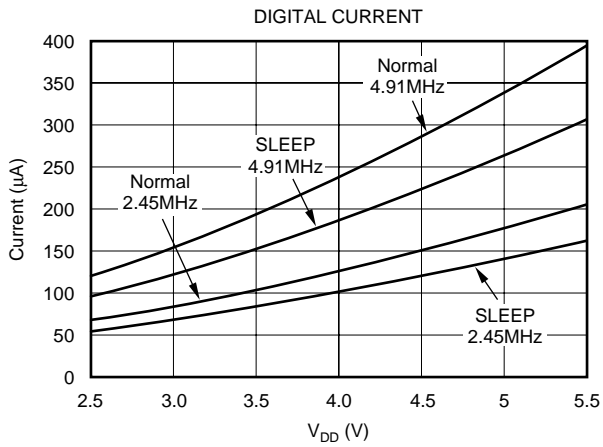
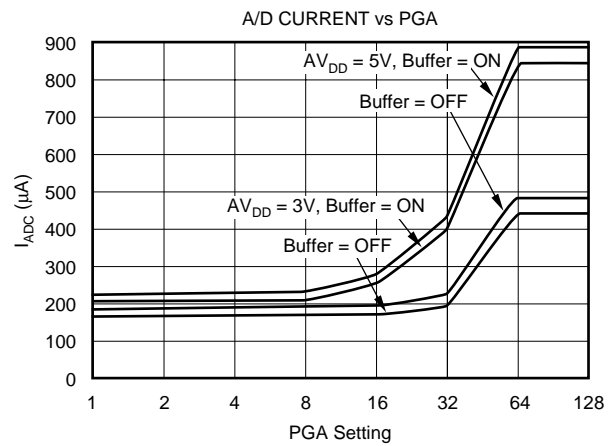
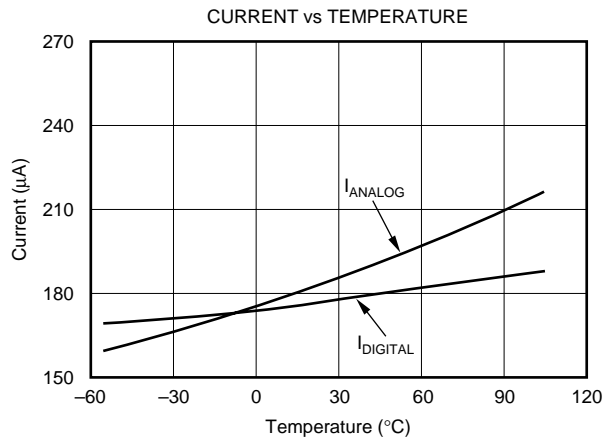
TYPICAL CHARACTERISTICS (Cont.)

$AV_{DD} = +5V$, $DV_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $R_{DAC} = 150k\Omega$, $f_{DATA} = 10Hz$, and $V_{REF} = +2.5V$, unless otherwise specified.



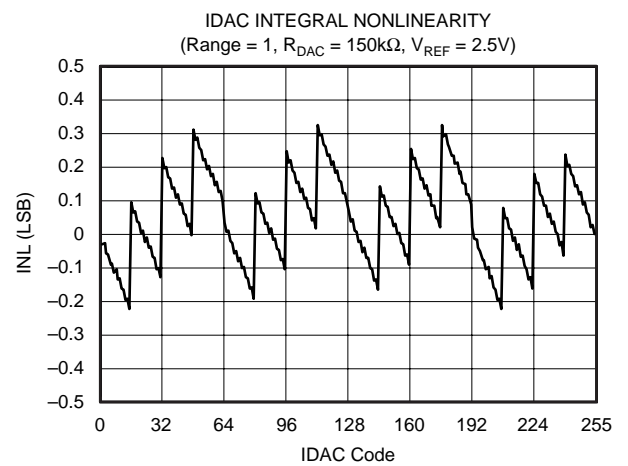
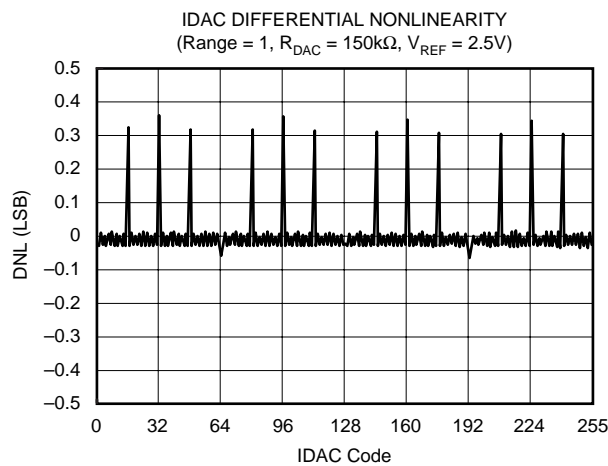
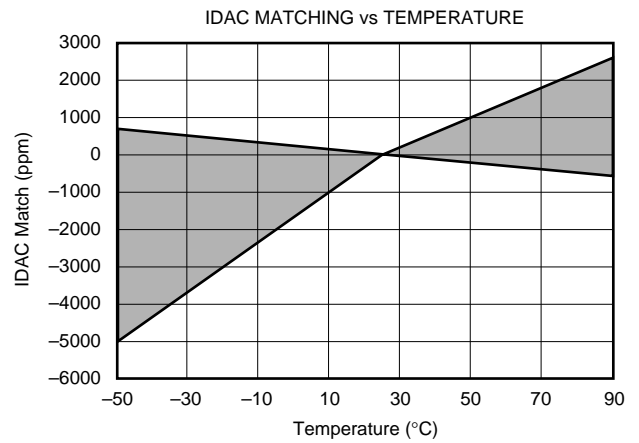
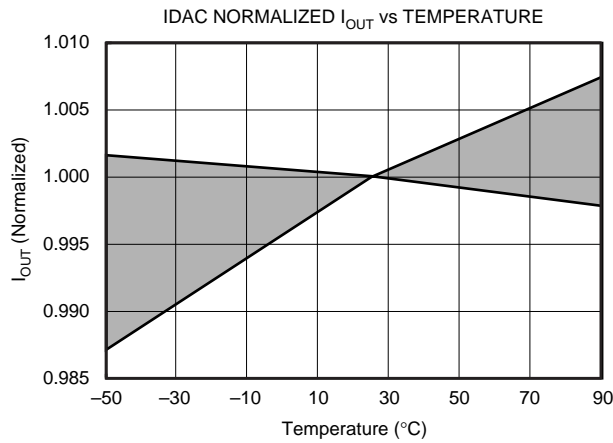
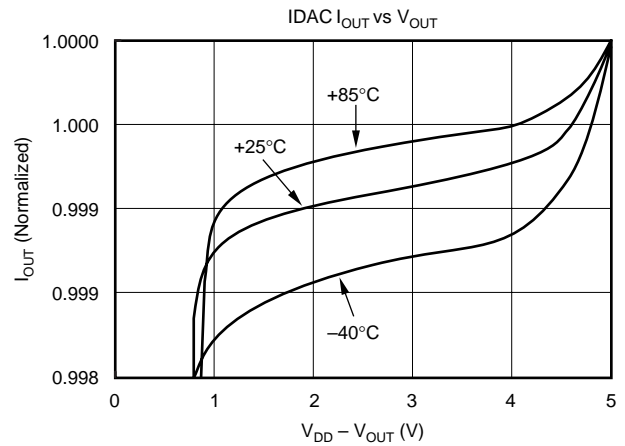
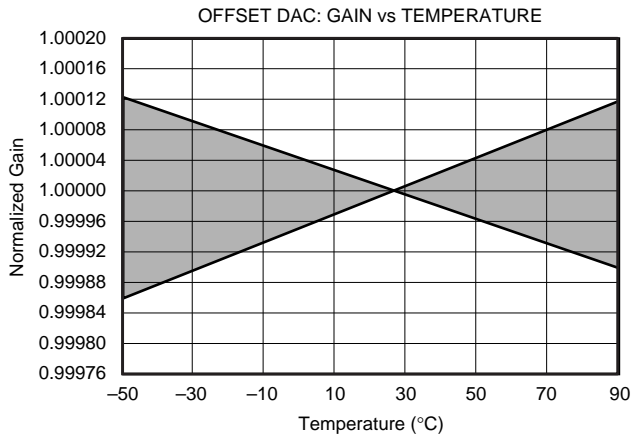
TYPICAL CHARACTERISTICS (Cont.)

$AV_{DD} = +5V$, $DV_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $R_{DAC} = 150k\Omega$, $f_{DATA} = 10Hz$, and $V_{REF} = +2.5V$, unless otherwise specified.



TYPICAL CHARACTERISTICS (Cont.)

$V_{DD} = +5V$, $DV_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $R_{DAC} = 150k\Omega$, $f_{DATA} = 10Hz$, and $V_{REF} = +2.5V$, unless otherwise specified.



OVERVIEW

INPUT MULTIPLEXER

The input multiplexer (mux) provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 1. If channel 1 is selected as the positive differential input channel, any other channel can be selected as the negative differential input channel. With this method, it is possible to have up to eight fully differential input channels.

In addition, current sources are supplied that will source or sink current to detect open or short circuits on the pins.

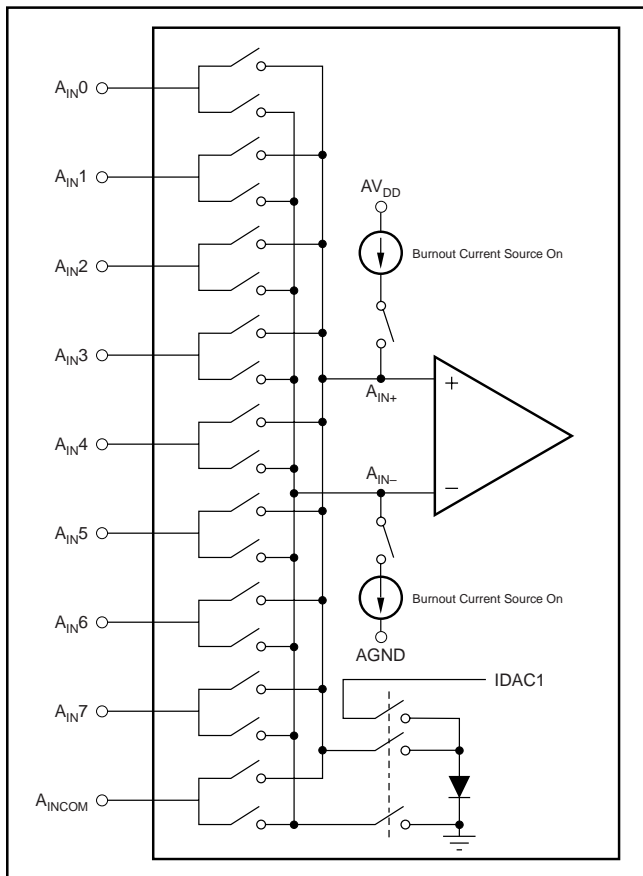


FIGURE 1. Input Multiplexer Configuration.

TEMPERATURE SENSOR

An on-chip diode provides temperature sensing capability. When the configuration register for the input MUX is set to all 1s, the diode is connected to the input of the A/D converter. All other channels are open. The anode of the diode is connected to the positive input of the A/D converter, and the cathode of the diode is connected to negative input of the A/D converter. The output of IDAC1 is connected to the anode to bias the diode and the cathode of the diode is also connected to ground to complete the circuit.

In this mode, the output of IDAC1 is also connected to the output pin, so some current may flow into an external load from IDAC1, rather than the diode. See Application Report *Measuring Temperature with the ADS1216, ADS1217, or ADS1218* (SBAA073) for more information.

BURNOUT CURRENT SOURCES

When the Burnout bit is set in the ACR configuration register, two current sources are enabled. The current source on the positive input channel sources approximately 2μA of current. The current source on the negative input channel sinks approximately 2μA. This allows for the detection of an open circuit (full-scale reading) or short circuit (0V differential reading) on the selected input differential pair.

INPUT BUFFER

The input impedance of the ADS1217 without the buffer is 10MΩ/PGA. With the buffer enabled, the input voltage range is reduced and the analog power-supply current is higher. The buffer is controlled by ANDing the state of the buffer pin with the state of the BUFFER bit in the ACR register. See Application Report *Input Currents for High-Resolution ADCs* (SBAA090) for more information.

IDAC1 AND IDAC2

The ADS1217 has two 8-bit current output DACs that can be controlled independently. The output current is set with R_{DAC} , the range select bits in the ACR register, and the 8-bit digital value in the IDAC register. The output current = $(V_{REF}/8R_{DAC}) (2^{RANGE-1}) (DAC CODE)$. With $V_{REFOUT} = 2.5V$ and $R_{DAC} = 150k\Omega$, the full-scale output can be selected to be 0.5, 1, or 2mA. The compliance voltage range is AGND to within 1V of AV_{DD} . When the internal voltage reference of the ADS1217 is used, it is the reference for the IDAC. An external reference may be used for the IDACs by disabling the internal reference and tying the external reference input to the V_{REFOUT} pin.

PGA

The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 10V full-scale range, the A/D converter can resolve to 2μV. With a PGA of 128 on a 80mV full-scale range, the A/D converter can resolve to 150nV.

PGA OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA by using the ODAC register. The ODAC (Offset DAC) register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Using the ODAC does not reduce the performance of the A/D converter. See Application Report *The Offset DAC* (SBAA077) for more information.

MODULATOR

The modulator is a single-loop, 2nd-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the external clock (f_{OSC}). The frequency division is determined by the SPEED bit in the setup register.

| SPEED BIT | f_{MOD} |
|-----------|---------------|
| 0 | $f_{OSC}/128$ |
| 1 | $f_{OSC}/256$ |

VOLTAGE REFERENCE INPUT

The ADS1217 uses a differential voltage reference input. The input signal is measured against the differential voltage $V_{REF} \equiv (V_{REF+}) - (V_{REF-})$. For $AV_{DD} = 5V$, V_{REF} is typically 2.5V. For $AV_{DD} = 3V$, V_{REF} is typically 1.25V. Due to the sampling nature of the modulator, the reference input current increases with higher modulator clock frequency (f_{MOD}) and higher PGA settings.

ON-CHIP VOLTAGE REFERENCE

A selectable voltage reference (1.25V or 2.5V) is available for supplying the voltage reference input. To use, connect V_{REF-} to AGND and V_{REF+} to V_{REFOUT} . The enabling and voltage selection are controlled through bits REF EN and REF HI in the setup register. The 2.5V reference requires $AV_{DD} = 5V$. When using the on-chip voltage reference, the V_{REFOUT} pin should be bypassed with a 0.1 μ F capacitor to AGND.

V_{RCAP} PIN

This pin provides a bypass cap for noise filtering on internal V_{REF} circuitry only. As this is a sensitive pin, place the capacitor as close as possible and avoid any resistive loading. The recommended capacitor is a 0.001 μ F ceramic cap. If an external V_{REF} is used, this pin can be left unconnected.

CLOCK GENERATOR

The clock source for the ADS1217 can be provided from a crystal, oscillator, or external clock. When the clock source is a crystal, external capacitors must be provided to ensure start-up and a stable clock frequency; see Figure 2 and Table I.

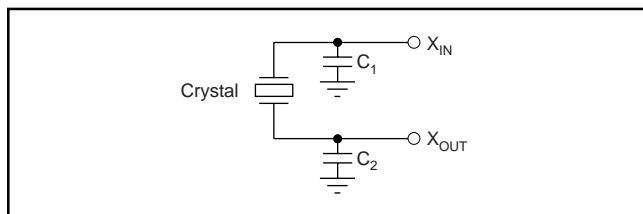


FIGURE 2. Crystal Connection.

| CLOCK SOURCE | FREQUENCY | C ₁ | C ₂ | PART NUMBER |
|--------------|-----------|----------------|----------------|---------------------|
| Crystal | 2.4576 | 0-20pF | 0-20pF | ECS, ECSD 2.45 - 32 |
| Crystal | 4.9152 | 0-20pF | 0-20pF | ECS, ECLS 4.91 |
| Crystal | 4.9152 | 0-20pF | 0-20pF | ECS, ECSD 4.91 |
| Crystal | 4.9152 | 0-20pF | 0-20pF | CTS, MP 042 4M9182 |

TABLE I. Typical Clock Sources.

CALIBRATION

The offset and gain errors in the ADS1217, or the complete system, can be reduced with calibration. Internal calibration of the ADS1217 is called self calibration. This is handled with three commands. One command does both offset and gain calibration. There is also a gain calibration command and an offset calibration command. Each calibration process takes seven t_{DATA} periods to complete. It takes 14 t_{DATA} periods to

complete both an offset and gain calibration. Self-gain calibration is optimized for PGA gains less than 8. When using higher gains, system gain calibration is recommended.

For system calibration, the appropriate signal must be applied to the inputs. The system offset command requires a "zero" differential input signal. It then computes an offset that will nullify offset in the system. The system gain command requires a positive "full-scale" differential input signal. It then computes a value to nullify gain errors in the system. Each of these calibrations will take seven t_{DATA} periods to complete.

Calibration must be performed after power on, a change in decimation ratio, or a change of the PGA. For operation with a reference voltage greater than $(AV_{DD} - 1.5V)$, the buffer must also be turned off during calibration.

At the completion of calibration, the \overline{DRDY} signal goes LOW, which indicates the calibration is finished and valid data is available. See Application Report *Calibration Routine and Register Value Generation for the ADS121x Series* (SBAA099) for more information.

DIGITAL FILTER

The Digital Filter can use either the fast settling, sinc², or sinc³ filter, as shown in Figure 3. In addition, the Auto mode changes the sinc filter after the input channel or PGA is changed. When switching to a new channel, it will use the fast settling filter; It will then use the sinc² followed by the sinc³ filter. This combines the low-noise advantage of the sinc³ filter with the quick response of the fast settling time filter. See Figure 4 for the frequency response of each filter.

When using the fast setting filter, select a decimation value set by the DEC0 and M/DEC1 registers that is evenly divisible by four for the best gain accuracy. For example, choose 260 rather than 261.

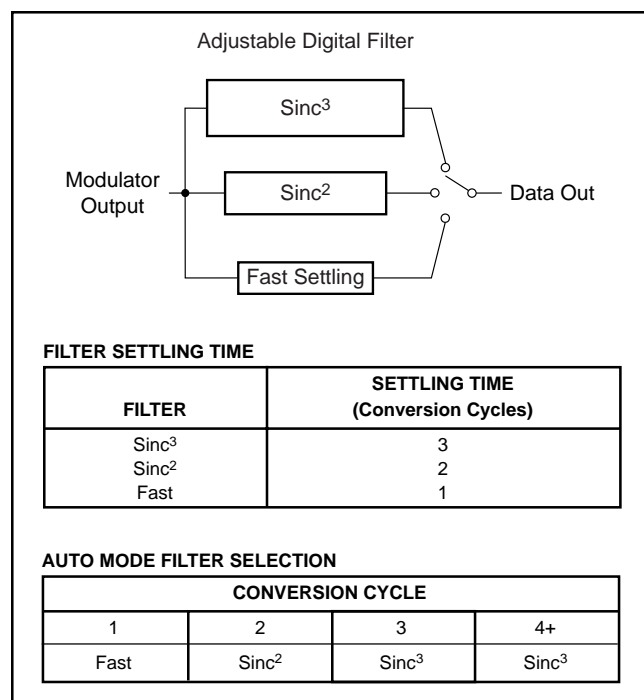


FIGURE 3. Filter Step Responses.

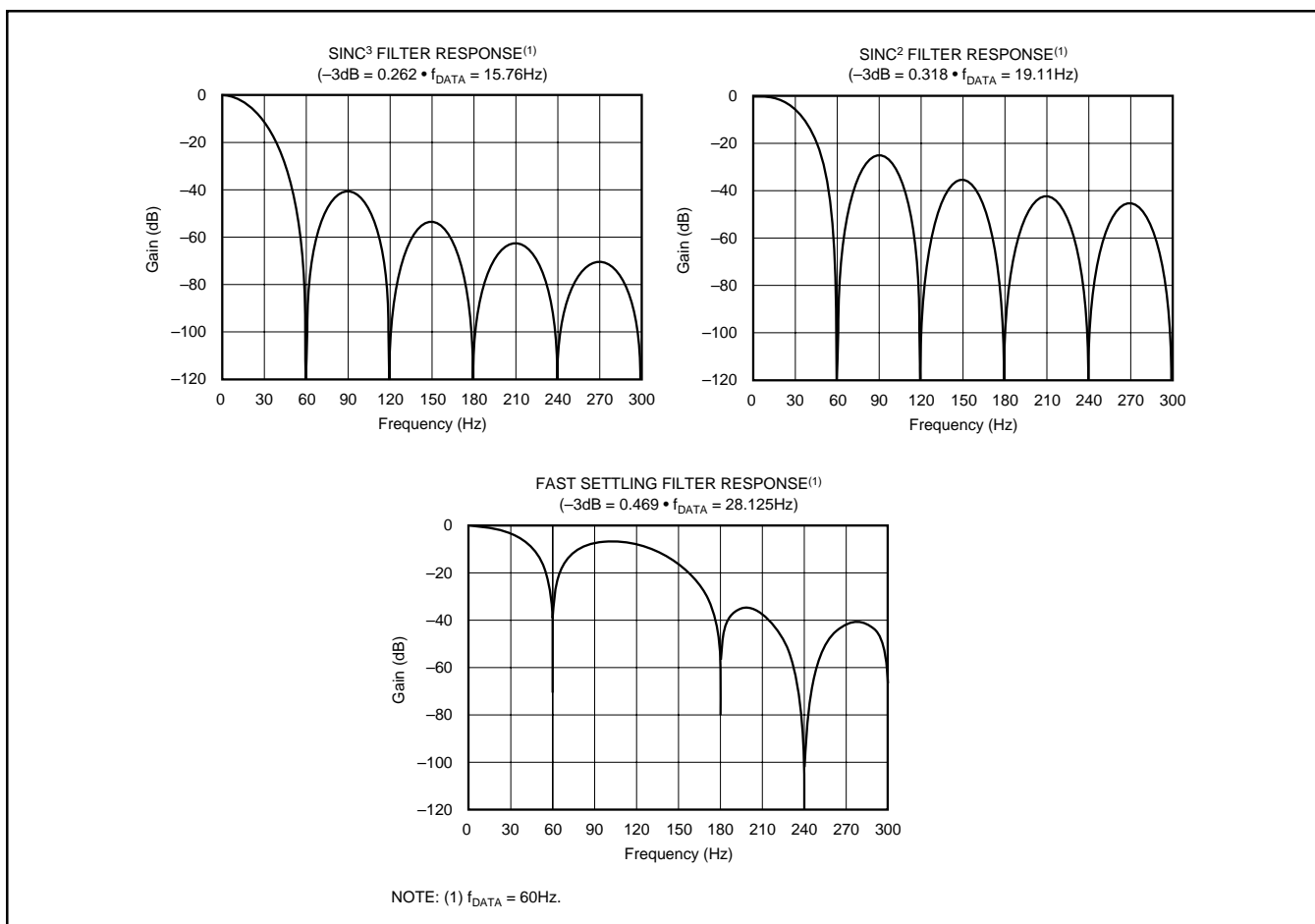


FIGURE 4. Filter Frequency Responses.

DIGITAL I/O INTERFACE

The ADS1217 has eight pins dedicated for digital I/O. The default power-up condition for the digital I/O pins are as inputs. All of the digital I/O pins are individually configurable as inputs or outputs. They are configured through the DIR control register. The DIR register defines whether the pin is an input or output, and the DIO register defines the state of the digital output. When the digital I/O are configured as inputs, DIO is used to read the state of the pin. If the digital I/O are not used, either 1) configure as outputs; or, 2) leave as inputs and tie to ground, this prevents excess power dissipation.

SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) allows a controller to communicate synchronously with the ADS1217. The ADS1217 operates in slave only mode.

Chip Select (\overline{CS})

The chip select (\overline{CS}) input of the ADS1217 must be externally asserted before a master device can exchange data with the ADS1217. \overline{CS} must be LOW for the duration of the transaction. \overline{CS} can be tied low.

Serial Clock (SCLK)

SCLK, a Schmitt Trigger input, clocks data transfer on the D_{IN} input and D_{OUT} output. When transferring data to or from the ADS1217, multiple bits of data may be transferred back-to-

back with no delay in SCLKs or toggling of \overline{CS} . Make sure to avoid glitches on SCLK as they can cause extra shifting of the data.

Polarity (POL)

The serial clock polarity is specified by the POL input. When SCLK is active HIGH, set POL HIGH. When SCLK is active LOW, set POL LOW.

DATA READY

The \overline{DRDY} output is used as a status signal to indicate when data is ready to be read from the ADS1217. \overline{DRDY} goes LOW when new data is available. It is reset HIGH when a read operation from the data register is complete. It also goes HIGH prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

DSYNC OPERATION

DSYNC is used to provide for synchronization of the A/D conversion with an external event. Synchronization can be achieved either through the \overline{DSYNC} pin or the DSYNC command. When the \overline{DSYNC} pin is used, the filter counter is reset on the falling edge of \overline{DSYNC} . The modulator is held in reset until \overline{DSYNC} is taken HIGH. Synchronization occurs on the next rising edge of the system clock after \overline{DSYNC} is taken HIGH.

When the DSYNC command is sent, the filter counter is reset on the edge of the last SCLK on the DSYNC command. The modulator is held in reset until the next edge of SCLK is detected. Synchronization occurs on the next rising edge of the system clock after the first SCLK after the DSYNC command. After a DSYNC operation, $\overline{\text{DRDY}}$ is held HIGH until valid data is ready.

RESET

There are three methods to reset the ADS1217: the $\overline{\text{RESET}}$ input, the RESET command, and a special SCLK input pattern. When using the $\overline{\text{RESET}}$ input, take it LOW to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the $\overline{\text{RESET}}$ input back high. Also, avoid glitches on the $\overline{\text{RESET}}$ input as these may cause accidental resets. The RESET command takes effect after all 8 bits have been shifted into DIN. Afterwards, the reset releases automatically. The ADS1217 can also be reset with a special pattern on SCLK, see the Timing Diagram. Reset occurs on the falling edge of the last SCLK edge in the pattern (for POL = 0). Afterwards, the reset releases automatically.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry was designed to accommodate digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically.

MEMORY

Two types of memory are used on the ADS1217: registers and RAM. 16 registers directly control the various functions (PGA, DAC value, Decimation Ratio, etc.) and can be directly read or written. Collectively, the registers contain all the information needed to configure the part, such as data format, mux settings, calibration settings, decimation ratio, etc. Additional registers, such as output data, are accessed through dedicated instructions.

REGISTER BANK TOPOLOGY

The operation of the device is set up through individual registers. The set of the 16 registers required to configure the device is referred to as a Register Bank, as shown in Figure 5.

Reads and Writes to Registers and RAM occur on a byte basis. However, copies between registers and RAM occurs on a bank basis. The RAM is independent of the Registers; that is, the RAM can be used as general-purpose RAM.

The ADS1217 supports any combination of eight analog inputs. With this flexibility, the device could easily support eight unique configurations—one per input channel. In order to facilitate this type of usage, eight separate register banks are available. Therefore, each configuration could be written once and recalled as needed without having to serially retransmit all the configuration data. Checksum commands are also included, which can be used to verify the integrity of RAM.

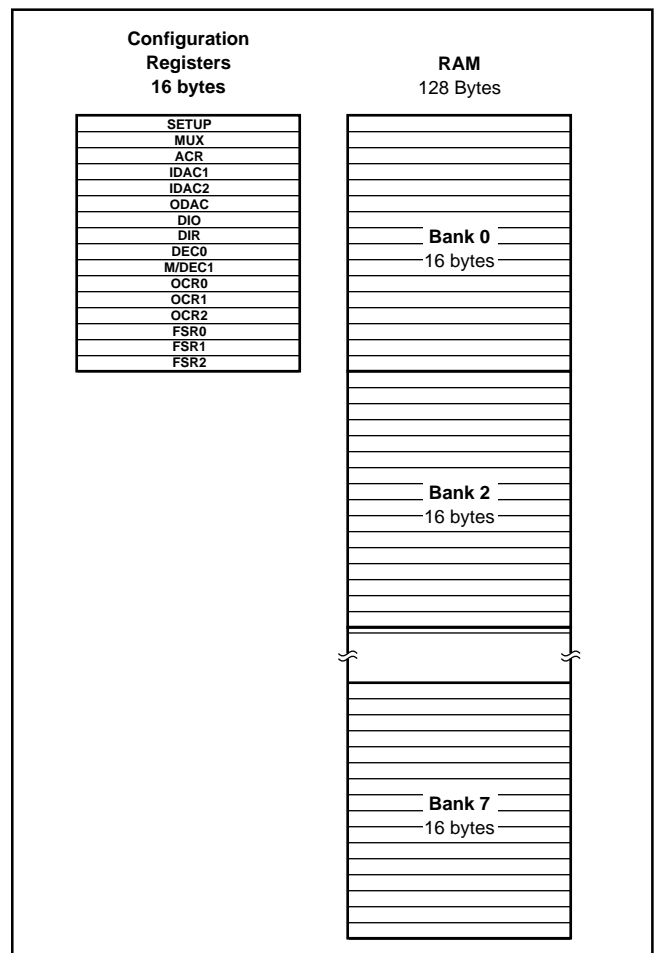


FIGURE 5. Memory Organization.

The RAM provides eight “banks”, with a bank consisting of 16 bytes. The total size of the RAM is 128 bytes. Copies between the registers and RAM are performed on a bank basis. Also, the RAM can be directly read or written through the serial interface on power-up. The banks allow separate storage of settings for each input.

The RAM address space is linear, therefore accessing RAM is done using an auto-incrementing pointer. Access to RAM in the entire memory map can be done consecutively without having to address each bank individually. For example, if you were currently accessing bank 0 at offset $0F_H$ (the last location of bank 0), the next access would be bank 1 and offset 00_H . Any access after bank 7 and offset $0F_H$ will wrap around to bank 0 and Offset 00_H .

Although the Register Bank memory is linear, the concept of addressing the device can also be thought of in terms of bank and offset addressing. Looking at linear and bank addressing syntax, we have the following comparison: in the linear memory map, the address 14_H is equivalent to bank 1 and offset 04_H . Simply stated, the most significant four bits represent the bank, and the least significant four bits represent the offset. The offset is equivalent to the register address for that bank of memory.

REGISTER MAP

| ADDRESS | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-----------------|----------|---------|---------|---------|---------|----------|---------|---------|-----------|
| 00 _H | SETUP | ID | ID | ID | SPEED | REF EN | REF HI | BUF EN | BIT ORDER |
| 01 _H | MUX | PSEL3 | PSEL2 | PSEL1 | PSEL0 | NSEL3 | NSEL2 | NSEL1 | NSEL0 |
| 02 _H | ACR | BOCS | IDAC2R1 | IDAC2R0 | IDAC1R1 | IDAC1R0 | PGA2 | PGA1 | PGA0 |
| 03 _H | IDAC1 | IDAC1_7 | IDAC1_6 | IDAC1_5 | IDAC1_4 | IDAC1_3 | IDAC1_2 | IDAC1_1 | IDAC1_0 |
| 04 _H | IDAC2 | IDAC2_7 | IDAC2_6 | IDAC2_5 | IDAC2_4 | IDAC2_3 | IDAC2_2 | IDAC2_1 | IDAC2_0 |
| 05 _H | ODAC | SIGN | OSET_6 | OSET_5 | OSET_4 | OSET_3 | OSET_2 | OSET_1 | OSET_0 |
| 06 _H | DIO | DIO_7 | DIO_6 | DIO_5 | DIO_4 | DIO_3 | DIO_2 | DIO_1 | DIO_0 |
| 07 _H | DIR | DIR_7 | DIR_6 | DIR_5 | DIR_4 | DIR_3 | DIR_2 | DIR_1 | DIR_0 |
| 08 _H | DEC0 | DEC07 | DEC06 | DEC05 | DEC04 | DEC03 | DEC02 | DEC01 | DEC00 |
| 09 _H | M/DEC1 | DRDY | U/B | SMODE1 | SMODE0 | Reserved | DEC10 | DEC09 | DEC08 |
| 0A _H | OCR0 | OCR07 | OCR06 | OCR05 | OCR04 | OCR03 | OCR02 | OCR01 | OCR00 |
| 0B _H | OCR1 | OCR15 | OCR14 | OCR13 | OCR12 | OCR11 | OCR10 | OCR09 | OCR08 |
| 0C _H | OCR2 | OCR23 | OCR22 | OCR21 | OCR20 | OCR19 | OCR18 | OCR17 | OCR16 |
| 0D _H | FSR0 | FSR07 | FSR06 | FSR05 | FSR04 | FSR03 | FSR02 | FSR01 | FSR00 |
| 0E _H | FSR1 | FSR15 | FSR14 | FSR13 | FSR12 | FSR11 | FSR10 | FSR09 | FSR08 |
| 0F _H | FSR2 | FSR23 | FSR22 | FSR21 | FSR20 | FSR19 | FSR18 | FSR17 | FSR16 |

TABLE II. Registers.

DETAILED REGISTER DEFINITIONS

SETUP (Address 00_H) Setup Register

Reset Value = iii01110

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|--------|--------|--------|-----------|
| ID | ID | ID | SPEED | REF EN | REF HI | BUF EN | BIT ORDER |

bit 7-5 Factory Programmed Bits

bit 4 SPEED: Modulator Clock Speed

0 : $f_{MOD} = f_{OSC}/128$ (default)

1 : $f_{MOD} = f_{OSC}/256$

bit 3 REF EN: Internal Voltage Reference Enable

0 = Internal Voltage Reference Disabled

1 = Internal Voltage Reference Enabled (default)

bit 2 REF HI: Internal Reference Voltage Select

0 = Internal Reference Voltage = 1.25V

1 = Internal Reference Voltage = 2.5V (default)

bit 1 BUF EN: Buffer Enable

0 = Buffer Disabled

1 = Buffer Enabled (default)

bit 0 BIT ORDER: Set Order Bits are Transmitted

0 = Most Significant Bit Transmitted First (default)

1 = Least Significant Bit Transmitted First

Data is always shifted into the part most significant bit first. Data is always shifted out of the part most significant byte first. This configuration bit only controls the bit order within the byte of data that is shifted out.

MUX (Address 01_H) Multiplexer Control Register

Reset Value = 01_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PSEL3 | PSEL2 | PSEL1 | PSEL0 | NSEL3 | NSEL2 | NSEL1 | NSEL0 |

bit 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select

0000 = AIN0 (default)

0001 = AIN1

0010 = AIN2

0011 = AIN3

0100 = AIN4

0101 = AIN5

0110 = AIN6

0111 = AIN7

1xxx = AINCOM (except when all bits are 1s)

1111 = Temperature Sensor Diode

bit 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select

0000 = AIN0

0001 = AIN1 (default)

0010 = AIN2

0011 = AIN3

0100 = AIN4

0101 = AIN5

0110 = AIN6

0111 = AIN7

1xxx = AINCOM (except when all bits are 1s)

1111 = Temperature Sensor Diode

ACR (Address 02_H) Analog Control RegisterReset Value = 00_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|---------|---------|---------|---------|-------|-------|-------|
| BOCS | IDAC2R1 | IDAC2R0 | IDAC1R1 | IDAC1R0 | PGA2 | PGA1 | PGA0 |

bit 7 BOCS: Burnout Current Source
0 = Disabled (default)
1 = Enabled

$$\text{IDAC Current} = \left(\frac{V_{\text{REF}}}{8R_{\text{DAC}}} \right) \left(2^{\text{RANGE}-1} \right) (\text{DAC Code})$$

bit 6-5 IDAC2R1: IDAC2R0: Full-Scale Range Select for IDAC2

00 = Off (default)
01 = Range 1
10 = Range 2
11 = Range 3

bit 4-3 IDAC1R1: IDAC1R0: Full-Scale Range Select for IDAC1

00 = Off (default)
01 = Range 1
10 = Range 2
11 = Range 3

bit 2-0 PGA2: PGA1: PGA0: Programmable Gain Amplifier Gain Selection

000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

IDAC1 (Address 03_H) Current DAC 1Reset Value = 00_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| IDAC1_7 | IDAC1_6 | IDAC1_5 | IDAC1_4 | IDAC1_3 | IDAC1_2 | IDAC1_1 | IDAC1_0 |

The DAC code bits set the output of DAC1 from 0 to full-scale. The value of the full-scale current is set by this Byte, V_{REF} , R_{DAC} , and the DAC1 range bits in the ACR register.

IDAC2 (Address 04_H) Current DAC 2Reset Value = 00_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| IDAC2_7 | IDAC2_6 | IDAC2_5 | IDAC2_4 | IDAC1_3 | IDAC1_2 | IDAC1_1 | IDAC1_0 |

The DAC code bits set the output of DAC2 from 0 to full-scale. The value of the full-scale current is set by this Byte, V_{REF} , R_{DAC} , and the DAC2 range bits in the ACR register.

ODAC (Address 05_H) Offset DAC SettingReset Value = 00_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SIGN | OSET6 | OSET5 | OSET4 | OSET3 | OSET2 | OSET1 | OSET0 |

bit 7 Offset Sign
0 = Positive
1 = Negative

$$\text{bit 6-0 Offset} = \frac{V_{\text{REF}}}{\text{PGA}} \cdot \left(\frac{\text{Code}}{127} \right)$$

NOTE: The offset must be used after calibration or the calibration will notify the effects.

DIO (Address 06_H) Digital I/OReset Value = 00_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DIO7 | DIO6 | DIO5 | DIO4 | DIO3 | DIO2 | DIO1 | DIO0 |

A value written to this register will appear on the digital I/O pins if the pin is configured as an output in the DIR register. Reading this register will return the value of the digital I/O pins.

DIR (Address 07_H) Direction control for digital I/OReset Value = FF_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DIR7 | DIR6 | DIR5 | DIR4 | DIR3 | DIR2 | DIR1 | DIR0 |

Each bit controls whether the Digital I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

DEC0 (Address 08_H) Decimation Register
(Least Significant 8 bits)Reset Value = 80_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DEC07 | DEC06 | DEC05 | DEC04 | DEC03 | DEC02 | DEC01 | DEC00 |

The decimation value is defined with 11 bits for a range of 20 to 2047. This register is the least significant 8 bits. The 3 most significant bits are contained in the M/DEC1 register. The default data rate is 10Hz with a 2.4576MHz crystal.

M/DEC1 (Address 09_H) Mode and Decimation RegisterReset Value = 07_H

| | | | | | | | |
|-------|-------|--------|--------|----------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| DRDY | U/B | SMODE1 | SMODE0 | Reserved | DEC10 | DEC09 | DEC08 |

bit 7 DRDY: Data Ready (Read Only) _____
This bit duplicates the state of the DRDY pin.

bit 6 U/B: Data Format
0 = Bipolar (default)
1 = Unipolar

| U/B | ANALOG INPUT | DIGITAL OUTPUT |
|-----|--------------|----------------|
| 0 | +FS | 0x7FFFFFFF |
| | Zero | 0x000000 |
| | -FS | 0x800000 |
| 1 | +FS | 0xFFFFFFFF |
| | Zero | 0x000000 |
| | -FS | 0x000000 |

bit 5-4 SMODE1: SMODE0: Settling Mode
00 = Auto (default)
01 = Fast Settling filter
10 = Sinc² filter
11 = Sinc³ filter

bit 2-0 DEC10: DEC09: DEC08: Most Significant Bits of the Decimation Value

OCR0 (Address 0A_H) Offset Calibration Coefficient (Least Significant Byte)Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| OCR07 | OCR06 | OCR05 | OCR04 | OCR03 | OCR02 | OCR01 | OCR00 |

OCR1 (Address 0B_H) Offset Calibration Coefficient (Middle Byte)Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| OCR15 | OCR14 | OCR13 | OCR12 | OCR11 | OCR10 | OCR09 | OCR08 |

OCR2 (Address 0C_H) Offset Calibration Coefficient

(Most Significant Byte)

Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| OCR23 | OCR22 | OCR21 | OCR20 | OCR19 | OCR18 | OCR17 | OCR16 |

FSR0 (Address 0D_H) Full-Scale Register

(Least Significant Byte)

Reset Value = 24_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| FSR07 | FSR06 | FSR05 | FSR04 | FSR03 | FSR02 | FSR01 | FSR00 |

FSR1 (Address 0E_H) Full-Scale Register

(Middle Byte)

Reset Value = 90_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| FSR15 | FSR14 | FSR13 | FSR12 | FSR11 | FSR10 | FSR09 | FSR08 |

FSR2 (Address 0F_H) Full-Scale Register

(Most Significant Byte)

Reset Value = 67_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| FSR23 | FSR22 | FSR21 | FSR20 | FSR19 | FSR18 | FSR17 | FSR16 |

COMMAND DEFINITIONS

The commands listed below control the operation of the ADS1217. Some of the commands are stand-alone commands (e.g., RESET) while others require additional bytes (e.g., WREG requires command, count, and the data bytes). Commands that output data require a minimum of four f_{OSC} cycles before the data is ready (e.g., RDATA).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

a = RAM bank address (0 to 7)

| COMMANDS | DESCRIPTION | COMMAND BYTE | 2ND COMMAND BYTE |
|----------|-----------------------------------|-------------------------------------|--------------------------|
| RDATA | Read Data | 0000 0001 (01 _H) | — |
| RDATA C | Read Data Continuously | 0000 0011 (03 _H) | — |
| STOPC | Stop Read Data Continuously | 0000 1111 (0F _H) | — |
| RREG | Read from REG Bank <i>rrrr</i> | 0001 <i>rrrr</i> (1x _H) | xxxx_nnnn (# of reg-1) |
| RRAM | Read from RAM Bank <i>aaa</i> | 0010 0aaa (2x _H) | xnnn_nnnn (# of bytes-1) |
| CREG | Copy REGs to RAM Bank <i>aaa</i> | 0100 0aaa (4x _H) | — |
| CREGA | Copy REGS to all RAM Banks | 0100 1000 (48 _H) | — |
| WREG | Write to REG <i>rrrr</i> | 0101 <i>rrrr</i> (5x _H) | xxxx_nnnn (# of reg-1) |
| WRAM | Write to RAM Bank <i>aaa</i> | 0110 0aaa (6x _H) | xnnn_nnnn (# of bytes-1) |
| CRAM | Copy RAM Bank <i>aaa</i> to REG | 1100 0aaa (Cx _H) | — |
| CSRAMX | Calc RAM Bank <i>aaa</i> Checksum | 1101 0aaa (Dx _H) | — |
| CSARAMX | Calc all RAM Bank Checksum | 1101 1000 (D8 _H) | — |
| CSREG | Calc REG Checksum | 1101 1111 (DF _H) | — |
| CSRAM | Calc RAM Bank <i>aaa</i> Checksum | 1110 0aaa (Ex _H) | — |
| CSARAM | Calc all RAM Banks Checksum | 1110 1000 (E8 _H) | — |
| SELF CAL | Self Cal Offset and Gain | 1111 0000 (F0 _H) | — |
| SELF CAL | Self Cal Offset | 1111 0001 (F1 _H) | — |
| SELF CAL | Self Cal Gain | 1111 0010 (F2 _H) | — |
| SYS CAL | Sys Cal Offset | 1111 0011 (F3 _H) | — |
| SYS CAL | Sys Cal Gain | 1111 0100 (F4 _H) | — |
| WAKEUP | Wake Up From Sleep Mode | 1111 1011 (FB _H) | — |
| DSYNC | Sync DRDY | 1111 1100 (FC _H) | — |
| SLEEP | Put in Sleep Mode | 1111 1101 (FD _H) | — |
| RESET | Reset to Power-Up Values | 1111 1110 (FE _H) | — |

NOTE: (1) The data received by the A/D converter is always MSB First, the data out format is set by the BIT ORDER bit in ACR reg.

TABLE III. Command Summary.

RDATA

Read Data

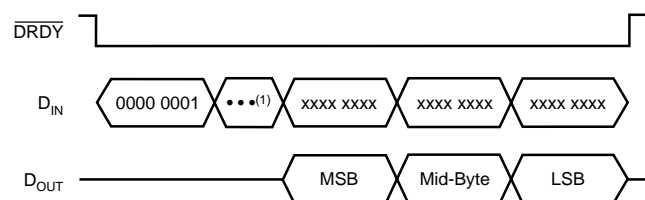
Description: Read a single 24-bit ADC conversion result. On completion of read back, DRDY goes HIGH.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



RDATA C

Read Data Continuous

Description: Read Data Continuous mode enables the continuous output of new data on each DRDY. This command eliminates the need to send the Read Data Command on each DRDY. This mode may be terminated by either the STOP Read Continuous command or the RESET command.

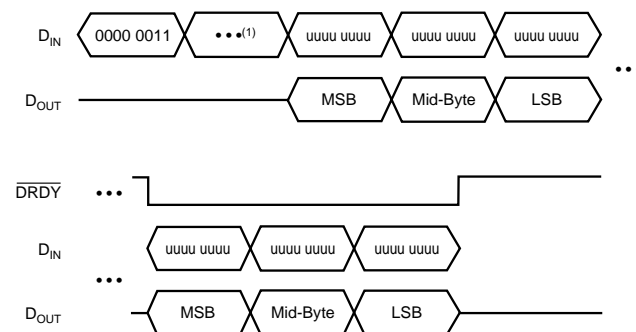
Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence:

Command terminated when *uuuu uuuu* equals STOPC or RESET.



NOTE: (1) For wait time, refer to timing specification.

STOPC

Stop Continuous

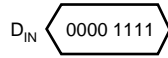
Description: Ends the continuous data output mode.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG

Read from Registers

Description: Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte. If the count exceeds the remaining registers, the addresses will wrap back to the beginning.

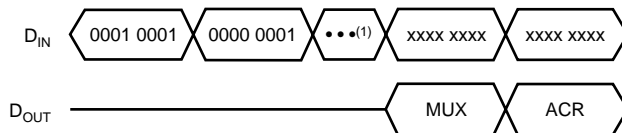
Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence:

Read Two Registers Starting from Register 01_H (MUX)



RRAM

Read from RAM

Description: Up to 128 bytes can be read from RAM starting at the bank specified in the op code. All reads start at the address for the beginning of the RAM bank. The number of bytes to read will be one plus the value of the second byte.

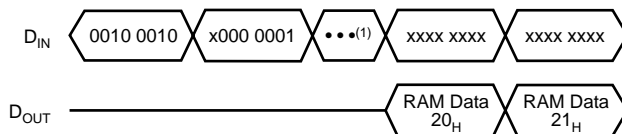
Operands: a, n

Bytes: 2

Encoding: 0010 0aaa xnnn nnnn

Data Transfer Sequence:

Read Two RAM Locations Starting from 20_H



CREG

Copy Registers to RAM Bank

Description: Copy the 16 control registers to the RAM bank specified in the op code. Refer to timing specifications for command execution time.

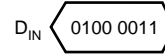
Operands: a

Bytes: 1

Encoding: 0100 0aaa

Data Transfer Sequence:

Copy Register Values to RAM Bank 3



CREGA

Copy Registers to All RAM Banks

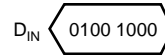
Description: Duplicate the 16 control registers to all the RAM banks. Refer to timing specifications for command execution time.

Operands: None

Bytes: 1

Encoding: 0100 1000

Data Transfer Sequence:



WREG

Write to Register

Description: Write to the registers starting with the register specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

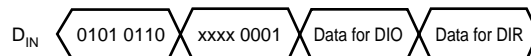
Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence:

Write Two Registers Starting from 06_H (DIO)



NOTE: (1) For wait time, refer to timing specification.

WRAM

Write to RAM

Description: Write up to 128 RAM locations starting at the beginning of the RAM bank specified as part of the instruction. The number of bytes written to RAM is one plus the value of the second byte.

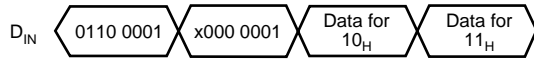
Operands: a, n

Bytes: 2

Encoding: 0110 0aaa xnnn nnnn

Data Transfer Sequence:

Write to Two RAM Locations starting from 10_H



CRAM

Copy RAM Bank to Registers

Description: Copy the selected RAM Bank to the Configuration Registers. This will overwrite all of the registers with the data from the RAM bank.

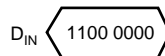
Operands: a

Bytes: 1

Encoding: 1100 0aaa

Data Transfer Sequence:

Copy RAM Bank 0 to the Registers



CSRAMX

Calculate RAM Bank Checksum

Description: Calculate the checksum of the selected RAM Bank. The checksum is calculated as a sum of all the bytes with the carry ignored. The ID, $\overline{\text{DRDY}}$, and DIO bits are masked so they are not included in the checksum.

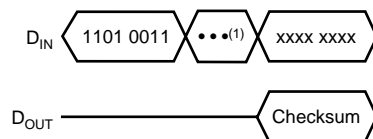
Operands: a

Bytes: 1

Encoding: 1101 0aaa

Data Transfer Sequence:

Calculate Checksum for RAM Bank 3



CSARAMX

Calculate the Checksum for all RAM Banks

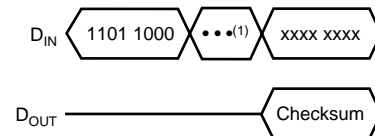
Description: Calculate the checksum of all RAM Banks. The checksum is calculated as a sum of all the bytes with the carry ignored. The ID, $\overline{\text{DRDY}}$, and DIO bits are masked so they are not included in the checksum.

Operands: None

Bytes: 1

Encoding: 1101 1000

Data Transfer Sequence:



CSREG

Calculate the Checksum of Registers

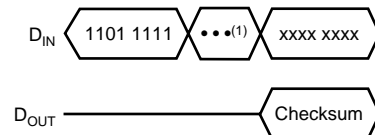
Description: Calculate the checksum of all the registers. The checksum is calculated as a sum of all the bytes with the carry ignored. The ID, $\overline{\text{DRDY}}$ and DIO bits are masked so they are not included in the checksum.

Operands: None

Bytes: 1

Encoding: 1101 1111

Data Transfer Sequence:



CSRAM

Calculate RAM Bank Checksum

Description: Calculate the checksum of the selected RAM Bank. The checksum is calculated as a sum of all the bytes with the carry ignored. All bits are included in the checksum calculation, there is no masking of bits.

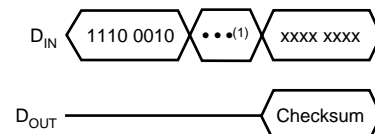
Operands: a

Bytes: 1

Encoding: 1110 0aaa

Data Transfer Sequence:

Calculate Checksum for RAM Bank 2



NOTE: (1) For wait time, refer to timing specification.

CSARAM

Calculate Checksum for all RAM Banks

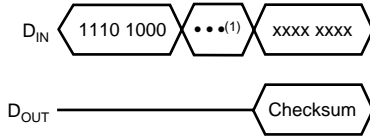
Description: Calculate the checksum of all RAM Banks. The checksum is calculated as a sum of all the bytes with the carry ignored. All bits are included in the checksum calculation, there is no masking of bits.

Operands: None

Bytes: 1

Encoding: 1110 1000

Data Transfer Sequence:



SELF CAL Offset and Gain Self Calibration

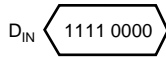
Description: Starts the process of self calibration. The Offset Control Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:



SELFOCAL Offset Self Calibration

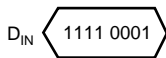
Description: Starts the process of self-calibration for offset. The Offset Control Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0001

Data Transfer Sequence:



SELFGCAL

Gain Self Calibration

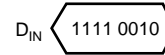
Description: Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0010

Data Transfer Sequence:



SYSOCAL System Offset Calibration

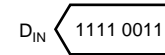
Description: Starts the system offset calibration process. For a system offset calibration the input should be set to 0V differential, and the ADS1217 computes the OCR register value that will compensate for offset errors. The Offset Control Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0011

Data Transfer Sequence:



SYSGCAL System Gain Calibration

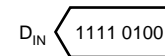
Description: Starts the system gain calibration process. For a system gain calibration, the differential input should be set to the reference voltage and the ADS1217 computes the FSR register value that will compensate for gain errors. The FSR is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0100

Data Transfer Sequence:



NOTE: (1) For wait time, refer to timing specification.

DSYNC

Sync DRDY

Description: Synchronizes the ADS1217 to the serial clock edge.

Operands: None

Bytes: 1

Encoding: 1111 1100

Data Transfer Sequence:



SLEEP

Sleep Mode

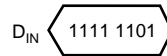
Description: Puts the ADS1217 into a low power sleep mode. SCLK must be inactive while in sleep mode. To exit this mode, issue the WAKEUP command.

Operands: None

Bytes: 1

Encoding: 1111 1101

Data Transfer Sequence:



WAKEUP Wakeup From Sleep Mode

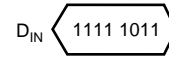
Description: Use this command to wake up from sleep mode.

Operands: None

Bytes: 1

Encoding: 1111 1011

Data Transfer Sequence:



RESET Reset to Power-Up Values

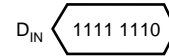
Description: Restore the registers to their power-up values. This command will also stop the Read Continuous mode. It does not affect the contents of RAM.

Operands: None

Bytes: 1

Encoding: 1111 1110

Data Transfer Sequence:



| MSB | LSB | | | | | | | | | | | | | | | |
|------|-------------|--------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
| 0000 | x | rdata | x | rdatac | x | x | x | x | x | x | x | x | x | x | x | stopc |
| 0001 | rreg 0 | rreg 1 | rreg 2 | rreg 3 | rreg 4 | rreg 5 | rreg 6 | rreg 7 | rreg 8 | rreg 9 | rreg A | rreg B | rreg C | rreg D | rreg E | rreg F |
| 0010 | rram 0 | rram 1 | rram 2 | rram 3 | rram 4 | rram 5 | rram 6 | rram 7 | x | x | x | x | x | x | x | x |
| 0011 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 0100 | creg 0 | creg 1 | creg 2 | creg 3 | creg 4 | creg 5 | creg 6 | creg 7 | crega | x | x | x | x | x | x | x |
| 0101 | wreg 0 | wreg 1 | wreg 2 | wreg 3 | wreg 4 | wreg 5 | wreg 6 | wreg 7 | wreg 8 | wreg 9 | wreg A | wreg B | wreg C | wreg D | wreg E | wreg F |
| 0110 | wram 0 | wram 1 | wram 2 | wram 3 | wram 4 | wram 5 | wram 6 | wram 7 | x | x | x | x | x | x | x | x |
| 0111 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1000 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1001 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1010 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1011 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1100 | cram 0 | cram 1 | cram 2 | cram 3 | cram 4 | cram 5 | cram 6 | cram 7 | x | x | x | x | x | x | x | x |
| 1101 | csramx 0 | csramx 1 | csramx 2 | csramx 3 | csramx 4 | csramx 5 | csramx 6 | csramx 7 | csa ramx | x | x | x | x | x | x | csreg |
| 1110 | cs ram 0 | cs ram 1 | cs ram2 | cs ram 3 | cs ram 4 | cs ram 5 | cs ram 6 | cs ram 7 | csa ram | x | x | x | x | x | x | x |
| 1111 | self cal | self ocal | self gcal | sys ocal | sys gcal | x | x | x | x | x | x | wakeup | dsync | sleep | reset | x |

x = Reserved

TABLE IV. Command Map.

DEFINITION OF TERMS

Analog Input Voltage—the voltage at any one analog input relative to AGND.

Analog Input Differential Voltage—given by the following equation: $(A_{IN+}) - (A_{IN-})$. Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is $2 \cdot 2.5V$. The negative full-scale output is produced when the differential is $2 \cdot (-2.5V)$. In each case, the actual input voltages must remain within the AGND to AV_{DD} range.

Conversion Cycle—the term *conversion cycle* usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period. However, each digital output is actually based on the modulator results from several t_{DATA} time periods.

| FILTER SETTING | MODULATOR RESULTS |
|-------------------|--------------------------|
| Fast Settling | 1 t_{DATA} Time Period |
| Sinc ² | 2 t_{DATA} Time Period |
| Sinc ³ | 3 t_{DATA} Time Period |

Data Rate—the rate at which conversions are completed. See definition for f_{DATA} .

Decimation Ratio—defines the ratio between the output of the modulator and the output Data Rate. Valid values for the Decimation Ratio are from 20 to 2047. Larger Decimation Ratios will have lower noise.

Effective Resolution—the effective resolution of the ADS1217 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and Vrms (referenced to input). Computed directly from the converter's output data, each is a statistical calculation. The conversion from one to the other is shown below.

Effective number of bits (ENOB) or effective resolution is commonly used to define the usable resolution of the A/D converter. It is calculated from empirical data taken directly from the device. It is typically determined by applying a fixed known signal source to the analog input and computing the standard deviation of the data sample set. The rms noise defines the $\pm\sigma$ interval about the sample mean.

The data from the A/D converter is output as codes, which then can be easily converted to other units, such as ppm or volts. The equations and table below show the relationship between bits or codes, ppm, and volts.

$$ENOB = \frac{-20 \log(\text{ppm})}{6.02}$$

| BITS rms | BIPOLAR Vrms | UNIPOLAR Vrms |
|----------|--|--|
| | $\frac{\left(\frac{4V_{REF}}{PGA}\right)}{10^{\left(\frac{6.02 \cdot ENOB}{20}\right)}}$ | $\frac{\left(\frac{2V_{REF}}{PGA}\right)}{10^{\left(\frac{6.02 \cdot ENOB}{20}\right)}}$ |
| 24 | 596nV | 298nV |
| 22 | 2.38 μ V | 1.19 μ V |
| 20 | 9.54 μ V | 4.77 μ V |
| 18 | 38.1 μ V | 19.1 μ V |
| 16 | 153 μ V | 76.4 μ V |
| 14 | 610 μ V | 305 μ V |
| 12 | 2.44mV | 1.22mV |

f_{DATA} —the frequency of the digital output data produced by the ADS1217, f_{DATA} is also referred to as the Data Rate.

$$f_{DATA} = \left(\frac{f_{MOD}}{\text{Decimation Ratio}} \right) = \left(\frac{f_{OSC}}{\text{mfactor} \cdot \text{Decimation Ratio}} \right)$$

f_{MOD} —the frequency or speed at which the modulator of the ADS1217 is running. This depends on the SPEED bit as shown below:

| SPEED BIT | f_{MOD} |
|-----------|---------------|
| 0 | $f_{OSC}/128$ |
| 1 | $f_{OSC}/256$ |

f_{OSC} —the frequency of the crystal input signal at the X_{IN} input of the ADS1217.

f_{SAMP} —the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

| PGA SETTING | SAMPLING FREQUENCY |
|-------------|---|
| 1, 2, 4, 8 | $f_{SAMP} = \frac{f_{OSC}}{\text{mfactor}}$ |
| 8 | $f_{SAMP} = \frac{2f_{OSC}}{\text{mfactor}}$ |
| 16 | $f_{SAMP} = \frac{8f_{OSC}}{\text{mfactor}}$ |
| 32 | $f_{SAMP} = \frac{16f_{OSC}}{\text{mfactor}}$ |
| 64, 128 | $f_{SAMP} = \frac{16f_{OSC}}{\text{mfactor}}$ |

Filter Selection—the ADS1217 uses a (sinc/x) filter or *sinc* filter. There are three different sinc filters that can be selected. A fast settling filter will settle in one t_{DATA} cycle. The sinc² filter will settle in two cycles and have lower noise. The sinc³ will achieve lowest noise and higher number of effective bits, but requires three cycles to settle. The ADS1217 will operate with any one of these filters, or it can operate in an auto mode, where it will first select the fast settling filter after a new channel is selected and will then switch to sinc² for one reading, followed by sinc³ from then on.

Full-Scale Range (FSR)—as with most A/D converters, the full-scale range of the ADS1217 is defined as the “input”, which produces the positive full-scale digital output minus the “input”, which produces the negative full-scale digital output. The full-scale range changes with gain setting, see Table V.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: $2 \cdot [1.25\text{V (positive full-scale) minus } -1.25\text{V (negative full-scale)}] = 5\text{V}$.

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full - Scale Range}}{2^N}$$

where N is the number of bits in the digital output.

t_{DATA} —the inverse of f_{DATA} , or the period between each data output.

| GAIN SETTING | 5V SUPPLY ANALOG INPUT ⁽¹⁾ | | | GENERAL EQUATIONS | | |
|--------------|---------------------------------------|--|------------------|--------------------------------------|--|---|
| | FULL-SCALE RANGE | DIFFERENTIAL INPUT VOLTAGES ⁽²⁾ | PGA OFFSET RANGE | FULL-SCALE RANGE | DIFFERENTIAL INPUT VOLTAGES ⁽²⁾ | PGA SHIFT RANGE |
| 1 | 10V | ±5V | ±2.5 | $\frac{4V_{\text{REF}}}{\text{PGA}}$ | $\frac{\pm 2V_{\text{REF}}}{\text{PGA}}$ | $\frac{\pm V_{\text{REF}}}{\text{PGA}}$ |
| 2 | 5V | ±2.5V | ±1.25V | | | |
| 4 | 2.5V | ±1.25V | ±0.625V | | | |
| 8 | 1.25V | ±0.625V | ±312.5mV | | | |
| 16 | 0.625V | ±312.5mV | ±156.25mV | | | |
| 32 | 312.5mV | ±156.25mV | ±78.125mV | | | |
| 64 | 156.25mV | ±78.125mV | ±39.0625mV | | | |
| 128 | 78.125mV | ±39.0625mV | ±19.531mV | | | |

NOTES: (1) With a 2.5V reference. (2) The ADS1217 allows common-mode voltage as long as the absolute input voltage on $A_{\text{IN}+}$ or $A_{\text{IN}-}$ does not go below AGND or above AV_{DD} .

TABLE V. Full-Scale Range versus PGA Setting.

Revision History

| DATE | REVISION | PAGE | SECTION | DESCRIPTION |
|------|----------|------|----------------------------|---|
| 2/07 | C | 2,4 | Electrical Characteristics | Changed Gain Error condition from "Before Calibration" to "After Calibration" |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| ADS1217IPFBR | ACTIVE | TQFP | PFB | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1217IPFBRG4 | ACTIVE | TQFP | PFB | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1217IPFBT | ACTIVE | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1217IPFBTG4 | ACTIVE | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

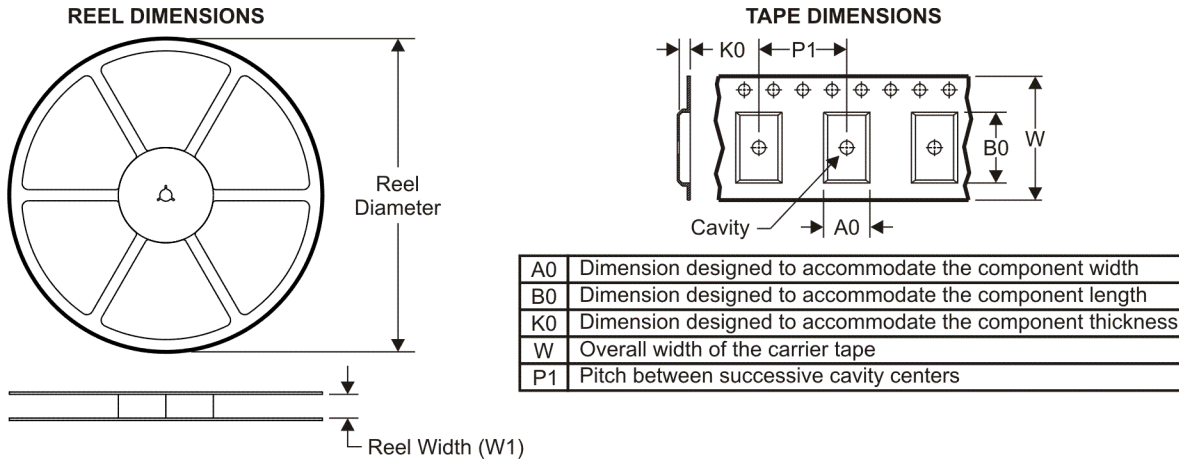
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

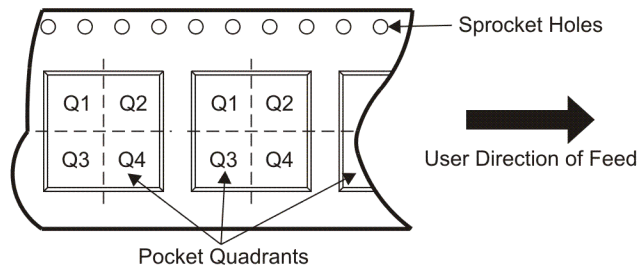
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TAPE AND REEL INFORMATION



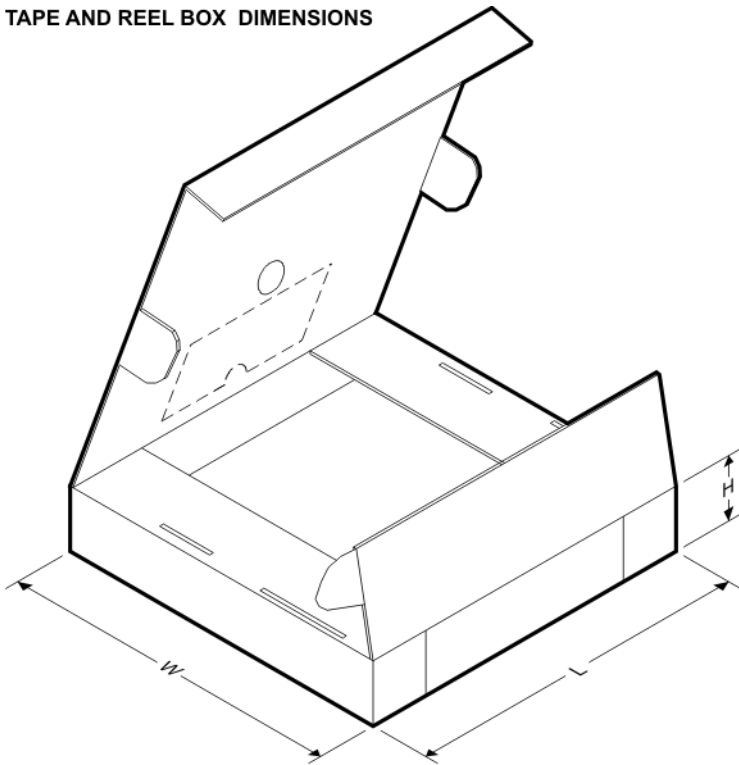
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS1217IPFBR | TQFP | PFB | 48 | 2000 | 330.0 | 16.8 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS1217IPFBT | TQFP | PFB | 48 | 250 | 177.8 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

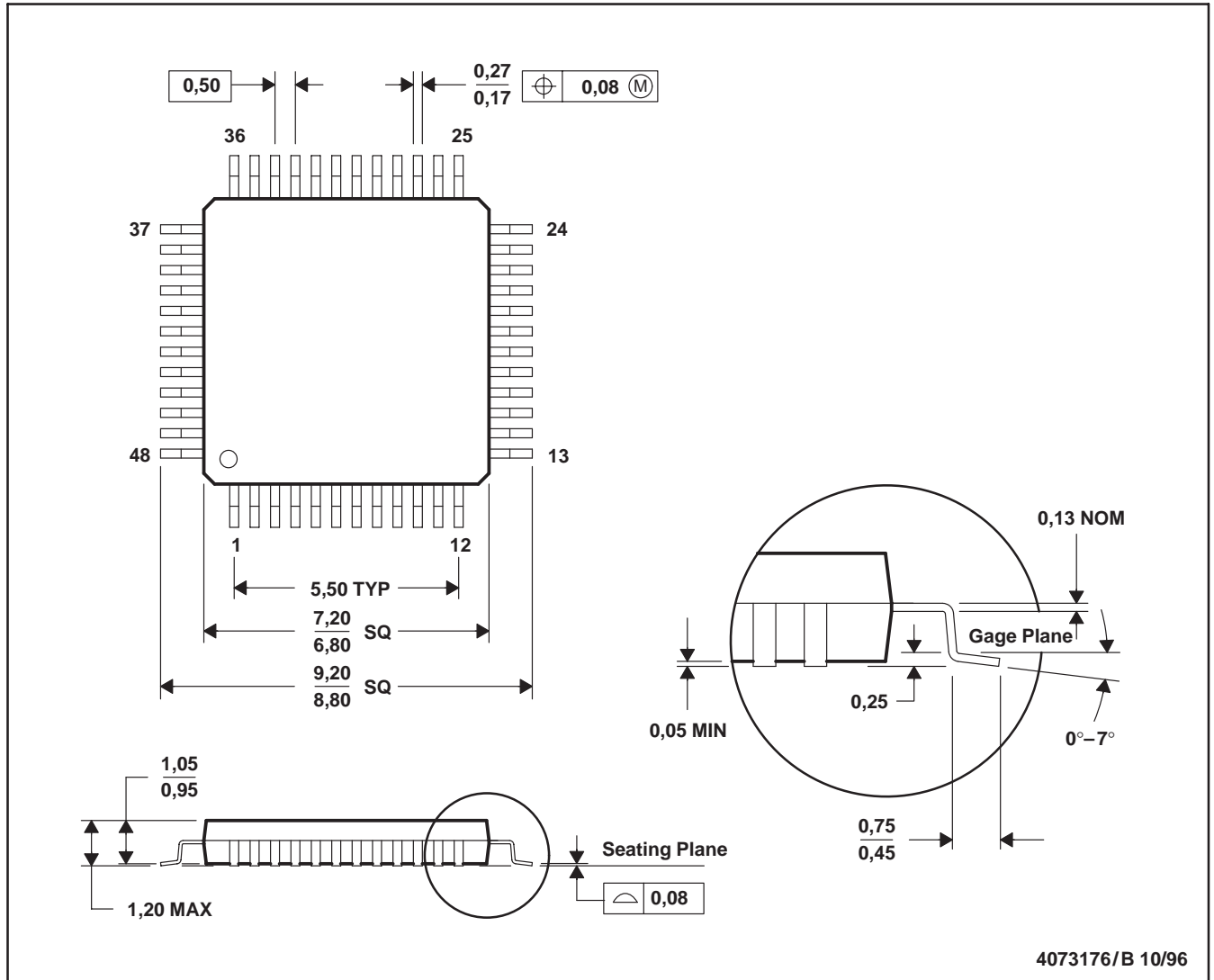


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS1217IPFBR | TQFP | PFB | 48 | 2000 | 346.0 | 346.0 | 33.0 |
| ADS1217IPFBT | TQFP | PFB | 48 | 250 | 184.0 | 184.0 | 50.0 |

PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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