



Two 1-Bit, 10MHz, 2nd-Order Delta-Sigma Modulators

Check for Samples: [ADS1209](#)

FEATURES

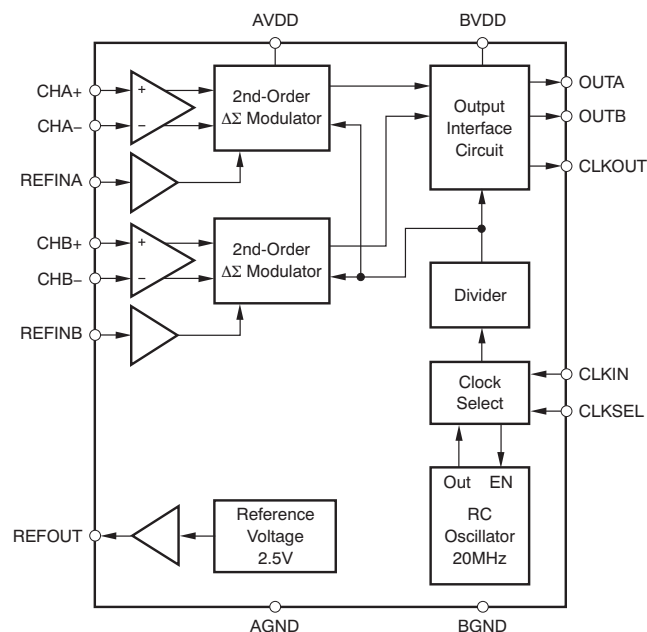
- **16-Bit Resolution**
- **13-Bit Linearity**
- **±2.3V Specified Input Voltage Range**
- **Internal Reference Voltage: 2%**
- **Gain Error: 0.5%**
- **Two Independent Delta-Sigma Modulators**
- **Two Input Reference Buffers**
- **On-Chip Oscillator**
- **Selectable Internal or External Clock**
- **Specified Temperature Range:
–40°C to +105°C**
- **TSSOP-24 Package**

APPLICATIONS

- **Motor Control**
- **Current Measurement**
- **Resolver**
- **Industrial Process Control**
- **Instrumentation**

DESCRIPTION

The ADS1209 is a two-channel, high-performance, delta-sigma ($\Delta\Sigma$) modulator with an 86dB dynamic range, operating from a single +5V supply. The differential inputs are ideal for direct connection to signal sources in an industrial environment. With the appropriate digital filter and modulator rate, the device can be used to achieve 16-bit analog-to-digital (A/D) conversion with no missing codes. Effective accuracy of 14 bits can be obtained with a digital filter bandwidth of 20kHz at a modulator rate of 10MHz. The ADS1209 is designed for use in high-resolution measurement applications including current measurements, industrial process control, and resolvers. It is available in a TSSOP-24 package and is specified for operation over the ambient temperature range of –40°C to +105°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---------|--------------|--------------------|-----------------------------|-----------------|---------------------------|
| ADS1209 | TSSOP-24 | PW | -40°C to +105°C | ADS1209SPW | Tube, 60 |
| | | | | ADS1209SPWR | Tape and Reel, 2000 |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating ambient temperature range, unless otherwise noted.

| | ADS1209 | UNIT |
|--|---|-------|
| Supply voltage, AVDD to AGND | -0.3 to 6 | V |
| Supply voltage, BVDD to BGND | -0.3 to 6 | V |
| Analog input voltage | AGND - 0.3 to AVDD + 0.3 | V |
| Reference input voltage | AGND - 0.3 to AVDD + 0.3 | V |
| Digital input voltage | BGND - 0.3 to BVDD + 0.3 | V |
| Ground voltage difference, AGND to BGND | ±0.3 | V |
| Input current to any pin except supply | ±10 | mA |
| Operating virtual junction temperature range, T _J | -40 to +150 | °C |
| Operating ambient temperature range, T _{OA} | -40 to +125 | °C |
| ESD ratings, all pins | Human body model (HBM) JEDEC standard 22, test method A114-C.01 | +2000 |
| | Charged device model (CDM) JEDEC standard 22, test method C101 | +500 |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

| PACKAGE | T _A ≤ +25°C POWER RATING | DERATING FACTOR ABOVE T _A = +25°C ⁽¹⁾ | T _A = +70°C POWER RATING | T _A = +85°C POWER RATING | T _A = +105°C POWER RATING |
|----------|-------------------------------------|---|-------------------------------------|-------------------------------------|--------------------------------------|
| TSSOP-24 | 1420mW | 11.3mW/°C | 909mW | 738mW | 511mW |

(1) This is the inverse of the traditional junction-to-ambient thermal resistance (R_{θJA}). Thermal resistances are not production tested and are for informational purposes only.

THERMAL CHARACTERISTICS: TSSOP-24

Over the operating ambient temperature range of -40°C to +105°C, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| R _{θJA} | Junction-to-air thermal resistance High-K thermal resistance ⁽¹⁾ | | 88 | | °C/W |
| R _{θJC} | Junction-to-case thermal resistance | | 26 | | °C/W |
| P _D | Device power dissipation CLKSEL = 0, 5V supply | | | 100 | mW |

(1) Modeled in accordance with the High-K thermal definitions of EIA/JESD51-3.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|--------------------|--------------------------|-----|--------------------------|------|
| Supply voltage, AVDD to AGND | | 4.5 | 5 | 5.5 | V |
| Supply voltage, BVDD to BGND | Low-voltage levels | 2.7 | 3.0 | 3.6 | V |
| | 5V logic levels | 4.5 | 5 | 5.5 | V |
| Reference input voltage, V _{REF} | | 0.5 | 2.5 | 2.6 | V |
| Operating common-mode signal | | 0 | | AVDD | V |
| Analog inputs | +IN – (–IN) | –0.92 × V _{REF} | | +0.92 × V _{REF} | V |
| External clock ⁽¹⁾ | | 16 | 20 | 24 | MHz |
| Operating ambient temperature range, T _{OA} | | –40 | | +125 | °C |
| Specified ambient temperature range, T _A | | –40 | | +105 | °C |

(1) With reduced accuracy, clock can go from 1MHz up to 33MHz; see [Typical Characteristic](#) curves.

ELECTRICAL CHARACTERISTICS

Over operating ambient temperature range of –40°C to +105°C, AVDD = 5V, BVDD = 3V, CHx+ = 0.2V to 4.8V, CHx– = 2.5V, V_{REFIN} = V_{REFOUT} = 2.5V (internal), CLKIN = 20MHz, and 16-bit Sinc³ filter with OSR = 256, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | ADS1209 | | | UNIT |
|----------------------|---|---|--------------------------|--------------------|--------------------------|--------|
| | | | MIN | TYP ⁽¹⁾ | MAX | |
| RESOLUTION | | | 16 | | | Bits |
| DC ACCURACY | | | | | | |
| INL | Integral linearity error ⁽²⁾ | V _{IN} = ±2.3V _{PP} | –8 | ±3.8 | +8 | LSB |
| | | V _{IN} = ±2.0V _{PP} | –4 | ±1.8 | +4 | LSB |
| | Integral linearity match | | 1 | | 4 | LSB |
| DNL | Differential nonlinearity | | –1 | | +1 | LSB |
| V _{OS} | Input offset error | | –3 | ±1.5 | +3 | mV |
| | Input offset error match | | 0.2 | | 2 | mV |
| TCV _{OS} | Input offset error thermal drift | | –8 | 1 | +8 | µV/°C |
| G _{ERR} | Gain error | Referenced to V _{REFIN} | –0.5 | ±0.02 | +0.5 | % FSR |
| | Gain error match | | 0.1 | | 0.5 | % FSR |
| TCG _{ERR} | Gain error thermal drift | | ±1.3 | | | ppm/°C |
| PSRR | Power-supply rejection ratio | 4.5V < AVDD < 5.5V | 82 | | | dB |
| ANALOG INPUTS | | | | | | |
| FSR | Full-scale differential input voltage range | (CHx+) – (CHx–); CHx– = 2.5V | –V _{REFIN} | | +V _{REFIN} | V |
| | Specified differential input voltage range | (CHx+) – (CHx–); CHx– = 2.5V | –0.92 × V _{REF} | | +0.92 × V _{REF} | V |
| | Absolute operating input voltage range | | 0 | | AV _{DD} | V |
| C _I | Input capacitance | CHx to AGND | 3 | | | pF |
| I _{IL} | Input leakage current | Clock turned off | –1 | | 1 | µA |
| R _{ID} | Differential input resistance | | 100 | | | kΩ |
| C _{ID} | Differential input capacitance | | 2.5 | | | pF |
| CMRR | Common-mode rejection ratio | At dc | 108 | | | dB |
| | | V _{IN} = ±1.25V _{PP} at 40kHz | 117 | | | dB |
| BW | Bandwidth | Full-scale sine wave, –3dB | 50 | | | MHz |

(1) All typical values are at T_A = +25°C.

(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range, expressed either as the number of LSBs or as a percent of specified input range (4.6V).

ELECTRICAL CHARACTERISTICS (continued)

Over operating ambient temperature range of -40°C to $+105^{\circ}\text{C}$, $\text{AVDD} = 5\text{V}$, $\text{BVDD} = 3\text{V}$, $\text{CHx+} = 0.2\text{V}$ to 4.8V , $\text{CHx-} = 2.5\text{V}$, $\text{V}_{\text{REFIN}} = \text{V}_{\text{REFOUT}} = 2.5\text{V}$ (internal), $\text{CLKIN} = 20\text{MHz}$, and 16-bit Sinc³ filter with $\text{OSR} = 256$, unless otherwise noted.

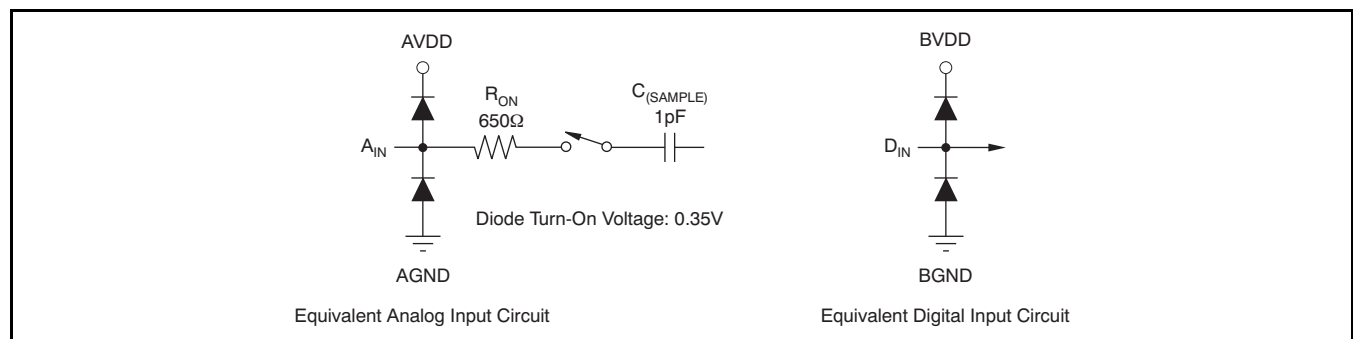
| PARAMETER | TEST CONDITIONS | ADS1209 | | | UNIT | |
|---------------------------------|--------------------------------|---|---------------------------|--------------------------|-------|----------------------------|
| | | MIN | TYP ⁽¹⁾ | MAX | | |
| SAMPLING DYNAMICS | | | | | | |
| f_{CLK} | Internal clock frequency | $\text{CLKSEL} = 1, -40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ | 8 | 10 | 12 | MHz |
| | | $\text{CLKSEL} = 1, -40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ | 7.8 | 10 | 12 | MHz |
| f_{CLKIN} | External clock frequency | $\text{CLKSEL} = 0$ | 1 | 20 | 24 | MHz |
| AC ACCURACY | | | | | | |
| THD | Total harmonic distortion | $V_{\text{IN}} = \pm 2.3V_{\text{PP}}$ at 5kHz | | -85 | -80 | dB |
| SFDR | Spurious-free dynamic range | $V_{\text{IN}} = \pm 2.3V_{\text{PP}}$ at 5kHz | 82 | 86 | | dB |
| SNR | Signal-to-noise ratio | $V_{\text{IN}} = \pm 2.3V_{\text{PP}}$ at 5kHz | 86 | 90 | | dB |
| | | $V_{\text{IN}} = \pm 2.0V_{\text{PP}}$ at 5kHz | 85 | 89 | | dB |
| SINAD | Signal-to-noise + distortion | $V_{\text{IN}} = \pm 2.3V_{\text{PP}}$ at 5kHz | 80 | 84 | | dB |
| | Channel-to-channel isolation | $V_{\text{IN}} = \pm 2.3V_{\text{PP}}$ at 5kHz | | 100 | | dB |
| REFERENCE VOLTAGE OUTPUT | | | | | | |
| V_{REFOUT} | Reference output voltage | | 2.450 | 2.5 | 2.550 | V |
| $\text{TCV}_{\text{REFOUT}}$ | Reference output voltage drift | | | ± 20 | | ppm/ $^{\circ}\text{C}$ |
| | Output voltage noise | $f = 0.1\text{Hz}$ to 10Hz , $C_L = 10\mu\text{F}$ | | 10 | | μV_{RMS} |
| | | $f = 10\text{Hz}$ to 10kHz , $C_L = 10\mu\text{F}$ | | 12 | | μV_{RMS} |
| I_{REFOUT} | Output current | | | 10 | | μA |
| I_{REFSC} | Short-circuit current | | | 0.5 | | mA |
| | Turn-on settling time | To accuracy level of 0.1%, no load | | 100 | | μs |
| REFERENCE VOLTAGE INPUT | | | | | | |
| V_{REFIN} | Input voltage | | 0.5 | 2.5 | 2.6 | V |
| R_{REFIN} | Input resistance | | | 100 | | M Ω |
| C_{REFIN} | Input capacitance | | | 5 | | pF |
| I_{REFIN} | Input current | | | | 1 | μA |
| DIGITAL INPUTS | | | | | | |
| | Logic family | | CMOS with Schmitt Trigger | | | |
| V_{IH} | High-level input voltage | | $0.7 \times \text{BVDD}$ | $\text{BVDD} + 0.3$ | | V |
| V_{IL} | Low-level input voltage | | -0.3 | $0.3 \times \text{BVDD}$ | | V |
| I_{IN} | Input current | $\text{V}_{\text{IN}} = \text{BVDD}$ or BGND | | ± 50 | | nA |
| C_I | Input capacitance | | | 5 | | pF |
| DIGITAL OUTPUTS | | | | | | |
| | Logic family | | CMOS | | | |
| V_{OH} | High-level output voltage | $\text{BVDD} = 4.5\text{V}$, $\text{I}_{\text{OH}} = -100\mu\text{A}$ | 4.44 | | | V |
| V_{OL} | Low-level output voltage | $\text{BVDD} = 4.5\text{V}$, $\text{I}_{\text{OL}} = +100\mu\text{A}$ | | | 0.5 | V |
| C_O | Output capacitance | | | 5 | | pF |
| C_L | Load capacitance | | | | 30 | pF |
| | Data format | | Bit stream | | | |

ELECTRICAL CHARACTERISTICS (continued)

Over operating ambient temperature range of -40°C to $+105^{\circ}\text{C}$, $\text{AVDD} = 5\text{V}$, $\text{BVDD} = 3\text{V}$, $\text{CHx+} = 0.2\text{V}$ to 4.8V , $\text{CHx-} = 2.5\text{V}$, $\text{V}_{\text{REFIN}} = \text{V}_{\text{REFOUT}} = 2.5\text{V}$ (internal), $\text{CLKIN} = 20\text{MHz}$, and 16-bit Sinc³ filter with $\text{OSR} = 256$, unless otherwise noted.

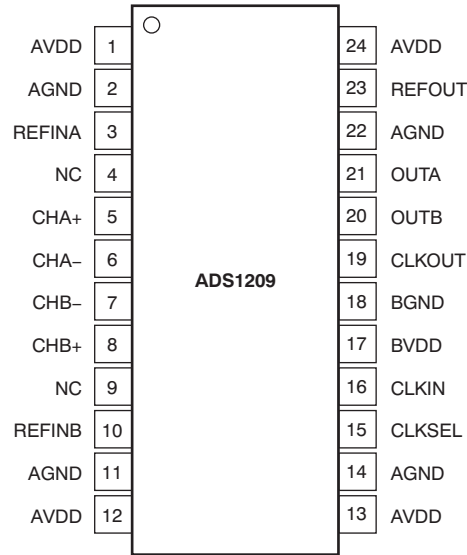
| PARAMETER | TEST CONDITIONS | ADS1209 | | | UNIT | |
|------------------------|-------------------------------------|--|---------------------|---------------------|-------|----|
| | | MIN | TYP ⁽¹⁾ | MAX | | |
| DIGITAL INPUTS | | | | | | |
| | Logic family | LVCMOS | | | | |
| V_{IH} | High-level input voltage | $\text{BVDD} = 3.6\text{V}$ | 2 | $\text{BVDD} + 0.3$ | V | |
| V_{IL} | Low-level input voltage | $\text{BVDD} = 2.7\text{V}$ | -0.3 | 0.8 | V | |
| I_{IN} | Input current | $\text{V}_{\text{IN}} = \text{BVDD}$ or BGND | | ± 50 | nA | |
| C_1 | Input capacitance | | 5 | | pF | |
| DIGITAL OUTPUTS | | | | | | |
| | Logic family | LVCMOS | | | | |
| V_{OH} | High-level output voltage | $\text{BVDD} = 2.7\text{V}$, $\text{I}_{\text{OH}} = -100\mu\text{A}$ | $\text{BVDD} - 0.2$ | | V | |
| V_{OL} | Low-level output voltage | $\text{BVDD} = 2.7\text{V}$, $\text{I}_{\text{OL}} = +100\mu\text{A}$ | | 0.2 | V | |
| C_0 | Output capacitance | | 5 | | pF | |
| C_L | Load capacitance | | | 30 | pF | |
| | Data format | Bit stream | | | | |
| POWER SUPPLY | | | | | | |
| AVDD | Analog supply voltage | | 4.5 | 5.0 | 5.5 | V |
| BVDD | Buffer I/O supply voltage | Low-voltage levels | 2.7 | 3.0 | 3.6 | V |
| | | 5V logic levels | 4.5 | 5.0 | 5.5 | V |
| AIDD | Analog operating supply current | $\text{CLKSEL} = 1$ | | 12.2 | 17 | mA |
| | | $\text{CLKSEL} = 0$ | | 11.8 | 16 | mA |
| BIDD | Buffer I/O operating supply current | $\text{BVDD} = 3\text{V}$, $\text{CLKOUT} = 10\text{MHz}$ | | 0.9 | 2 | mA |
| | | $\text{BVDD} = 5\text{V}$, $\text{CLKOUT} = 10\text{MHz}$ | | 1.3 | 3 | mA |
| P_D | Power dissipation | $\text{CLKSEL} = 1$, 5V supply | | 67.5 | 100.0 | mW |
| | | $\text{CLKSEL} = 0$, 5V supply | | 65.5 | 95 | mW |

EQUIVALENT INPUT CIRCUITS



PIN CONFIGURATION

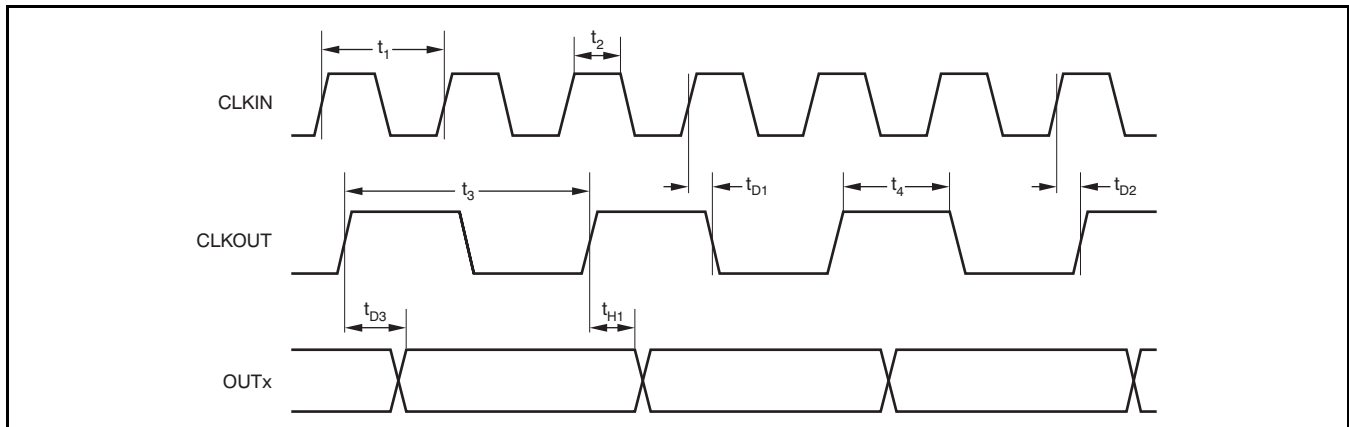
**PW PACKAGE
TSSOP-24
(TOP VIEW)**



PIN DESCRIPTIONS

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|--------|-----|--------------------|---|
| NAME | NO. | | |
| AVDD | 1 | P | Analog power supply; nominal 5V. Decouple to AGND with a 0.1µF ceramic capacitor. |
| AGND | 2 | P | Analog ground. Connect to analog ground plane. |
| REFINA | 3 | AI | Reference voltage input for channel A |
| NC | 4 | NC | This pin is not internally connected |
| CHA+ | 5 | AI | Fully differential noninverting analog input channel A |
| CHA- | 6 | AI | Fully differential inverting analog input channel A |
| CHB- | 7 | AI | Fully differential inverting analog input channel B |
| CHB+ | 8 | AI | Fully differential noninverting analog input channel B |
| NC | 9 | NC | This pin is not internally connected |
| REFINB | 10 | AI | Reference voltage input for channel B |
| AGND | 11 | P | Analog ground. Connect to analog ground plane. |
| AVDD | 12 | P | Analog power supply; nominal 5V. Decouple to AGND with a 0.1µF ceramic capacitor. |
| AVDD | 13 | P | Analog power supply; nominal 5V. Decouple to AGND with a 0.1µF ceramic capacitor. |
| AGND | 14 | P | Analog ground. Connect to analog ground plane. |
| CLKSEL | 15 | DI | Clock select input. When this pin is low, an external clock source at CLKIN is used. When high, the internal RC oscillator is used as clock source. |
| CLKIN | 16 | DI | External clock input. Must be tied to BVDD or BGND, if not used. |
| BVDD | 17 | P | I/O buffer power supply, nominal: 3V. Decouple to BGND with a 0.1µF ceramic capacitor |
| BGND | 18 | P | I/O buffer ground. Connect to digital ground plane |
| CLKOUT | 19 | DO | Bit stream clock output |
| OUTB | 20 | DO | Bit stream data output of channel B modulator |
| OUTA | 21 | DO | Bit stream data output of channel A modulator |
| AGND | 22 | P | Analog ground. Connect to analog ground plane. |
| REFOUT | 23 | AO | Internal reference voltage output, nominal: 2.5V. Decouple to AGND with a 0.1µF ceramic capacitor. |
| AVDD | 24 | P | Analog power supply, nominal: 5V. Decouple to AGND with a 0.1µF ceramic capacitor. |

(1) AI = analog input; AO = analog output; DI = digital input; DO = digital output; P = power supply; NC = not connected.

PARAMETER MEASUREMENT INFORMATION

Figure 1. ADS1209 Timing Diagram
TIMING CHARACTERISTICS⁽¹⁾

Over the recommended operating ambient temperature range of -40°C to $+105^{\circ}\text{C}$, $V_{\text{DD}} = 5\text{V}$, and $BV_{\text{DD}} = 2.7\text{V}$ to 5V , unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------|---|-----------------|----------------|---------------|------|
| t_1 | CLKIN period | CLKSEL = 0 | 41.6 | 1000 | ns |
| t_2 | CLKIN high time | CLKSEL = 0 | 10 | $t_1 - 10$ | ns |
| t_3 | CLKOUT period | CLKSEL = 0 | $2 \times t_1$ | | ns |
| | | CLKSEL = 1 | 83 | 125 | ns |
| t_4 | CLKOUT high time | | $(t_3/2) - 5$ | $(t_3/2) + 5$ | ns |
| t_{D1} | CLKIN rising edge to CLKOUT falling edge delay | CLKSEL = 0 | | 10 | ns |
| t_{D2} | CLKIN rising edge to CLKOUT rising edge delay | CLKSEL = 0 | | 10 | ns |
| t_{D3} | CLKOUT rising edge to new data valid delay | CLKSEL = 0 | $t_2 + 7$ | | ns |
| | | CLKSEL = 1 | $(t_3/4) + 8$ | | ns |
| t_{H1} | Data valid hold time referred to rising CLKOUT edge | CLKSEL = 0 | $t_2 - 3$ | | ns |
| | | CLKSEL = 1 | $(t_3/4) - 8$ | | ns |

(1) All input signals are specified with $t_R = t_F = 1.5\text{ns}$ (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{\text{IL}} + V_{\text{IH}})/2$.

TYPICAL CHARACTERISTICS

At AVDD = 5V, BVDD = 3V, CHx+ = +0.2V to +4.8V, CHx- = +2.5V, V_{REFIN} = V_{REFOUT} = 2.5V (internal), CLKSEL = 1, and 16-bit Sinc³ filter, with OSR = 256, unless otherwise noted.

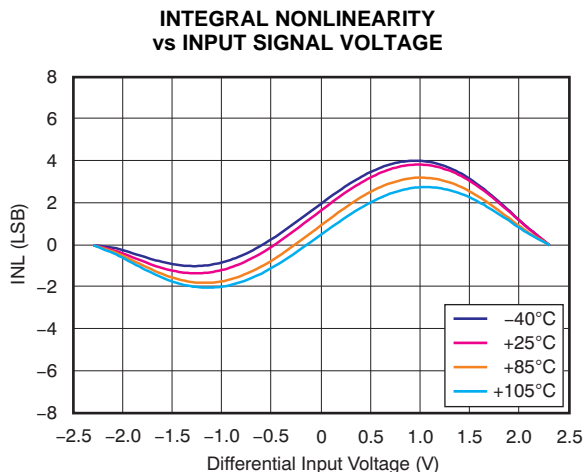


Figure 2.

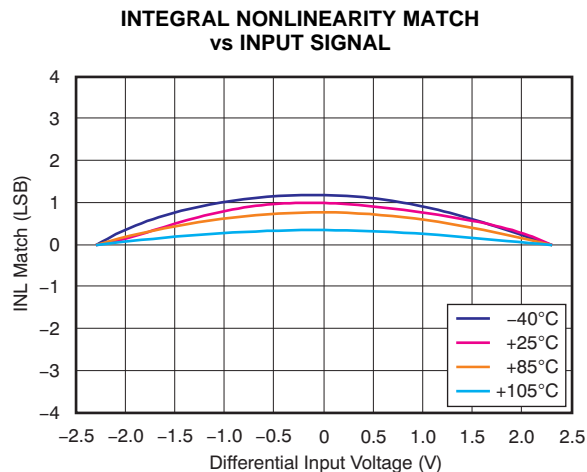


Figure 3.

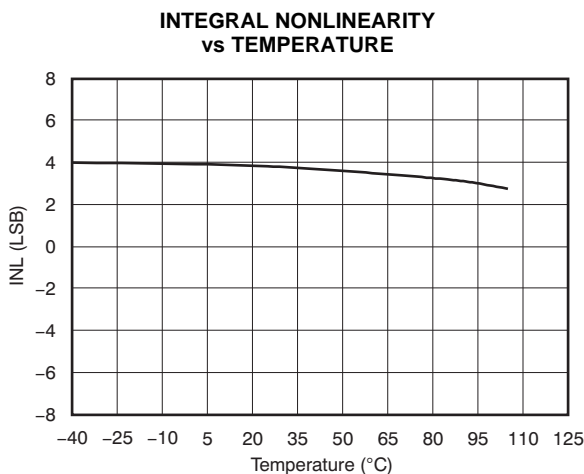


Figure 4.

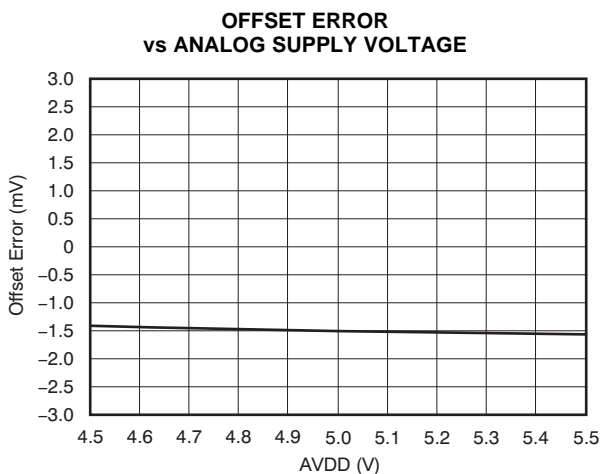


Figure 5.

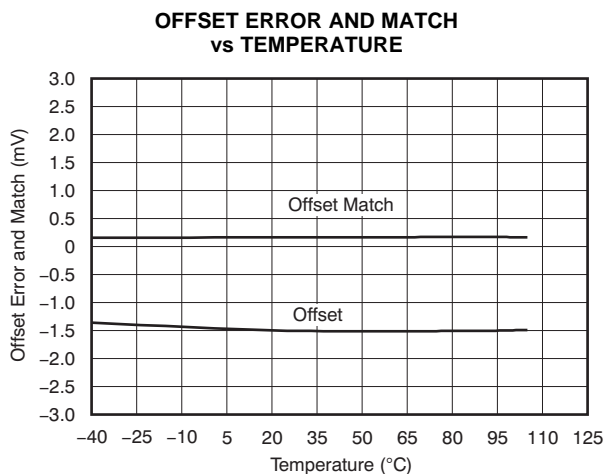


Figure 6.

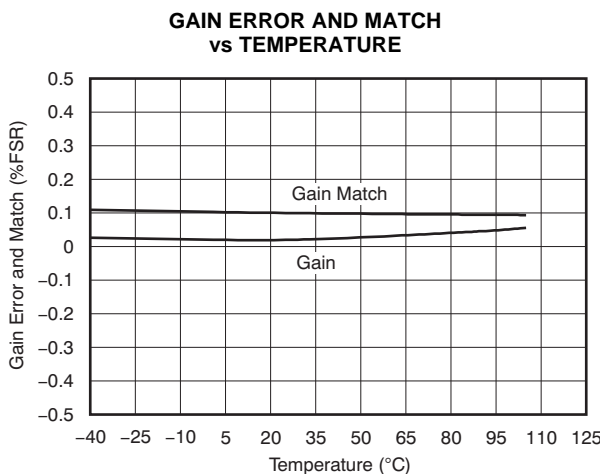


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5V, BVDD = 3V, CHx+ = +0.2V to +4.8V, CHx- = +2.5V, VREFIN = VREFOUT = 2.5V (internal), CLKSEL = 1, and 16-bit Sinc³ filter, with OSR = 256, unless otherwise noted.

POWER-SUPPLY REJECTION RATIO vs RIPPLE FREQUENCY

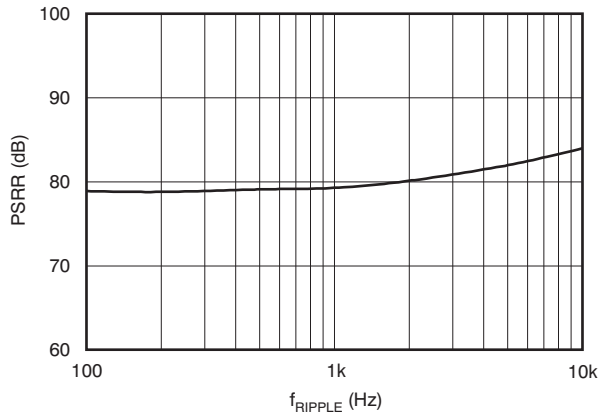


Figure 8.

COMMON-MODE REJECTION RATIO vs INPUT SIGNAL FREQUENCY

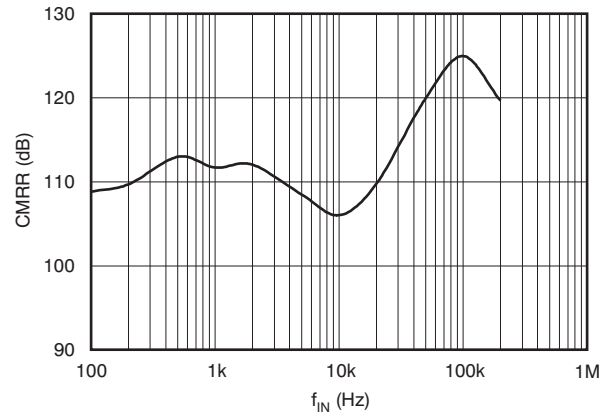


Figure 9.

INTERNAL CLOCK FREQUENCY ANALOG SUPPLY VOLTAGE

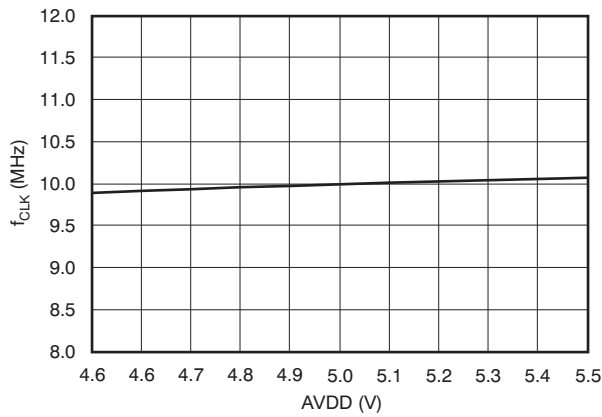


Figure 10.

INTERNAL CLOCK FREQUENCY vs TEMPERATURE

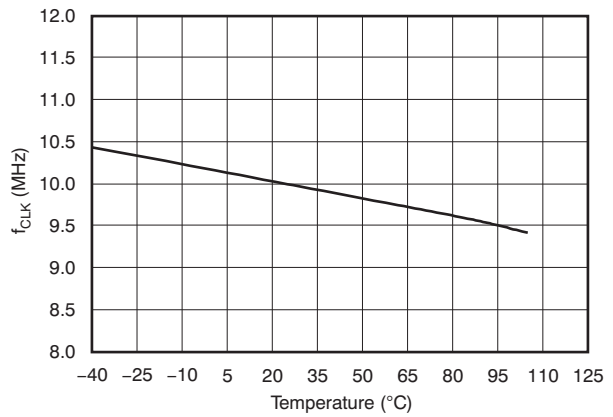


Figure 11.

TOTAL HARMONIC DISTORTION AND SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

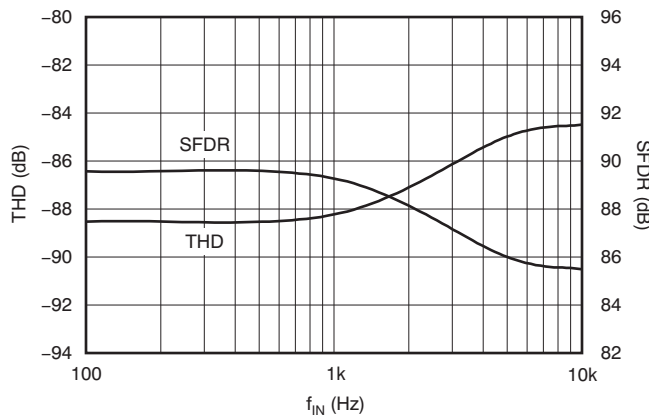


Figure 12.

TOTAL HARMONIC DISTORTION AND SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE

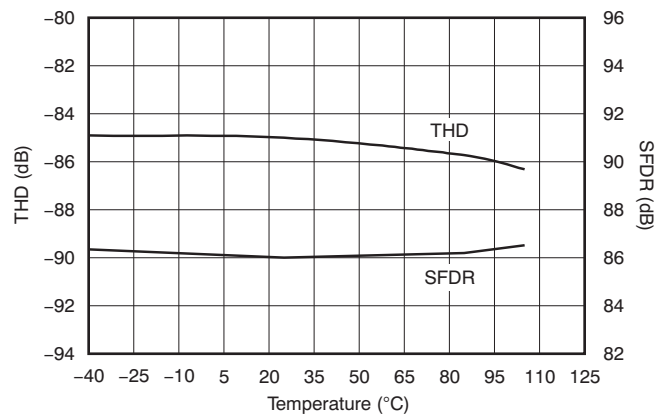


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5V, BVDD = 3V, CHx+ = +0.2V to +4.8V, CHx- = +2.5V, VREFIN = VREFOUT = 2.5V (internal), CLKSEL = 1, and 16-bit Sinc³ filter, with OSR = 256, unless otherwise noted.

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

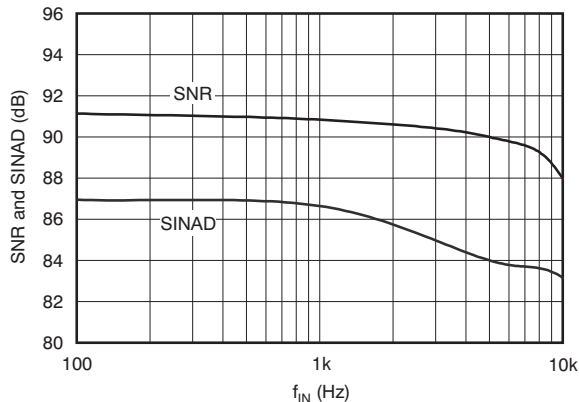


Figure 14.

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-NOISE + DISTORTION vs TEMPERATURE

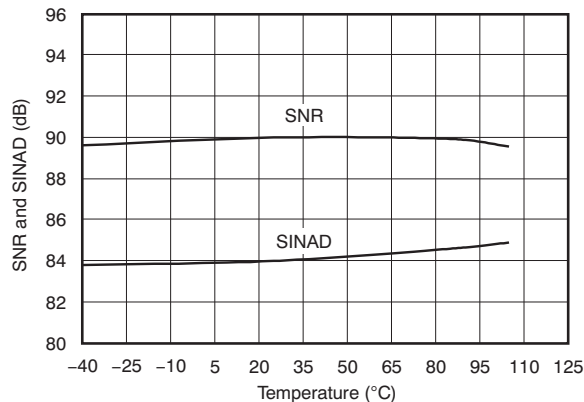


Figure 15.

FREQUENCY SPECTRUM (4096 Point FFT, f_{IN} = 1kHz, 4.6V_{PP})

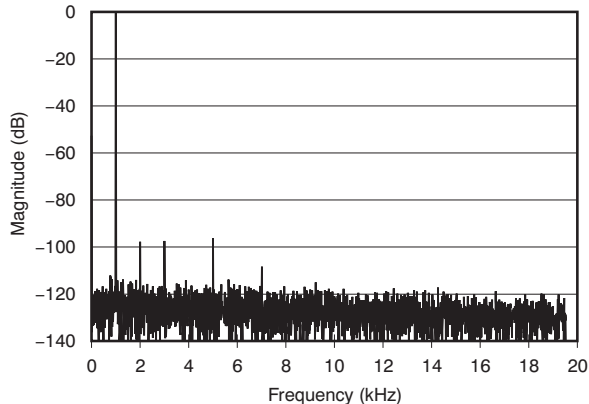


Figure 16.

FREQUENCY SPECTRUM (4096 Point FFT, f_{IN} = 5kHz, 4.6V_{PP})

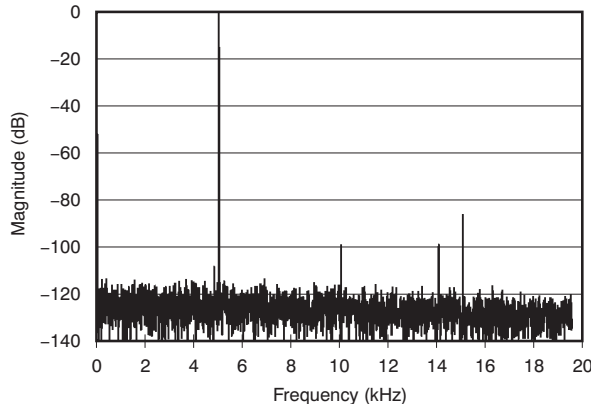


Figure 17.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE

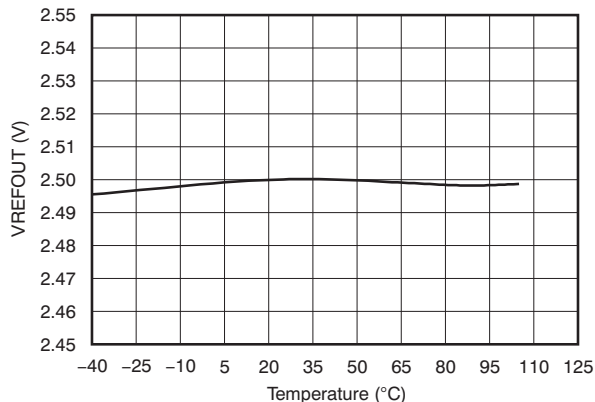


Figure 18.

SUPPLY CURRENT vs TEMPERATURE

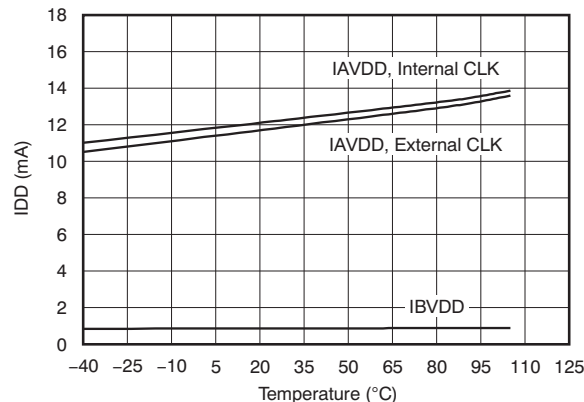


Figure 19.

GENERAL DESCRIPTION

The ADS1209 is a two-channel, second-order, CMOS device with two delta-sigma ($\Delta\Sigma$) modulators, designed for medium- to high-resolution A/D signal conversions from dc to 40kHz (filter response -3dB) if an oversampling ratio (OSR) of 64 is chosen. The output of the converter (OUTx) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies. A low-pass digital filter should be used at the output of the $\Delta\Sigma$ modulator. The filter serves two functions. First, it filters out high-frequency noise. Second, the filter converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation).

An application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) can be used to implement the digital filter. Alternatively, TI's [AMC1210](#) offers four programmable digital filters that can be used. [Figure 20](#) and [Figure 21](#) show typical application circuits with the ADS1209 connected to an FPGA or ASIC.

The overall performance (that is, speed and accuracy) depends on the selection of an appropriate OSR and filter type. A higher OSR produces greater output accuracy while operating at a lower data rate. Alternatively, a lower OSR produces lower output accuracy, but operates at a higher data rate. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 86dB with an OSR = 256.

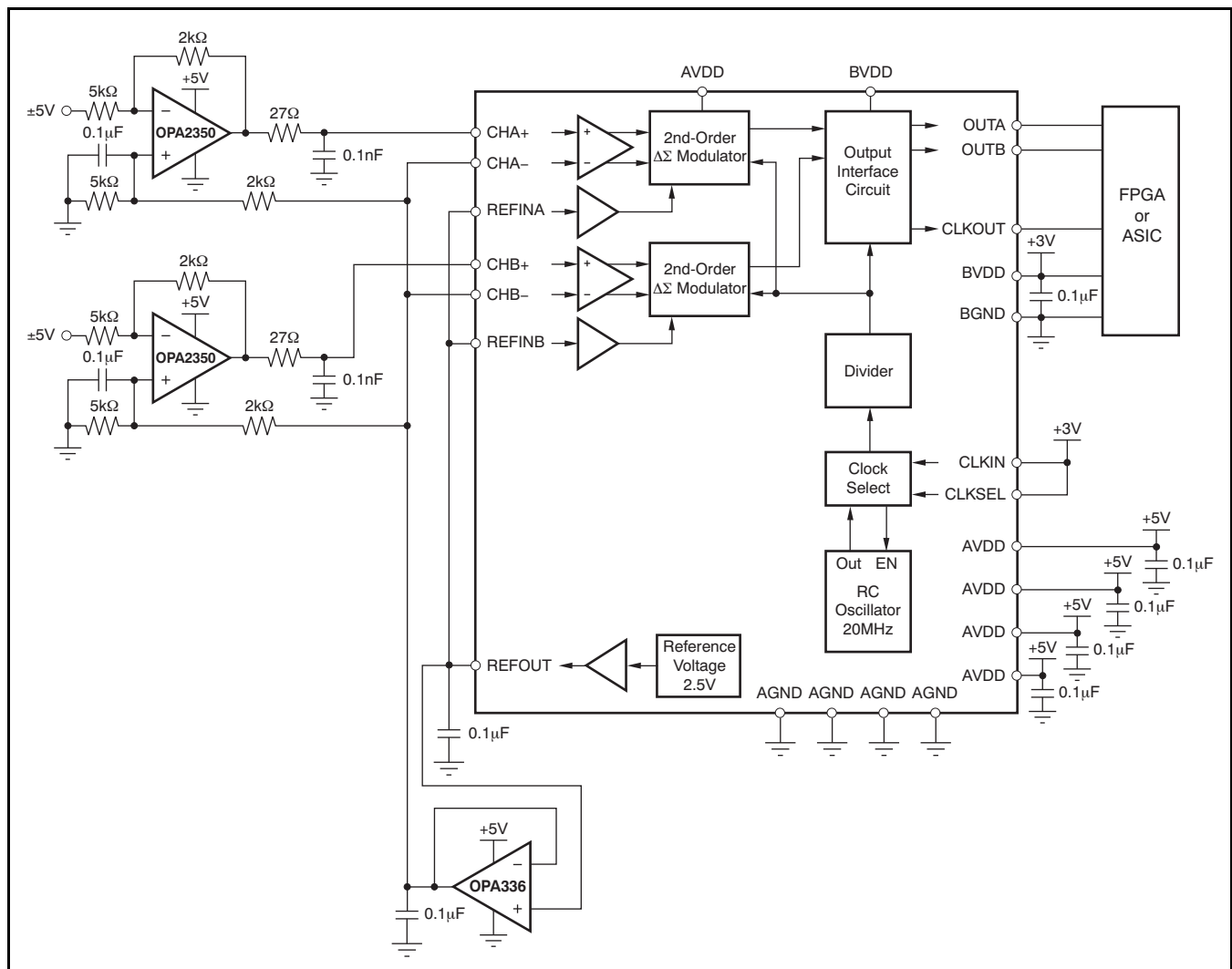


Figure 20. Single-Ended Connection Diagram for the ADS1209 $\Delta\Sigma$ Modulator

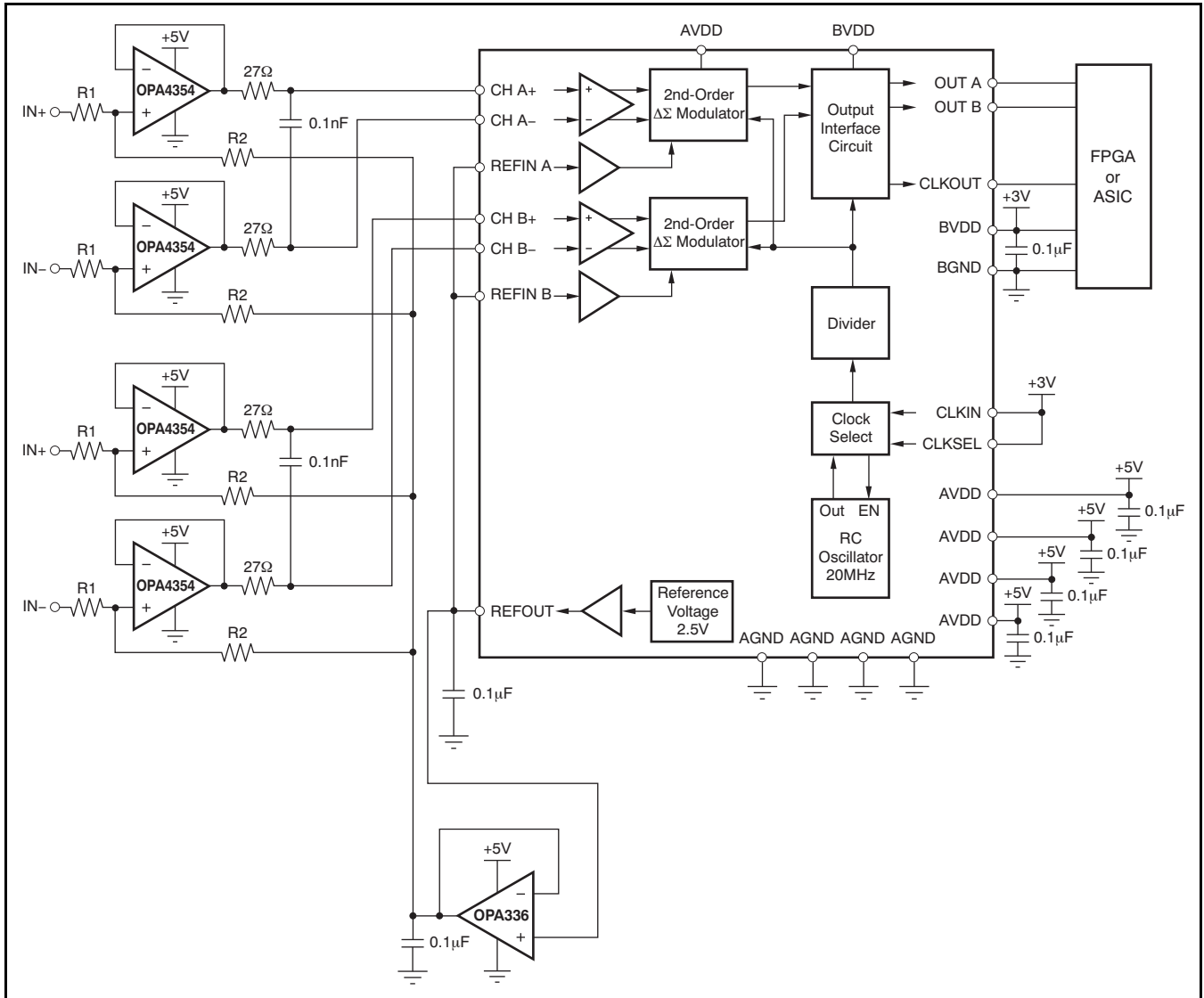


Figure 21. Differential Connection Diagram for the ADS1209 $\Delta\Sigma$ Modulator

THEORY OF OPERATION

The differential analog input of the ADS1209 is implemented with a switched-capacitor circuit. This circuit implements a second-order modulator stage, which digitizes the analog input signal into a 1-bit output stream. The clock source can be internal as well as external. Every analog input signal is continuously sampled by the modulator and compared to a reference voltage that is applied to the REFINx pin. A digital stream that represents the analog input voltage over time appears at the output of the corresponding converter.

ANALOG INPUT STAGE

Analog Input

The topology of the analog inputs of ADS1209 is based on fully differential switched-capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection, and excellent power-supply rejection.

The input impedance of the analog input depends on the modulator clock frequency (f_{MOD}). Figure 22 shows the basic input structure of one channel of the ADS1209. The relationship between the input impedance of the ADS1209 and the modulator clock frequency is:

$$Z_{IN} = \frac{100k\Omega}{f_{MOD}/10MHz} \quad (1)$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is high. This high impedance may cause degradation in gain, linearity, and THD. The importance of this effect depends on the desired system performance. There are two restrictions on the analog input signals, CHx+ and CHx-. If the input voltage exceeds the range (AGND – 0.3V) to (AVDD + 0.3V), the input current must be limited to 10mA because the input protection diodes on the front end of the converter begin to turn on. In addition, the linearity and noise performance of the device meet the stored specifications only when the differential analog voltage resides within $\pm 2.3V$ (with V_{REFIN} as a midpoint); however, the FSR input voltage is $\pm 2.5V$.

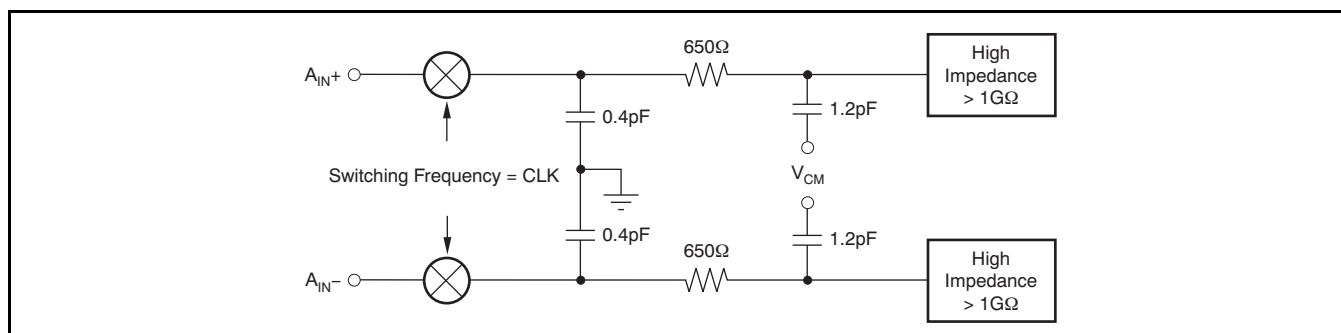


Figure 22. Input Impedance of the ADS1209

Modulator

The ADS1209 can be operated in two modes. When CKLSEL = 1, the two modulators operate using the internal clock, which is fixed at 20MHz. When CKLSEL = 0, the modulators operate using an external clock. In both modes, the clock is internally divided by two and functions as the modulator clock. The frequency of the external clock can vary from 1MHz to 24MHz to adjust for the clock requirements of the application.

The modulator topology is a second-order, switched-capacitor, $\Delta\Sigma$ modulator, such as the one conceptualized in Figure 23. The analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing analog voltages at X_2 and X_3 . The voltages at X_2 and X_3 are presented to the respective individual integrators. The output of these integrators progresses in a negative or positive direction. When the value of the signal at X_4 equals the comparator reference voltage, the output of the

comparator switches from low to high, or vice versa, depending on its original state. When the output value of the comparator switches direction, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X_6 , causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

DIGITAL OUTPUT

A differential input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of +2.3V produces a stream of ones and zeros that are high 92% of the time. A differential input of -2.3V produces a stream of ones and zeros that are high 8% of the time. The input voltage versus the output modulator signal is shown in Figure 24.

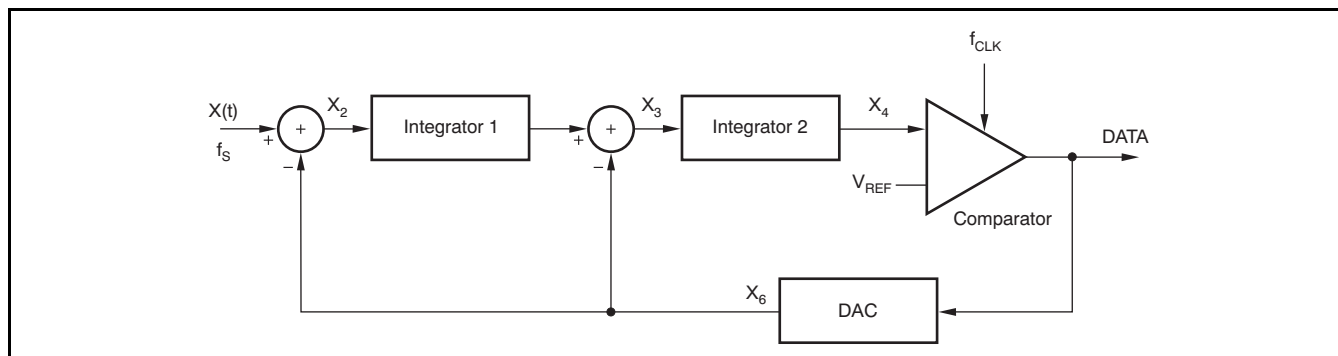


Figure 23. Block Diagram of the Second-Order Modulator

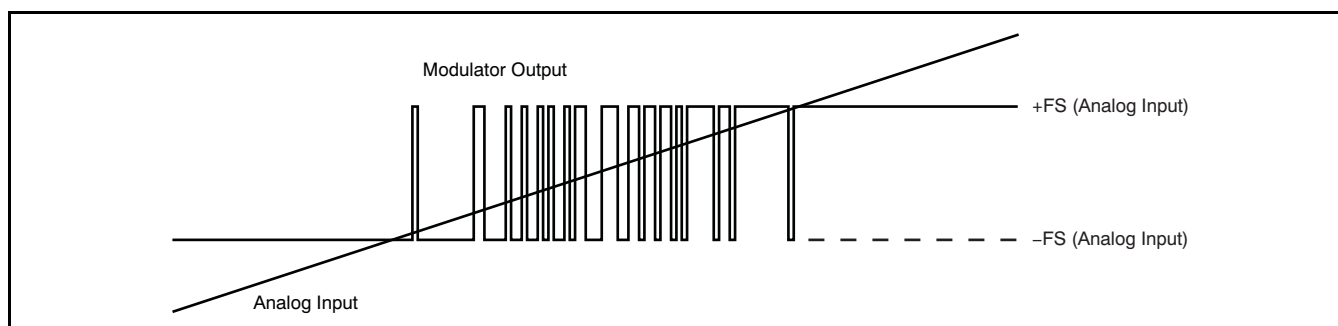


Figure 24. Analog Input vs Modulator Output of the ADS1209

DIGITAL INTERFACE

INTRODUCTION

The analog signal connected to the input of the $\Delta\Sigma$ modulator is converted using the clock signal applied to the modulator. The result of the conversion (or modulation) is available on one of the OUTx pins, depending on the modulator. In addition, a common clock output signal (CLKOUT) for both simultaneously-sampling modulators is provided. If CLKSEL = 1, CLKIN must not be left floating, but should be tied to BVDD or BGND.

MODES OF OPERATION

The device clock of the ADS1209 is 20MHz by default. The device clock can either be generated by the internal 20MHz RC oscillator or can be provided by an external clock source. For this purpose, the CLKIN pin is provided; it is controlled by the mode setting, CLKSEL.

The device clock is divided by two before being used as the modulator clock. Therefore, the default clock frequency of the modulator is 10MHz. With a possible external clock range of 1MHz to 24MHz, the modulator operates between 500kHz and 12MHz.

FILTER USAGE

The modulator generates a bitstream. In order to output a digital word equivalent to the analog input voltage, the bitstream must be processed by a digital filter.

A simple filter, built with minimal effort and hardware, is the Sinc³ filter shown in Equation 2:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance with a relatively low number of gates required for implementation. For oversampling ratios in the range of 16 to 256, this filter architecture represents a good choice. All the characterizations in this data sheet are done using a Sinc³ filter with an oversampling ratio of OSR = 256 and an output word width of 16 bits.

In a Sinc³ filter response (shown in Figure 25 and Figure 26), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{MOD}/OSR$. The -3dB point is located at half the Nyquist frequency or $f_{DATA}/4$.

This behavior can be adjusted by a cascaded filter structure. For example, the first decimation stage can be a Sinc³ filter with a low OSR, and the second stage a high-order filter.

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

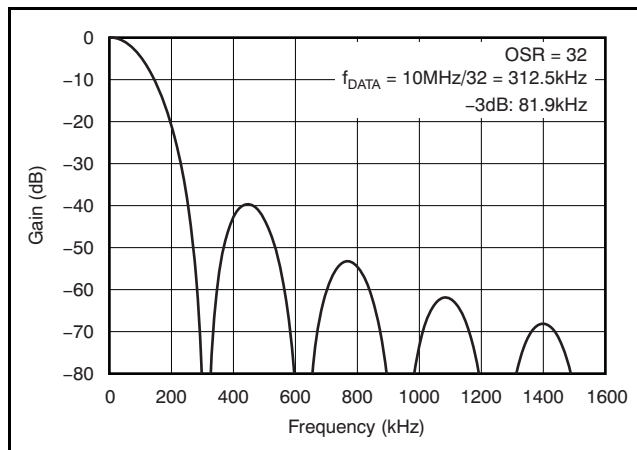


Figure 25. Frequency Response of Sinc³ Filter (OSR = 32)

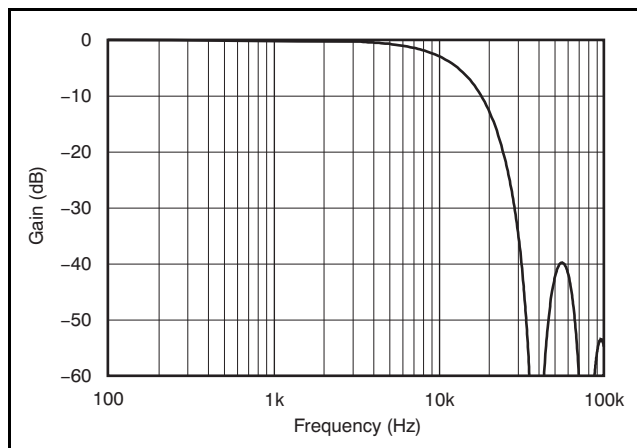


Figure 26. Frequency Response of Sinc³ Filter (OSR = 256)

The effective number of bits (ENOB) can be used to compare the performance of A/D converters and $\Delta\Sigma$ modulators. Figure 27 shows the ENOB of the ADS1209 with different filter types. In this data sheet, the ENOB is calculated from the SNR as shown in Equation 3:

$$\text{SNR} = 1.76\text{dB} + 6.02\text{dB} \times \text{ENOB} \quad (3)$$

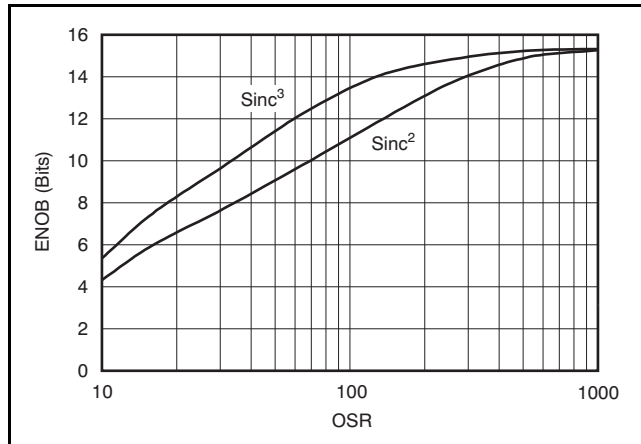


Figure 27. Measured ENOB vs OSR

In motor-control applications, a very fast response time is required for overcurrent detection. There is a constraint between $1\mu\text{s}$ and $5\mu\text{s}$ with 3 bits to 7 bits of resolution. The time for full settling depends on the filter order. Therefore, the full settling of the Sinc^3 filter requires three data clocks and the Sinc^2 filter requires two data clocks. The data clock is equal to

the modulator clock divided by the OSR. For overcurrent protection, filter types other than Sinc^3 may be a better choice. A simple example is a Sinc^2 filter. The Sincfast is a modified Sinc^2 filter as Equation 4 shows:

$$H(z) = \left(\frac{1 - z^{-\text{OSR}}}{1 - z^{-1}} \right)^2 (1 + z^{-2 \times \text{OSR}}) \quad (4)$$

Figure 28 compares the settling time of different filter types operating with a 10MHz modulator clock.

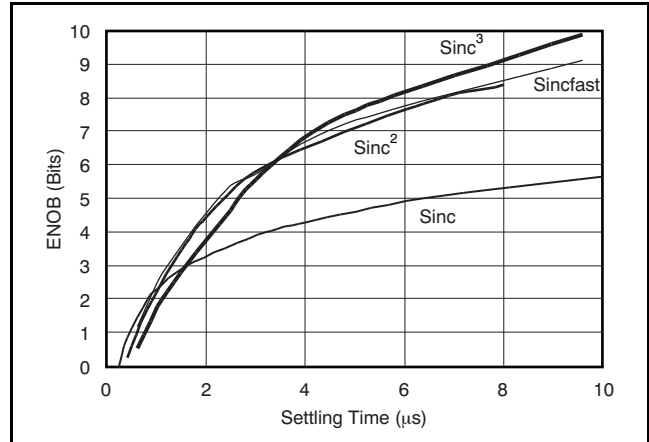


Figure 28. Measured ENOB vs Settling Time

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

LAYOUT CONSIDERATIONS

POWER SUPPLIES

An applied external digital filter rejects high-frequency noise. PSRR and CMRR improve at higher frequencies because the digital filter suppresses high-frequency noise. However, the suppression of the filter is not infinite while high-frequency noise continues to influence the conversion result.

Inputs to the ADS1209, such as CHx+, CHx–, and CLKIN, should not be present before the power supply is on. Violating this condition could cause latch-up. If these signals are present before the supply is on, series resistors should be used to limit the input current to a maximum of 10mA.

GROUNDING

Analog and digital sections of the design must be carefully and cleanly partitioned. Each section should have its own ground plane with a connection between them underneath the converter.

For multiple converters, connect the two ground planes as close as possible to each of the converters.

DECOUPLING

Good decoupling practices must be used for the ADS1209 and for all components in the design. All decoupling capacitors, specifically the 0.1 μ F ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1 μ F and 10 μ F capacitor, in parallel with the 0.1 μ F ceramic capacitor, can be used to decouple AVDD to AGND as well as BVDD to BGND. At least one 0.1 μ F ceramic capacitor must be used to decouple every AVDD to AGND and BVDD to BGND, as well as for the digital supply on each digital component.

The digital supply sets the I/O voltage for the interface and can be set within a range of 2.7V to 5.5V.

In cases where both the analog and digital I/O supplies share the same supply source, an RC filter of 10 Ω and 0.1 μ F can be used to help reduce the noise in the analog supply.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| ADS1209SPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1209SPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

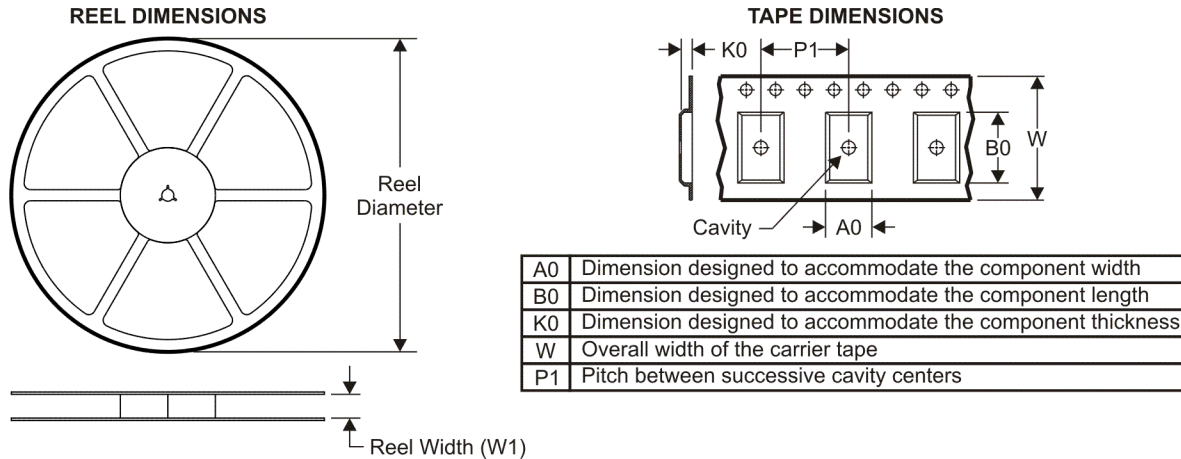
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS1209SPWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

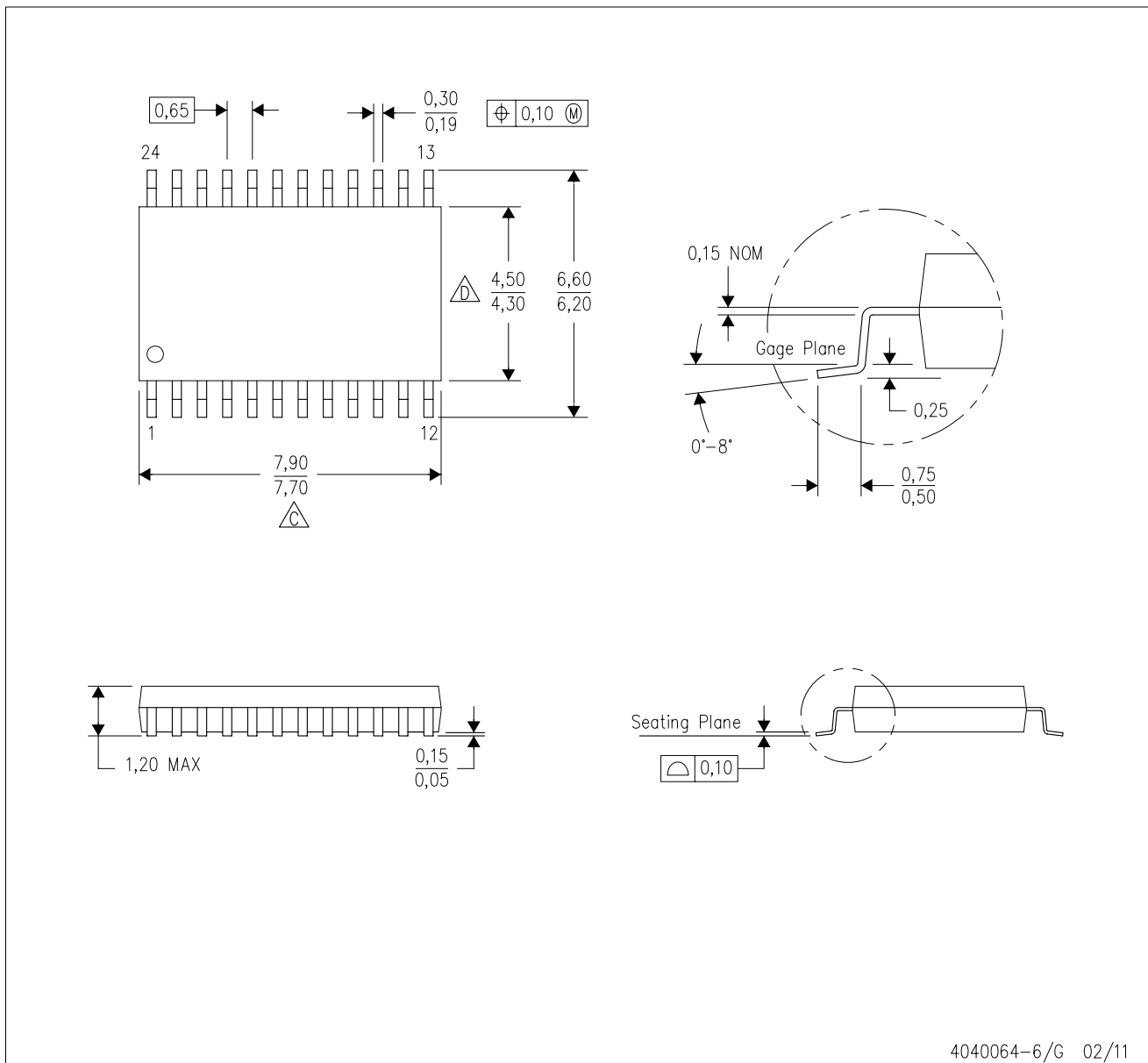


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS1209SPWR | TSSOP | PW | 24 | 2000 | 346.0 | 346.0 | 33.0 |

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

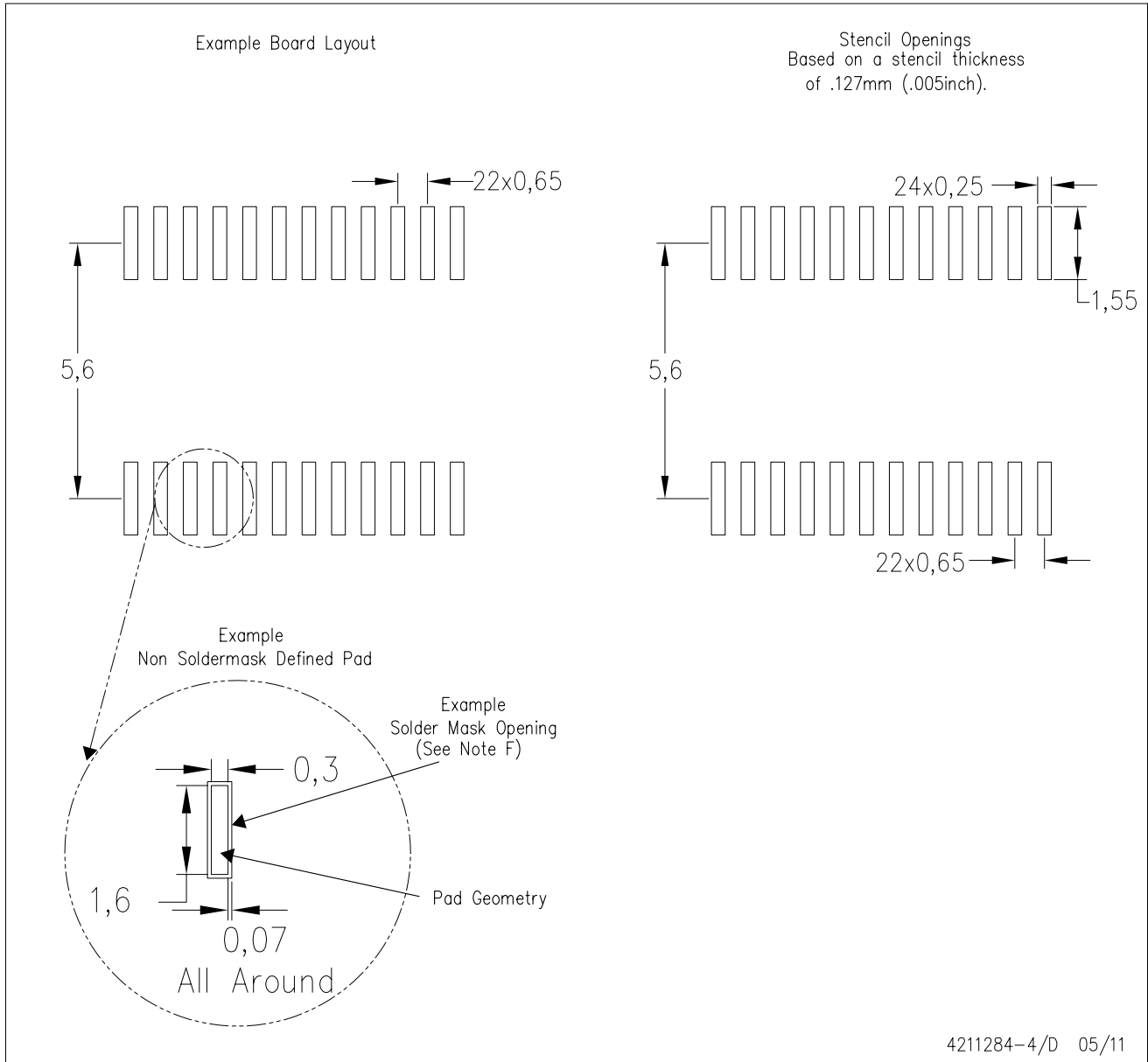


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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