18 V, Precision, 725 μA, 4 MHz CMOS RRIO Operational Amplifier

Preliminary Technical Data

ADA4666-2

FEATURES

Low power at high voltage (18 V): 725 μA maximum
Low offset voltage:
- **100 μV maximum at V_{CM}/2**
- **350 μV maximum over entire common mode range**

Low input bias current: 10 pA maximum
Gain bandwidth product: xxx kHz at A_V = 100 typical
Unity-gain crossover: 4.5MHz typical
−3 dB closed-loop bandwidth: xxx MHz typical
Single-supply operation: 3 V to 18 V
Dual-supply operation: ±1.5 V to ±9 V
Unity-gain stable

APPLICATIONS

Portable equipment
Current monitors
Buffer/level shifting
Active filters
High impedance sensor interface
Battery powered instrumentation

GENERAL DESCRIPTION

The ADA4666-2 is a dual, low power, rail-to-rail input/output amplifier optimized for 4 MHz, low power and wide operating supply voltage range applications.

The ADA4666-2 performance is guaranteed at 3.0 V, 10 V, and 18 V power supply voltages. It is an excellent selection for applications using single ended supplies of 3.3V, 5V, 10V, 12V and 15V and dual supplies of ±2.5V, ±3.3V and ±5V. It uses Analog Devices, Inc., patented DigiTrim® trimming technique, which achieves low offset voltage.

The ADA4666-2 is specified over the extended industrial temperature range (−40°C to +125°C) and is available in an 8-lead MSOP and LFCSP (3mm x 3mm) packages.

PIN CONNECTION DIAGRAMS

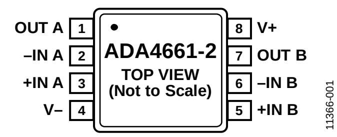

Figure 1. 8-Lead MSOP

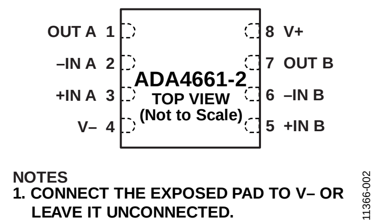

Figure 2. 8-Lead LFCSP

For ADA4666-2 pin connections and for more information about the pin connections for this part, see the **Error! Reference source not found.** section.

Table 1. Precision Low Power Op Amps (<1 mA)

Supply Voltage	5 V	12 V to 16 V	36 V
Single	ADA4505-1 AD8500		OP196
Dual	ADA4505-2 AD8502 AD8506	AD8657 AD8646 ADA4661-2	ADA4096-2 OP296
Quad	ADA4505-4 AD8504 AD8508	AD8659 AD8648	ADA4096-4 OP496

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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V_{SY} = 18 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$			150	µV
		V_{CM} = 1.5 V to 16.5 V			150	µV
		V_{CM} = 0 V to 18 V			300	µV
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C			1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.6	2.1	µV/°C
Input Bias Current	I_B			TBD	3	pA
		−40°C ≤ T_A ≤ +125°C			TBD	nA
Input Offset Current	I_{OS}				3	pA
		−40°C ≤ T_A ≤ +125°C			TBD	pA
Input Voltage Range			0		18	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 18 V	100	118		dB
		V_{CM} = 1.5 V to 16.5 V	115	135		dB
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C	TBD			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to 17.5 V	120	147		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Input Resistance	R_{IN}			TBD		GΩ
Input Capacitance, Differential Mode	C_{INDM}			TBD		pF
Input Capacitance, Common Mode	C_{INCM}			TBD		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	17.95	17.976		V
		−40°C ≤ T_A ≤ +125°C	TBD			V
		R_L = 1 kΩ to V_{CM}	17.6	17.79		V
		−40°C ≤ T_A ≤ +125°C	TBD			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		14	25	mV
		−40°C ≤ T_A ≤ +125°C		TBD		mV
		R_L = 1 kΩ to V_{CM}		120	200	mV
		−40°C ≤ T_A ≤ +125°C		TBD		mV
Short-Circuit Current	I_{SC}			±20		mA
Closed-Loop Output Impedance	Z_{OUT}	f = TBD kHz, A_V = 1		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		630	725	µA
		−40°C ≤ T_A ≤ +125°C			TBD	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 10 pF, A_V = 1		2.2		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 100		TBD		kHz
Unity-Gain Crossover	UGC	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		4.5		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\,dB}$	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		TBD		kHz
Phase Margin	Φ_M	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		TBD		Degrees
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		TBD		µs
Channel Separation	CS	f = 10 kHz, R_L = 10 kΩ		TBD		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV_{PEAK}; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		TBD		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	G= +1, f = 20 Hz to 20 kHz, V_{IN} = TBD @ X kHz				
BW = 80 kHz				TBD		%
BW = 500 kHz				TBD		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		TBD		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		TBD		pA/√Hz

ELECTRICAL CHARACTERISTICS—10 V OPERATION

V_{SY} = 10 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_{SY}/2			150	µV
		V_{CM} = 1.5 V to 8.5 V			150	µV
		V_{CM} = 0 V to 10 V			300	µV
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C			1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.6	2.1	µV/°C
Input Bias Current	I_B			0.9	15	pA
		−40°C ≤ T_A ≤ +125°C			TBD	nA
Input Offset Current	I_{OS}				30	pA
		−40°C ≤ T_A ≤ +125°C			TBD	pA
Input Voltage Range			0		10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 10 V	95	114		dB
		V_{CM} = 1.5 V to 8.5 V	115	140		dB
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C	TBD			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to 9.5 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Input Resistance	R_{IN}			TBD		GΩ
Input Capacitance, Differential Mode	C_{INDM}			TBD		pF
Input Capacitance, Common Mode	C_{INCM}			TBD		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	9.96	9.985		V
		−40°C ≤ T_A ≤ +125°C	TBD			V
		R_L = 1 kΩ to V_{CM}	9.7	9.88		V
		−40°C ≤ T_A ≤ +125°C	TBD			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		9.4	15	mV
		−40°C ≤ T_A ≤ +125°C		TBD		mV
		R_L = 1 kΩ to V_{CM}		77	110	mV
		−40°C ≤ T_A ≤ +125°C		TBD		mV
Short-Circuit Current	I_{SC}			±20		mA
Closed-Loop Output Impedance	Z_{OUT}	f = TBD kHz, A_V = 1		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		620	725	µA
		−40°C ≤ T_A ≤ +125°C			TBD	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 10 pF, A_V = 1		2.2		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 100		TBD		kHz
Unity-Gain Crossover	UGC	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		4.5		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		TBD		kHz
Phase Margin	Φ_M	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		TBD		Degrees
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		TBD		µs
Channel Separation	CS	f = 10 kHz, R_L = 10 kΩ		TBD		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV peak; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		TBD		dB
NOISE PERFORMANCE						

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise	THD+N	G= +1, f = 20Hz to 20kHz, V_{IN} = TBD @ X kHz				
BW = 80 kHz				TBD		%
BW = 500 kHz				TBD		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		TBD		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		TBD		pA/√Hz

ELECTRICAL CHARACTERISTICS—2.7 V OPERATION

V_{SY} = 3.0 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_{SY}/2		30	150	µV
		V_{CM} = 0 V to 3.0 V			300	µV
		V_{CM} = 0 V to 3.0 V; −40°C ≤ T_A ≤ +125°C			1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.6	2.1	µV/°C
Input Bias Current	I_B			0.5	8	pA
		−40°C ≤ T_A ≤ +125°C			TBD	nA
Input Offset Current	I_{OS}				16	pA
		−40°C ≤ T_A ≤ +125°C			TBD	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3.0 V	85	100		dB
		V_{CM} = 0 V to 3.0 V; −40°C ≤ T_A ≤ +125°C	TBD			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to 2.5 V	105	130		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Input Resistance	R_{IN}			>TBD		GΩ
Input Capacitance, Differential Mode	C_{INDM}			TBD		pF
Input Capacitance, Common Mode	C_{INCM}			TBD		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.98	2.99		V
		−40°C ≤ T_A ≤ +125°C	TBD			V
		R_L = 1 kΩ to V_{CM}	2.9	2.96		V
		−40°C ≤ T_A ≤ +125°C	TBD			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		4	8	mV
		−40°C ≤ T_A ≤ +125°C		TBD		mV
		R_L = 1 kΩ to V_{CM}		25	40	mV
		−40°C ≤ T_A ≤ +125°C		TBD		mV
Short-Circuit Current	I_{SC}			±20		mA
Closed-Loop Output Impedance	Z_{OUT}	f = TBD kHz, A_V = 1		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		615	725	µA
		−40°C ≤ T_A ≤ +125°C			TBD	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 10 pF, A_V = 1		2.2		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 100		TBD		kHz
Unity-Gain Crossover	UGC	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		4.5		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		TBD		kHz
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		TBD		µs
Phase Margin	Φ_M	V_{IN} = 10mVp-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		TBD		Degrees
Channel Separation	CS	f = 10 kHz, R_L = 10 kΩ		TBD		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV_{PEAK}; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		TBD		dB
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	G= +1, f = 20Hz to 20kHz, V_{IN} = TBD @ X kHz				

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BW = 80 kHz				TBD		%
BW = 500 kHz				TBD		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		TBD		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<TBD		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	20.5 V
Input Voltage	(V−) − 300 mV to (V+) + 300 mV
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Temperature Range	
Storage	−65°C to +150°C
Operating	−40°C to +125°C
Junction	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Human Body Model[2]	TBD
Machine Model[3]	TBD
Field-Induced Charge-Device Model[4]	TBD

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.
[2] Applicable Standard MIL-STD-883, Method 3015.7.
[3] Applicable Standard JESD22-A115-A (ESD MM standard of JEDEC).
[4] Applicable Standard JESD22-C101-C (ESD FICDM standard of JEDEC).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer JEDEC board. The exposed pad (LFCSP packages only) is soldered to the board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-xx)	TBD	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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