Low Cost, DC to 150 MHz Variable Gain Amplifier

AD8330

FEATURES

Fully differential signal path, also used with single-sided signals
Inputs from 0.3 mV to 1 V rms, rail-to-rail outputs
Differential R_{IN} = 1 kΩ; R_{OUT} (each output) 75 Ω
Automatic offset compensation (optional)
Linear-in-dB and linear-in-magnitude gain modes
0 dB to 50 dB, for 0 V < V_{DBS} < 1.5 V (30 mV/dB)
Inverted gain mode: 50 dB to 0 dB at −30 mV/dB
×0.03 to ×10 nominal gain for 15 mV < V_{MAG} < 5 V
Constant bandwidth: 150 MHz at all gains
Low noise: 5 nV/√Hz typical at maximum gain
Low distortion: ≤−62 dBc typical
Low power: 20 mA typical at V_S of 2.7 V to 6 V
Available in a space-saving, 3 mm × 3 mm LFCSP package

APPLICATIONS

Pre-ADC signal conditioning
75 Ω cable driving adjust
AGC amplifiers

FUNCTIONAL BLOCK DIAGRAM

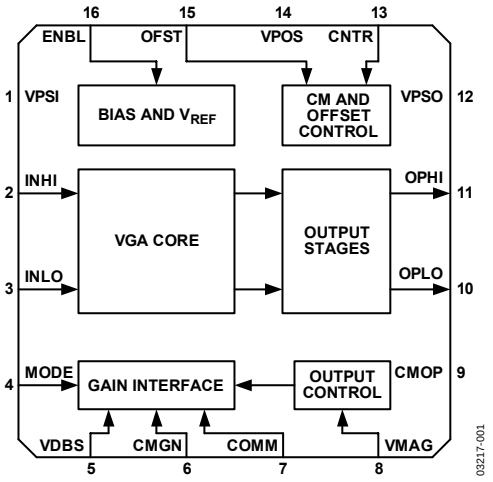


Figure 1.

GENERAL DESCRIPTION

The AD8330[1] is a wideband variable gain amplifier for applications requiring a fully differential signal path, low noise, well-defined gain, and moderately low distortion, from dc to 150 MHz. The input pins can also be driven from a single-ended source. The peak differential input is ±2 V, allowing sine wave operation at 1 V rms with generous headroom. The output pins can drive single-sided loads essentially rail-to-rail. The differential output resistance is 150 Ω. The output swing is a linear function of the voltage applied to the VMAG pin that internally defaults to 0.5 V, providing a peak output of ±2 V. This can be raised to 10 V p-p, limited by the supply voltage.

The basic gain function is linear-in-dB, controlled by the voltage applied to Pin VDBS. The gain ranges from 0 dB to 50 dB for control voltages between 0 V and 1.5 V—a slope of 30 mV/dB. The gain linearity is typically within ±0.1 dB. By changing the logic level on Pin MODE, the gain decreases over the same range, with an opposite slope. A second gain control port is provided at the VMAG pin and allows the user to vary the numeric gain from a factor of 0.03 to 10. All the parameters of the AD8330 have low sensitivities to temperature and supply voltages.

[1] Protected by U.S. Patent No. 5,969,657; other patents pending.

Using VMAG, the basic 0 dB to 50 dB range can be repositioned to any value from 20 dB higher (that is, 20 dB to 70 dB) to at least 30 dB lower (that is, −30 dB to +20 dB) to suit the application, thereby providing an unprecedented gain range of over 100 dB. A unique aspect of the AD8330 is that its bandwidth and pulse response are essentially constant for all gains, over both the basic 50 dB linear-in-dB range, but also when using the linear-in-magnitude function. The exceptional stability of the HF response over the gain range is of particular value in those VGA applications where it is essential to maintain accurate gain law-conformance at high frequencies.

An external capacitor at Pin OFST sets the high-pass corner of an offset reduction loop, whose frequency can be as low as 5 Hz. When this pin is grounded, the signal path becomes dc-coupled. When used to drive an ADC, an external common-mode control voltage at Pin CNTR can be driven to within 0.5 V of either ground or V_S to accommodate a wide variety of requirements. By default, the two outputs are positioned at the midpoint of the supply, $V_S/2$. Other features, such as two levels of power-down (fully off and a hibernate mode), further extend the practical value of this exceptionally versatile VGA.

The AD8330 is available in 16-lead LFCSP and 16-lead QSOP packages and is specified for operation from −40°C to +85°C.

Rev. D

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, C_L = 12 pF on OPHI and OPLO, R_L = ∞, V_{DBS} = 0.75 V, V_{MODE} = high, V_{MAG} = Pin VMAG open circuit (0.5 V), V_{OFST} = 0 V, differential operation, unless otherwise noted.

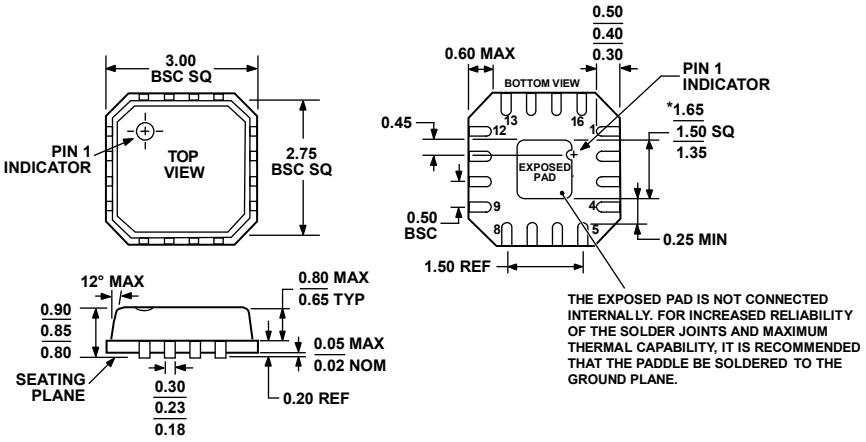
Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT INTERFACE	Pin INHI, Pin INLO				
Full-Scale Input	V_{DBS} = 0 V, differential drive	±1.4	±2		V
	V_{DBS} = 1.5 V	±4.5	±6.3		mV
Input Resistance	Pin-to-pin	800	1 k	1.2 k	Ω
Input Capacitance	Either pin to COMM		4		pF
Voltage Noise Spectral Density	f = 1 MHz, V_{DBS} = 1.5 V; inputs ac-shorted		5		nV/√Hz
Common-Mode Voltage Level			3.0		V
Input Offset	Pin OFST connected to Pin COMM		1		mV rms
Drift			2		µV/°C
Permissible CM Range[1]		0		V_S	V
Common-Mode AC Rejection	f = 1 MHz, 0.1 V rms		−60		dB
	f = 50 MHz		−55		dB
OUTPUT INTERFACE	Pin OPHI, Pin OPLO				
Small Signal −3 dB Bandwidth	0 V < V_{DBS} < 1.5 V		150		MHz
Peak Slew Rate	V_{DBS} = 0 V		1500		V/µs
Peak-to-Peak Output Swing		±1.8	±2	±2.2	V
	V_{MAG} ≥ 2 V (peaks are supply limited)	±4	±4.5		V
Common-Mode Voltage	Pin CNTR O/C	2.4	2.5	2.6	V
Voltage Noise Spectral Density	f = 1 MHz, V_{DBS} = 0 V		62		nV/√Hz
Differential Output Impedance	Pin-to-pin	120	150	180	Ω
HD2[2]	V_{OUT} = 1 V p-p, f = 10 MHz, R_L = 1 kΩ		−62		dBc
HD3[2]	V_{OUT} = 1 V p-p, f = 10 MHz, R_L = 1 kΩ		−53		dBc
OUTPUT OFFSET CONTROL	Pin OFST				
AC-Coupled Offset	C_{HPF} on Pin OFST (0 V < V_{DBS} < 1.5 V)		10		mV rms
High-Pass Corner Frequency	C_{HPF} = 3.3 nF, from OFST to CNTR (scales as 1/C_{HPF})		100		kHz
COMMON-MODE CONTROL	Pin CNTR				
Usable Voltage Range		0.5		4.5	V
Input Resistance	From Pin CNTR to V_S/2		4		kΩ
DECIBEL GAIN CONTROL	VDBS, CMGN, and MODE pins				
Normal Voltage Range	CMGN connected to COMM		0 to 1.5		V
Elevated Range	CMGN O/C (V_{CMGN} rises to 0.2 V)		0.2 to 1.7		V
Gain Scaling	Mode high or low	27	30	33	mV/dB
Gain Linearity Error	0.3 V ≤ V_{DBS} ≤ 1.2 V	−0.35	±0.1	+0.35	dB
Absolute Gain Error	V_{DBS} = 0 V	−2	±0.5	+2	dB
Bias Current	Flows out of Pin VDBS		100		nA
Incremental Resistance			100		MΩ
Gain Settling Time to 0.5 dB Error	V_{DBS} stepped from 0.05 V to 1.45 V or 1.45 V to 0.05 V		250		ns
Mode Up/Down	Pin MODE				
Mode Up Logic Level	Gain increases with V_{DBS}, MODE = O/C	1.5			V
Mode Down Logic Level	Gain decreases with V_{DBS}			0.5	V
LINEAR GAIN INTERFACE	Pin VMAG, Pin CMGN				
Peak Output Scaling, Gain vs. V_{MAG}	See the Circuit Description section	3.8	4.0	4.2	V/V
Gain Multiplication Factor vs. V_{MAG}	Gain is nominal when V_{MAG} = 0.5 V		×2		
Usable Input Range		0		5	V
Default Voltage	V_{MAG} O/C	0.48	0.5	0.52	V
Incremental Resistance			4		kΩ
Bandwidth	For V_{MAG} ≥ 0.1 V		150		MHz

Parameter	Conditions	Min	Typ	Max	Unit
CHIP ENABLE	Pin ENBL				
Logic Voltage for Full Shutdown				0.5	V
Logic Voltage for Hibernate Mode	Output pins remain at CNTR	1.3	1.5	1.7	V
Logic Voltage for Full Operation		2.3			V
Current in Full Shutdown			20	100	μA
Current in Hibernate Mode			1.5		mA
Minimum Time Delay[3]			1.7		μs
POWER SUPPLY	VPSI, VPOS, VPSO, COMM, and CMOP pins				
Supply Voltage		2.7		6	V
Quiescent Current	V_{DBS} = 0.75 V		20	27	mA

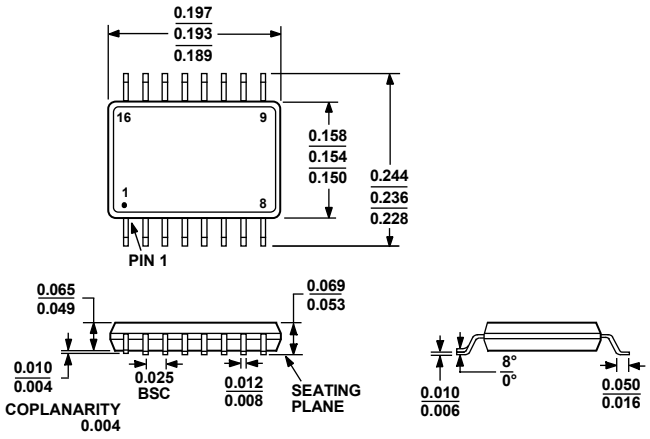
[1] The use of an input common-mode voltage significantly different from the internally set value is not recommended due to its effect on noise performance. See Figure 56.
[2] See the Typical Performance Characteristics section for more detailed information on distortion in a variety of operating conditions.
[3] For minimum sized coupling capacitors.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 78. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137-AB

Figure 79. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8330ACP-R2	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFA
AD8330ACP-REEL	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFA
AD8330ACP-REEL7	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFA
AD8330ACPZ-R2[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFZ
AD8330ACPZ-RL[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFZ
AD8330ACPZ-R7[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFZ
AD8330ARQ	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQ-REEL	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQ-REEL7	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQZ[1]	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQZ-RL[1]	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQZ-R7[1]	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330-EVAL		Evaluation Board		
AD8330-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.