ACPL-064L, ACPL-M61L, ACPL-W61L, ACPL-K64L

Ultra Low Power 10 MBd Digital CMOS Optocouplers

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The Avago ultra low power ACPL-x6xL digital optocouplers combine an AlGaAs light emitting diode (LED) and an integrated high gain photodetector. The optocoupler consumes extremely low power, at maximum 1.3mA I_{DD} current per channel across temperature. With a forward LED current as low as 1.6 mA most microprocessors can directly drive the LED.

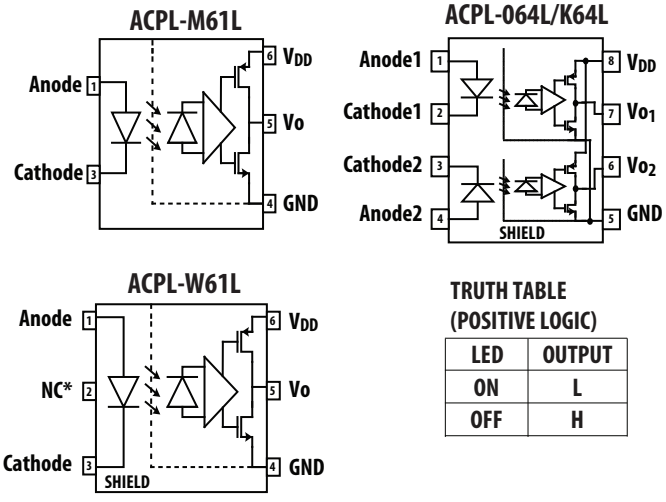
An internal Faraday shield provides a guaranteed common mode transient immunity specification of 20 kV/µs. Maximum AC and DC circuit isolation is achieved while maintaining TTL/CMOS compatibility.

The optocouplers CMOS outputs are slew-rate controlled and is designed to allow the rise and fall time to be controlled over a wide load capacitance range.

The ACPL-x6xL series operates from both 3.3 V and 5 V supply voltages with guaranteed AC and DC performance from –40°C to +105°C.

These low-power optocouplers are suitable for high speed logic interface applications.

Functional Diagrams



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

A 0.1 µF bypass capacitor must be connected between pins V_{DD} and GND.

Features

- Ultra-low I_{DD} current: 1.3 mA/channel maximum
- Low input current: 1.6 mA
- Built-in slew-rate controlled outputs
- 20 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V
- High speed: 10 MBd minimum
- Guaranteed AC and DC performance over wide temperature: –40°C to +105°C
- Wide package selection: SO-5, SO-8, stretched SO-6 and stretched SO-8
- Safety approval
  - UL 1577 recognized – 3750 Vrms for 1 minute for ACPL-064L/M61L and 5000 Vrms for 1 minute for ACPL-W61L/K64L
  - CSA Approval
  - IEC/EN/DIN EN 60747-5-5 approval for Reinforced Insulation
- RoHS compliant

Applications

- Communication interfaces: RS485, CANBus and I^2C
- Microprocessor system interfaces
- Digital isolation for A/D and D/A convertors

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

The ACPL-064L and ACPL-M61L are UL Recognized with an isolation voltage of 3750 V_{rms} for 1 minute per UL1577. The ACPL-W61L and ACPL-K64L are UL Recognized with an isolation voltage of 5000 V_{rms} for 1 minute per UL1577. All devices are RoHS compliant.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	UL1577 5000 Vrms /1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-M61L	-000E	SO-5	X				100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1500 per reel
	-560E		X	X		X	1500 per reel
ACPL-064L	-000E	SO-8	X				100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1500 per reel
	-560E		X	X		X	1500 per reel
ACPL-W61L	-000E	Stretched S06	X		X		100 per tube
	-060E		X		X	X	100 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K64L	-000E	Stretched S08	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To form an ordering part number, choose a part number from the part number column and combine it with the desired option from the option column.

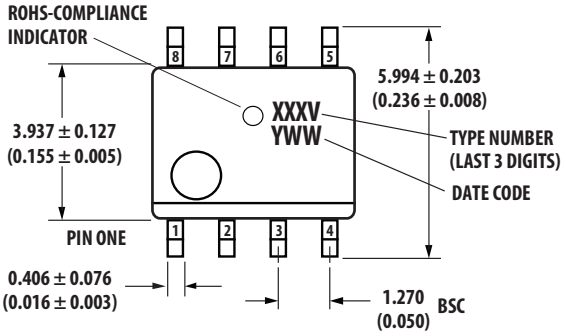
Example 1:

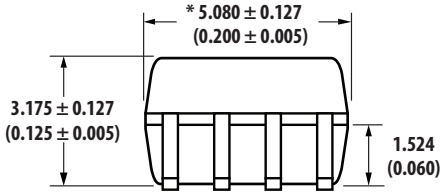
The part number ACPL-M61L-560E describes an optocoupler with a surface mount SO-5 package; delivered in Tape and Reel with 1500 parts per reel; with IEC/EN/DIN EN 60747-5-5 Safety Approval; and full RoHS compliance.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

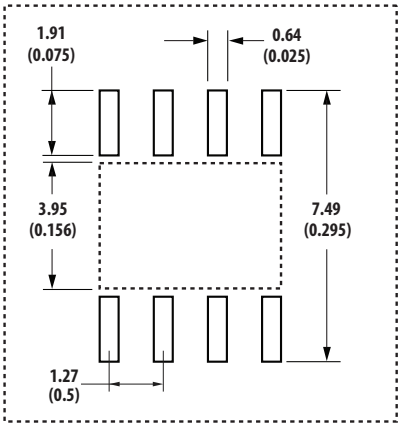
Package Outline Drawings

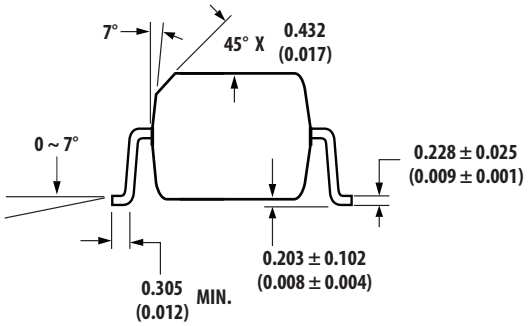
ACPL-064L SO-8 Package





LAND PATTERN RECOMMENDATION



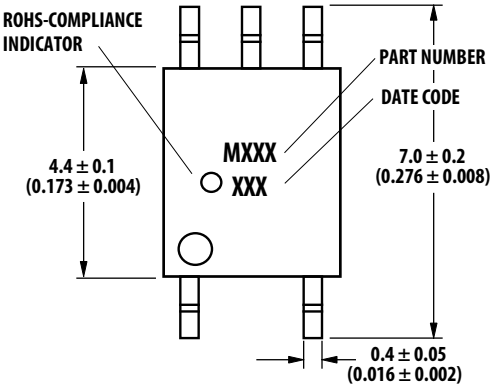


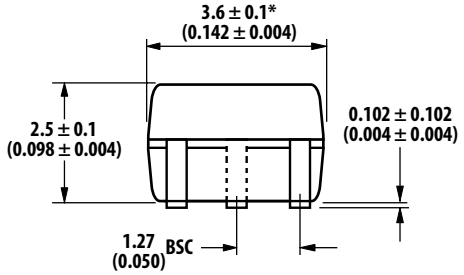
* Total package length (inclusive of mold flash) 5.207 ± 0.254 (0.205 ± 0.010)

Dimensions in Millimeters (Inches).

Note: Floating lead protrusion is 0.15 mm (6 mils) max.
Lead coplanarity = 0.10 mm (0.004 inches) max.
Option number 500 not marked.

ACPL-M61L SO-5 Package





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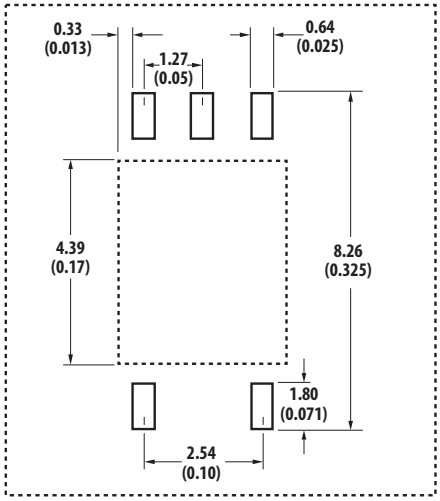
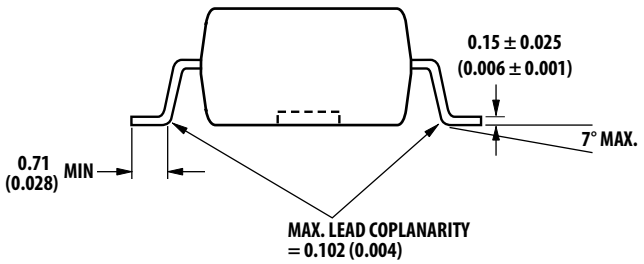
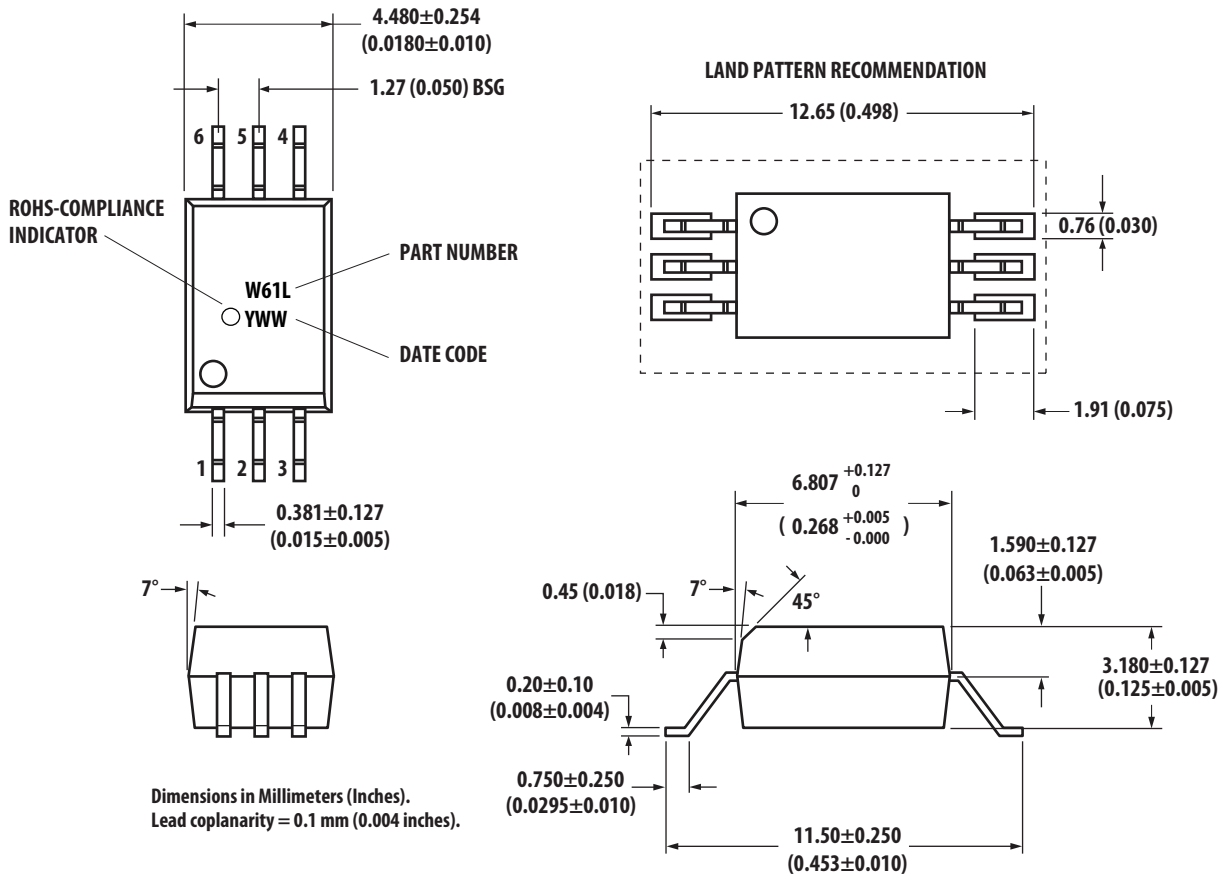




Dimensions in millimeters (inches).
Note: Foating Lead Protrusion is 0.15 mm (6 mils) max.

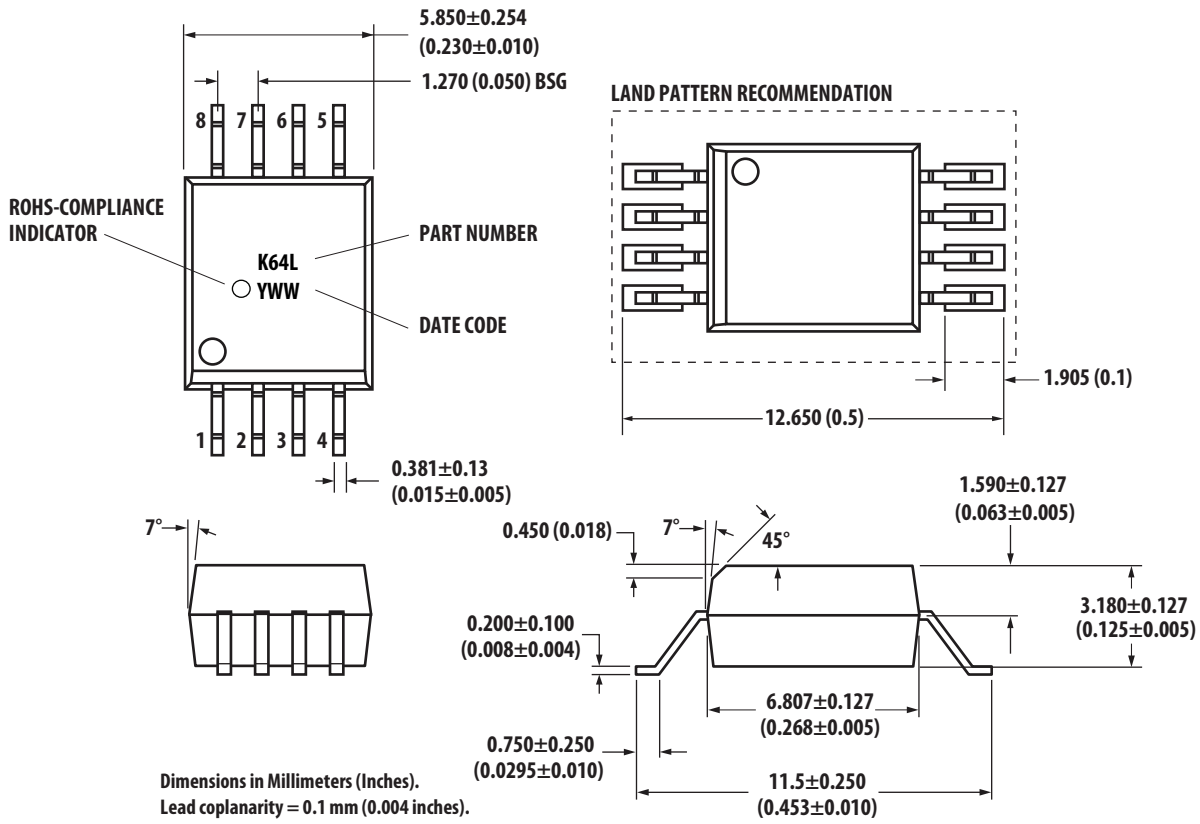
* Maximum Mold flash on each side is 0.15 mm (0.006).

ACPL-W61L Stretched SO-6 Package



Dimensions in Millimeters (Inches).
Lead coplanarity = 0.1 mm (0.004 inches).

ACPL-K64L Stretched SO-8 Package



Dimensions in Millimeters (Inches).
Lead coplanarity = 0.1 mm (0.004 inches).

Reflow Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-064L, ACPL-M61L, ACPL-W61L and ACPL-K64L are approved by the following organizations:

IEC/EN/DIN EN 60747-5-5 (Option 060 only)

UL

Approval under UL 1577 component recognition program up to V_{ISO} = 3750 V_{RMS} for the ACPL-M61L/064L and V_{ISO} = 5000 V_{RMS} for the ACPL-W61L/K64L File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

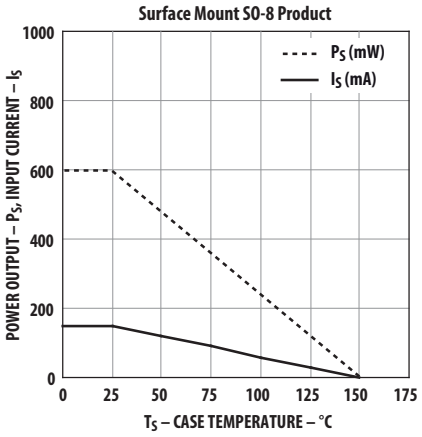
Parameter	Symbol	ACPL-064L	ACPL-M61L	ACPL-W61L ACPL-K64L	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	4.9	5	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	4.8	5	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	175	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

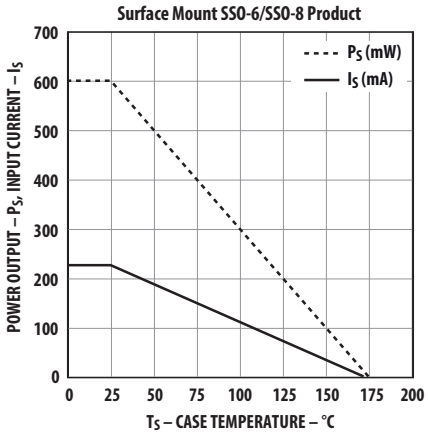
IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 060)

Description	Symbol	Characteristic ACPL-064L/ ACPL-M61L	Characteristic ACPL-W61L/ ACPL-K64L	Unit
Installation classification per DIN VDE 0110/39, Table 1				
for rated mains voltage ≤ 150 V_{rms}		I – IV	I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – III	I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – II	I – III	
for rated mains voltage ≤ 1000 V_{rms}			I – III	
Climatic Classification		55/105/21	55/105/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	567	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m =1 sec, Partial discharge < 5 pC	V_{PR}	1063	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	907	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.				
Case Temperature	T_S	150	175	°C
Input Current**	$I_{S, INPUT}$	150	230	mA
Output Power**	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figures for dependence of P_S and I_S on ambient temperature.





Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Condition
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Reverse Input Voltage	V_R		5	V	
Supply Voltage	V_{DD}		6.5	V	
Average Forward Input Current	I_F	–	8	mA	
Peak Forward Input Current (I_F at 1 µs pulse width, <10% duty cycle)	$I_{F(TRAN)}$	–	1	A	≤1 µs Pulse Width, <300 pulses per second
			80	mA	≤1 µs Pulse Width, <10% Duty Cycle
Output Current	I_O		10	mA	
Output Voltage	V_O	–0.5	V_{DD} +0.5	V	
Input Power Dissipation	P_I		14	mW	
Output Power Dissipation	P_O		20	mW	
Lead Solder Temperature	T_{LS}		260°C for 10 sec., 1.6 mm below seating plane		
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Operating Temperature	T_A	- 40	105	°C
Input Current, Low Level	I_{FL}	0	250	µA
Input Current, High Level	I_{FH}	1.6	6.0	mA
Power Supply Voltage	V_{DD}	2.7	5.5	V
Forward Input Voltage	$V_{F\ (OFF)}$		0.8	V

Electrical Specifications (DC)

Over the recommended temperature (T_A = –40°C to +105°C) and supply voltage (2.7 V ≤ V_{DD} ≤ 5.5 V). All typical specifications are at V_{DD} = 5 V and T_A = 25°C.

Parameter	Symbol	Channel	Min	Typ	Max	Units	Test Conditions
Input Forward Voltage	V_F		0.95	1.3	1.7	V	I_F = 2 mA Figure 1, 2
Input Reverse Breakdown Voltage	BV_R		3	5		V	I_R = 10 µA
Logic High Output Voltage	V_{OH}		V_{DD} - 0.1	V_{DD}		V	I_F = 0 mA, V_I = 0 V (R_T = 1.68 kΩ) or (R_T = 870 Ω), I_O = -20 µA
			V_{DD} - 1.0	V_{DD}		V	I_F = 0 mA, V_I = 0 V (R_T = 1.68 kΩ) or (R_T = 870 Ω), I_O = -3.2 mA
Logic Low Output Voltage	V_{OL}			0.03	0.1	V	I_F = 2 mA, V_I = 5 V (R_T = 1.68 kΩ) or V_I = 3.3V (R_T = 870 Ω), I_O = 20 µA
				0.18	0.4	V	I_F = 2 mA, V_I = 5 V (R_T = 1.68 kΩ) or V_I = 3.3V (R_T = 870 Ω), I_O = 3.2 mA
Input Threshold Current	I_{TH}			0.7	1.3	mA	Figure 3
Logic Low Output Supply Current	I_{DDL}	Single		0.8	1.3	mA	Figure 4
		Dual		1.6	2.6		
Logic High Output Supply Current	I_{DDH}	Single		0.8	1.3	mA	Figure 5
		Dual		1.6	2.6		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$			-1.6		mV/°C	I_F = 2 mA

Switching Specifications (AC)

Over the recommended temperature (T_A = –40°C to +105°C) and supply voltage (2.7 V ≤ V_{DD} ≤ 5.5 V). All typical specifications are at V_{DD} = 5 V, T_A = 25°C.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Propagation Delay Time to Logic Low Output [1]	t_{PHL}		46	80	ns	I_F = 2 mA, V_I = 5 V, R_T = 1.68 kΩ, C_L = 15 pF, CMOS Signal Levels.
Propagation Delay Time to Logic High Output [1]	t_{PLH}		40	80	ns	I_F = 2 mA, V_I = 3.3 V, R_T = 870 Ω, C_L = 15 pF, CMOS Signal Levels.
Pulse Width	t_{PW}	100			ns	
Pulse Width Distortion[2]	PWD		6	30	ns	Figure 6,7
Propagation Delay Skew [3]	t_{PSK}			30	ns	
Output Rise Time (10% – 90%)	t_R		12		ns	I_F = 2 mA, V_I = 5 V, R_T = 1.68 kΩ, C_L = 15 pF, CMOS Signal Levels.
			10		ns	I_F = 2 mA, V_I = 3.3 V, R_T = 870 Ω, C_L = 15 pF, CMOS Signal Levels.
Output Fall Time (90% - 10%)	t_F		12		ns	I_F = 2 mA, V_I = 5 V, R_T = 1.68 kΩ, C_L = 15 pF, CMOS Signal Levels.
			10		ns	I_F = 2 mA, V_I = 3.3 V, R_T = 870 Ω, C_L = 15 pF, CMOS Signal Levels.
Static Common Mode Transient Immunity at Logic High Output [4]	$\lvert CM_H \rvert$	20	35		kV/µs	V_{CM} = 1000 V, T_A = 25°C, I_F = 0 mA, V_I = 0 V (R_T =1.68 kΩ) or (R_T = 870Ω), C_L = 15 pF, CMOS Signal Levels. Figure 8
Static Common Mode Transient Immunity at Logic Low Output [5]	$\lvert CM_L \rvert$	20	35		kV/µs	V_{CM} = 1000 V, T_A = 25°C, V_I = 5 V (R_T = 1.68 kΩ) or V_I = 3.3 V (R_T = 870Ω), I_F = 2 mA, C_L= 15 pF, CMOS Signal Levels. Figure 8
Dynamic Common Mode Transient Immunity [6]	CMR_D		35		kV/µs	V_{CM} = 1000 V, T_A = 25°C, I_F = 2 mA, V_I = 5 V (R_T = 1.68 kΩ) or V_I = 3.3 V (R_T = 870Ω), 10MBd datarate, the absolute increase of PWD < 10ns Figure 8

Notes:

1. t_{PHL} propagation delay is measured from the 50% (V_{in} or I_F) on the rising edge of the input pulse to the 50% V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{in} or I_F) on the falling edge of the input pulse to the 50% level of the rising edge of the V_O signal.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$.
3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
4. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
5. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.
6. CM_D is the maximum tolerable rate of the common mode voltage during data transmission to assure that the absolute increase of the PWD is less than 10 ns.

Package Characteristics

All typicals are at T_A = 25°C.

Parameter	Symbol	Part Number	Min	Typ	Max	Units	Test Conditions
Input-Output Insulation	V_{ISO}	ACPL-064L ACPL-M61L	3750			V_{rms}	RH < 50% for 1 min. T_A = 25°C
		ACPL-W61L ACPL-K64L	5000				
Input-Output Resistance	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 V
Input-Output Capacitance	C_{I-O}			0.6		pF	f = 1 MHz, T_A = 25°C

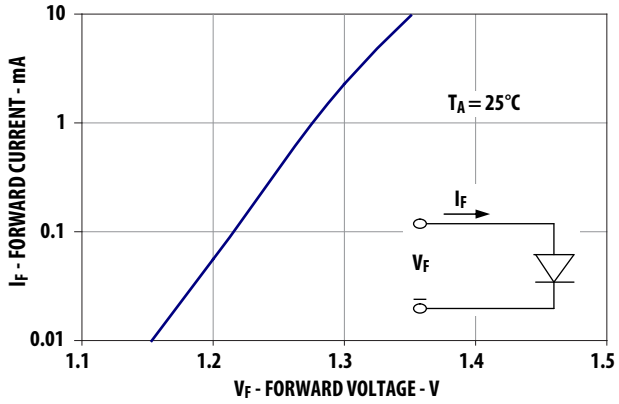


Figure 1. Typical input diode forward current characteristic

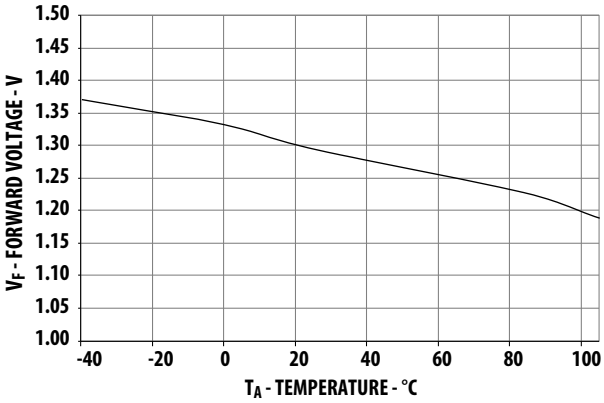


Figure 2. Typical V_F versus temperature

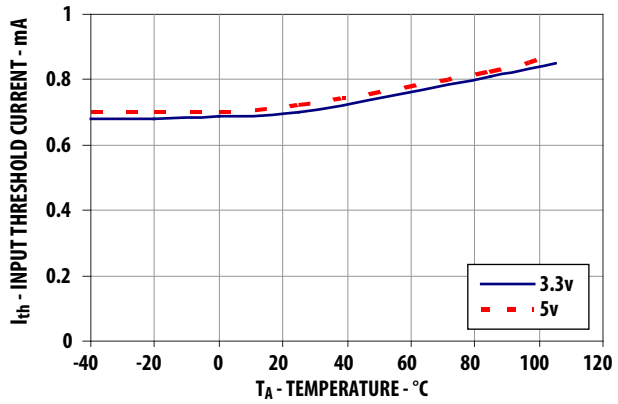


Figure 3. Typical input threshold current versus temperature

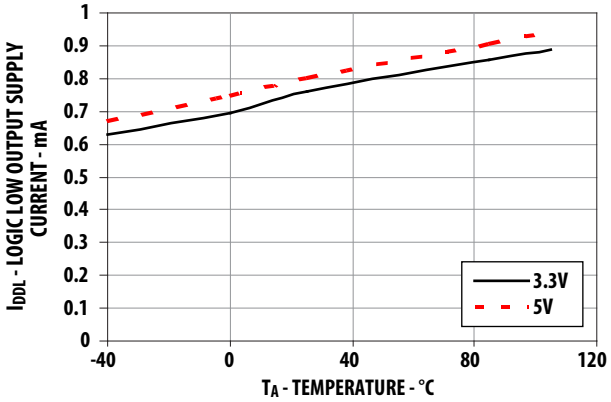


Figure 4. Typical logic low output supply current (per channel) versus temperature

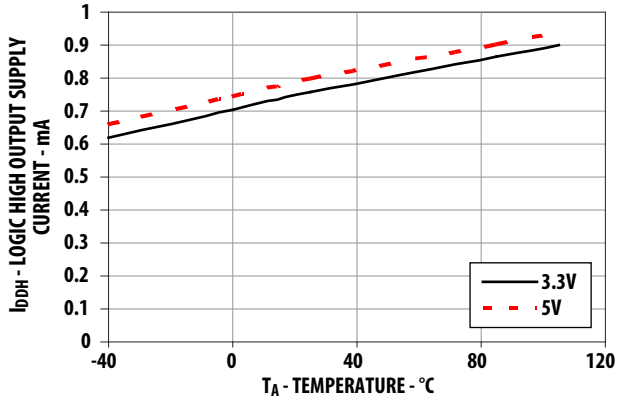


Figure 5. Typical logic high output supply current (per channel) versus temperature

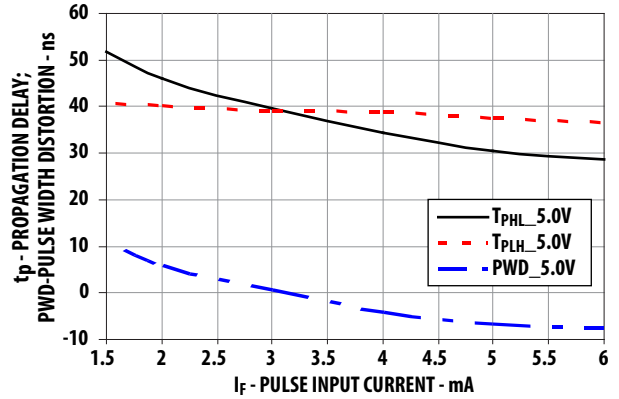


Figure 6. Typical switching speed versus pulse input with a 5 V supply voltage

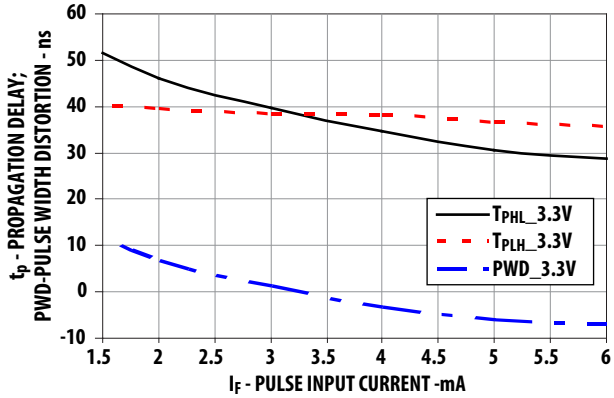


Figure 7. Typical switching speed versus pulse input current with a 3.3 V supply voltage

Supply Bypassing, LED Bias Resistors and PC Board Layout

The ACPL-x6xL optocouplers are extremely easy to use and feature high speed, push-pull CMOS outputs. Pull-up resistors are not required.

The external components required for proper operation are the input limiting resistors and the output bypass capacitor. Capacitor values should be 0.1 μF.

For each capacitor, the total lead length connecting the capacitor to the V_{DD} and GND pins should not exceed 20 mm.

For ACPL-M61L/W61L:

V_{DD} = 3.3 V: R_1 = 510 Ω ± 1%, R_2 = 360 Ω ± 1%

V_{DD} = 5.0 V: R_1 = 1000 Ω ± 1%, R_2 = 680 Ω ± 1%

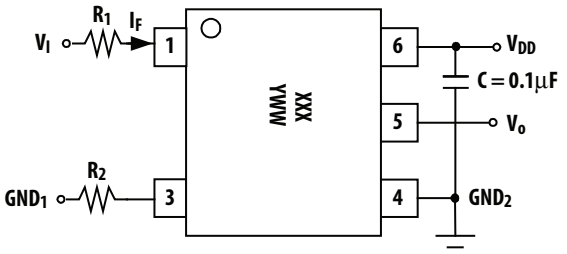
$R_T = R_1 + R_2$ $R_1/R_2 \approx 1.5$

For ACPL-064L/K64L:

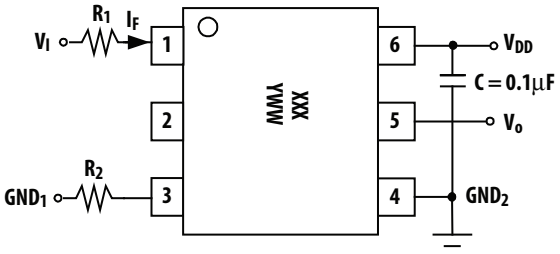
V_{DD} = 3.3 V: R_1 = 430 Ω ± 1%, R_2 = 430 Ω ± 1%

V_{DD} = 5.0 V: R_1 = 845 Ω ± 1%, R_2 = 845 Ω ± 1%

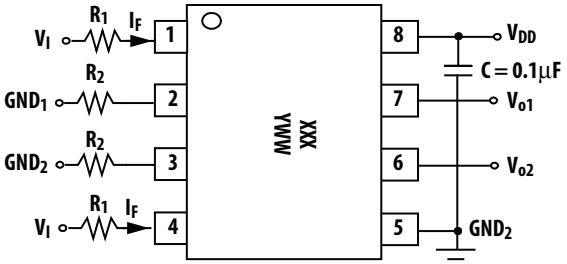
$R_T = R_1 + R_2$ $R_1/R_2 \approx 1$



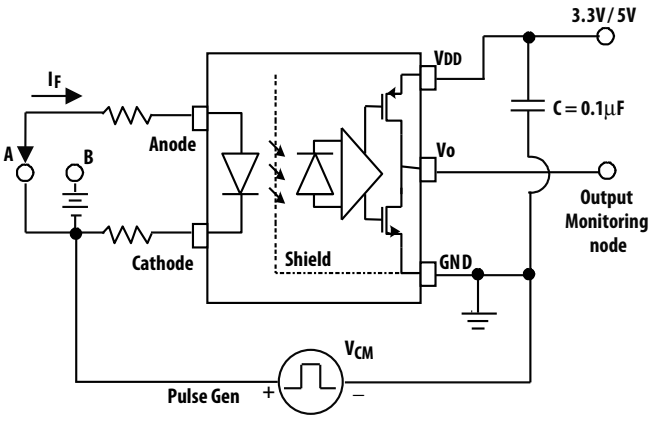
ACPL-M61L



ACPL-W61L



ACPL-064L/K64L



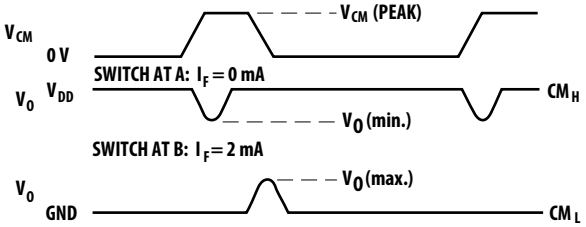


Figure 8. Recommended printed circuit board layout and input current limiting resistor selection.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low-to-high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high.

Similarly, the propagation delay from high-to-low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high-to-low (see Figure 9).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL}. PWD determines the maximum data rate of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, a PWD of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern.

If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As shown in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}. As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate.

Figure 10 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler.

Figure 10 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived.

From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

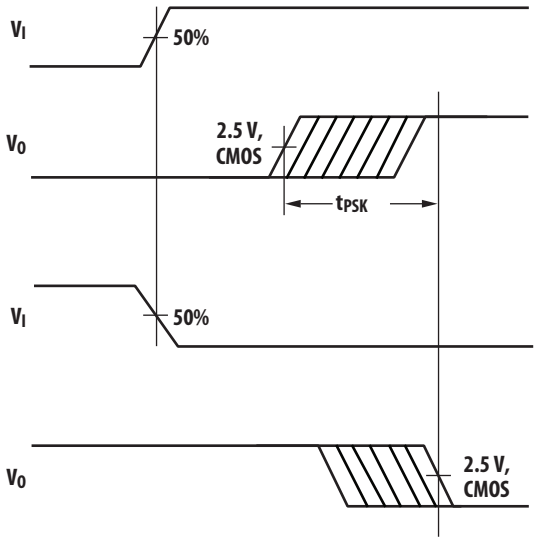


Figure 9. Propagation delay skew waveform

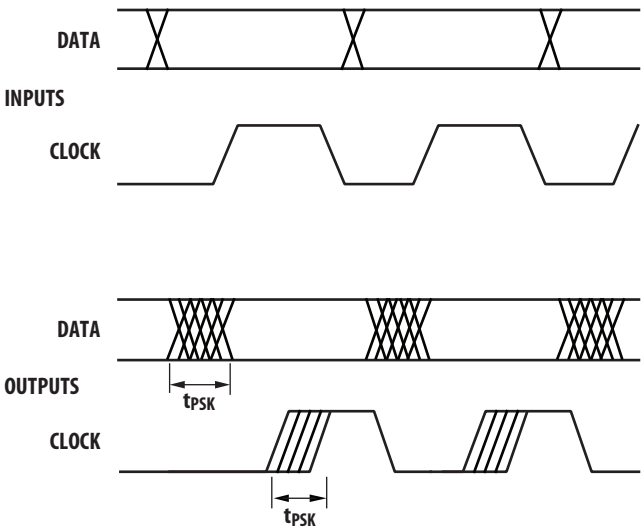


Figure 10. Parallel data transmission example

Optocoupler CMR Performance

The principal protection against common mode noise, comes from the fundamental isolation properties of the optocoupler, and this in turn is directly related to the Input-Output leakage capacitance of the optocoupler.

To provide maximum protection to circuitry connected to the input or output of the optocoupler the leakage capacitance is minimized by having large separation distances at all points in the optocoupler construction, including the LED/photodiode interface.

In addition to the optocouplers basic physical construction, additional circuit design steps mitigate the effects of common mode noise. The most important of these is the Faraday shield on the photodetector stage.

A Faraday shield is effective in optocouplers because the internal modulation frequency (light) is many orders of magnitude higher than the common mode noise frequency.

Improving CMR Performance at the Application Level

In an end application it desirable that the optocouplers common mode isolation be as close as possible to that indicated in the data sheet specifications. The first step in meeting this goal is to ensure maximum separation between PCB interconnects on either side of the optocoupler is maintained and that PCB tracks beneath the optocoupler are avoided.

It is inevitable that a certain amount of CMR noise will be coupled into the inputs and this can potentially result in false-triggering of the input. This problem is frequently observed in devices with input high input impedance. In some cases this can cause momentary missing pulses and may even cause input circuitry to latch-up in some alternate technologies.

The ACPL-x6xL optocoupler family does not have an input latch-up issue. Even at very high CMR levels such as those experienced in end equipment level tests (for example IEC61000-4-4) the ACPL-x6xL series is immune to latch-up because of the simple diode structure of the LED.

In some cases achieving the rated data sheet CMR performance level is not possible in an application. This is often because of the practical need to actually connect the isolator input to the output of a dynamically changing signal rather than tying the input statically to V_{DD} or GND. A data sheet CMR "specmanship" issue is often seen with alternative technology isolators that are based on AC encoding techniques.

To address the need to define achievable end application performance on data sheets, the ACPL-x6xL optocouplers include an additional typical performance specification for dynamic CMR in the electrical parameter table. The dynamic CMR specification indicates the typical achievable CMR performance as the input is being toggled on or off during a CMR transient.

The logic output the ACPL-x6xL optocouplers is mainly controlled by LED current level, and since the LED current features very fast rise and fall times, dynamic noise immunity is essentially the same as static noise immunity.

Despite their immunity to input latch-up and the excellent dynamic CMR immunity, ACPL-x6xL optocoupler devices are still potentially vulnerable to miss-operation caused by the LED being turned either on or off during a CMR disturbance. If the LED status could be ensured by design, the overall application level CMR performance would be that of the photodetector. To benefit from the inherently high CMR capabilities of the ACPL-x6xL family, some simple steps about operating the LED at the application level should be taken.

In particular, ensure that the LED stays either on or off during a CMR transient. Some common design techniques to accomplish this are:

Keep the LED On:

i) Overdrive the LED with a higher than required forward current.

Keep the LED Off:

i) Reverse bias the LED during the off state.

ii) Minimize the off-state impedance across the anode and cathode of the LED during the off state.

All these methods allow the full CMR capability of the ACPL-x6xL family to be achieved, but they do have practical implementation issues or require a compromise on power consumption.

There is, however, an effective method to meet the goal of maintaining the LED status during a CMR event with no other design compromises other than adding a single resistor.

This CMR optimization takes advantage of the differential connection to the LED. By ensuring the common mode impedances at both the cathode and anode of the LED are equal, the CMR transient on the LED is effectively canceled. As shown in Figure 11, this is easily achieved by using two, instead of one, input bias resistors.

Split LED Bias Resistor for Optimum CMR

Figure 11 shows the recommended drive circuit for the ACPL-x6xL that gives optimum common-mode rejection. The two current setting resistors balance the common mode impedances at the LED's anode and cathode. Common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which is not wanted when the LED should be on) or conversely cause current to be injected into the LED (which is not wanted when the LED should be off).

Figure 12 shows the parasitic capacitances (C_{LA} and C_{LC}) between the LED's anode and cathode, and output ground. Also shown in Figure 12 on the input side is an AC-equivalent circuit.

Table 1 shows the directions of I_{LP} and I_{LN} depend on the polarity of the common-mode transient. For transients occurring when the LED is on, common-mode rejection (CM_L, since the output is at "low" state) depends on LED current (I_F). For conditions where I_F is close to the switching threshold (I_{TH}), CM_L also depends on the extent to which I_{LP} and I_{LN} balance each other. In other words, any condition where a common-mode transient causes a momentary decrease in I_F (i.e. when $dV_{CM}/dt > 0$ and $|I_{FP}| > |I_{FN}|$, referring to Table 1). will cause a common-mode failure for transients which are fast enough.

Likewise for a common-mode transient that occurs when the LED is off (i.e. CM_H, since the output is at "high" state), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient "signal" may cause the output to spike below 2 V, which constitutes a CM_H failure.

The resistors recommended in Figure 11 include both the output impedance of the logic driver circuit and the external limiting resistor. The balanced I_{LED}-setting resistors help equalize the common mode voltage change at the anode and cathode. This reduces I_{LED} changes caused by transient coupling through the parasitic capacitors C_{LA} and C_{LC} shown in Figure 12.

For ACPL-M61L/W61L:

V_{DD} = 3.3 V: R_1 = 510 Ω ± 1%, R_2 = 360 Ω ± 1%

V_{DD} = 5.0 V: R_1 = 1000 Ω ± 1%, R_2 = 680 Ω ± 1%

$R_T = R_1 + R_2$ $R_1/R_2 \approx 1.5$

For ACPL-064L/K64L:

V_{DD} = 3.3 V: R_1 = 430 Ω ± 1%, R_2 = 430 Ω ± 1%

V_{DD} = 5.0 V: R_1 = 845 Ω ± 1%, R_2 = 845 Ω ± 1%

$R_T = R_1 + R_2$ $R_1/R_2 \approx 1$

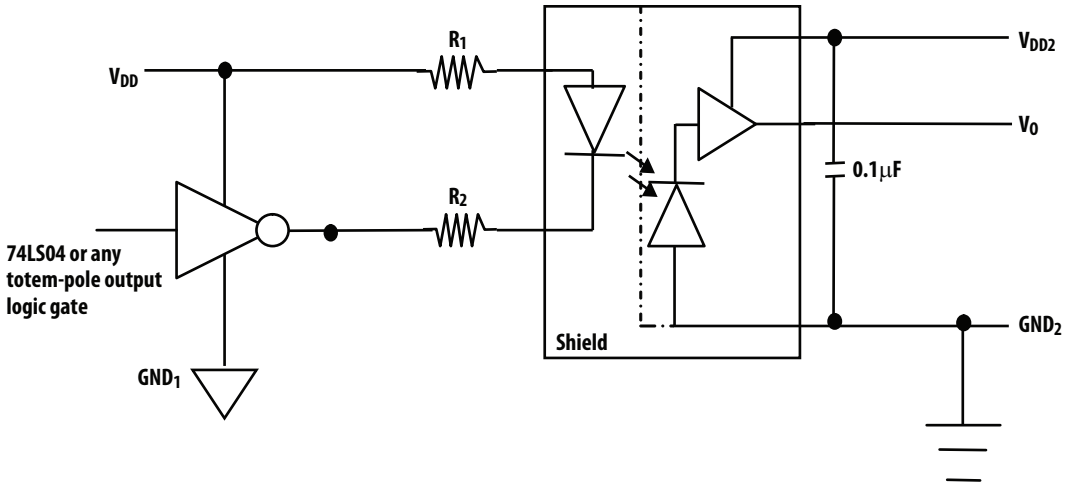


Figure 11. Recommended high-CMR drive circuit for the ACPL-x6xL.

For ACPL-M61L/W61L:
V_{DD} = 3.3 V: R_1 = 510 Ω ± 1%, R_2 = 360 Ω ± 1%
V_{DD} = 5.0 V: R_1 = 1000 Ω ± 1%, R_2 = 680 Ω ± 1%
$R_T = R_1 + R_2$ $R_1/R_2 \approx 1.5$

For ACPL-064L/K64L:
V_{DD} = 3.3 V: R_1 = 430 Ω ± 1%, R_2 = 430 Ω ± 1%
V_{DD} = 5.0 V: R_1 = 845 Ω ± 1%, R_2 = 845 Ω ± 1%
$R_T = R_1 + R_2$ $R_1/R_2 \approx 1$

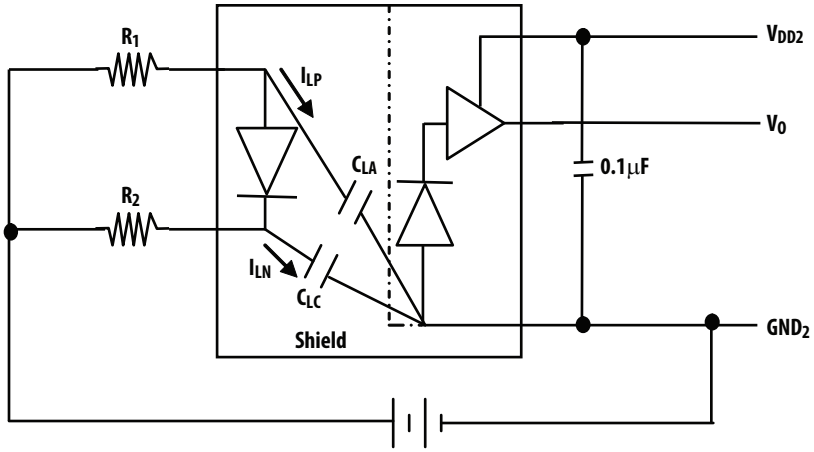


Figure 12. AC equivalent circuit of ACPL-x6xL.

Table 1. Common Mode Pulse Polarity and LED Current Transients

If dV_{CM}/dt Is:	Then I_{LP} flows:	and I_{LN} flows:	If $\|I_{LP}\| < \|I_{LN}\|$ LED current I_F is momentarily:	If $\|I_{LP}\| > \|I_{LN}\|$ LED Current I_F is momentarily:
positive (> 0)	away from the LED anode through C_{LA}	away from the LED cathode through C_{LC}	increased	decreased
negative (< 0)	toward the LED anode through C_{LA}	toward the LED cathode through C_{LC}	decreased	increased

Glitch Free Power-up and Power-Down Feature.

Upon Powering-up or Powering-down of the optocoupler, glitches produced in the output are undesirable. Glitches can lead to false data in the optocoupler application. ACPL-x6xL has a feature that holds the output in a known state until V_{DD} is at a safe level. Figure 13 and 14 show typical output waveforms during Power-up and Power-down process.

Slew-rate controlled outputs Feature

Typically, the output slew rate (rise and fall time) will vary with the output load, as more time is needed to charge up the higher load. The propagation delay and the PWD will increase with the load capacitance. This will be an issue especially in parallel communication because different communication line will have different load capacitances. However, Avago's new optocoupler ACPL-x6xL has built in slew-rate controlled feature, to ensure that the output rise and fall time remain stable across wide load capacitance. Figure 15 shows the rise time and fall time for ACPL-x6xL at 3.3V and 5V.

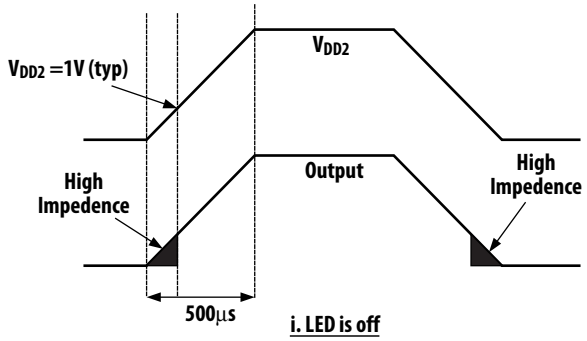


Figure 13. V_{DD} Ramp when LED is off.

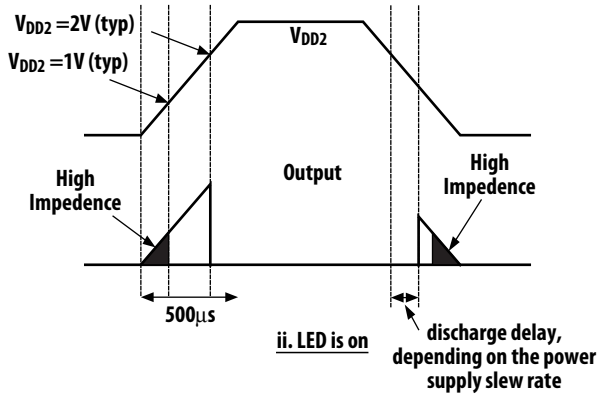
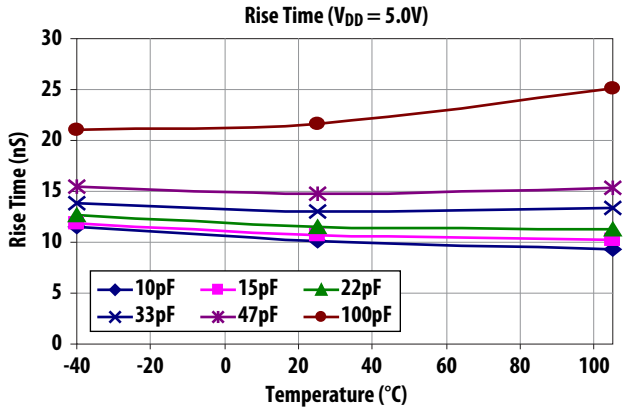
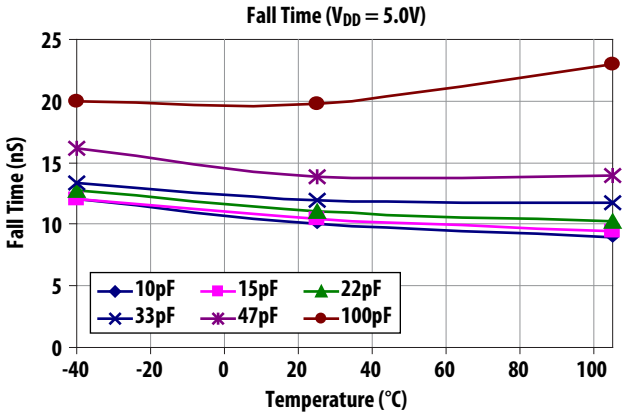
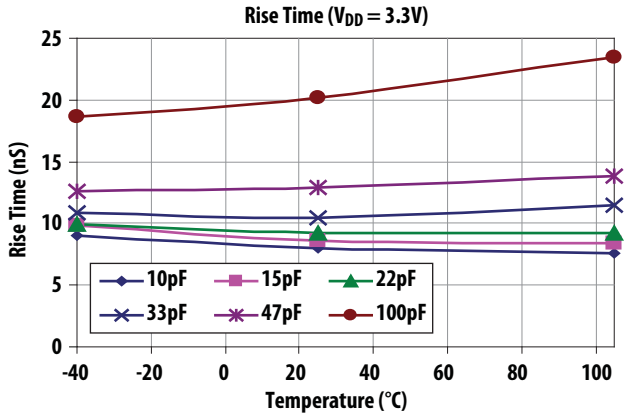


Figure 14. V_{DD} Ramp when LED is on.







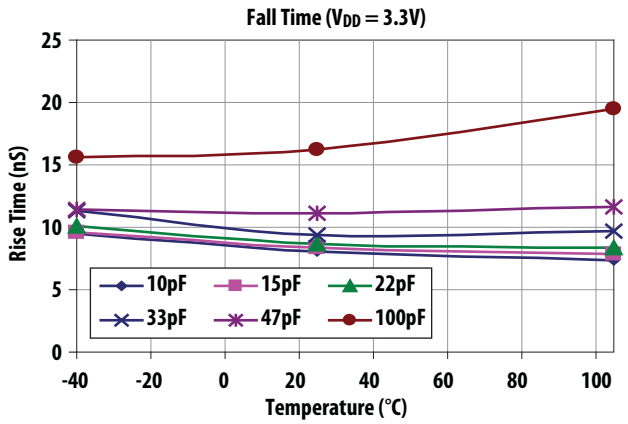


Figure 15. Rise and Fall time of ACPL-x6xL across wide load capacitance

Speed Improvement

A peaking capacitor can be placed across the input current limit resistor (Figure 16) to achieve enhanced speed performance. The value of the peaking cap is dependent to the rise and fall time of the input signal and supply voltages and LED input driving current (I_F). Figure 17 shows significant improvement of propagation delay and pulse with distortion with added peak capacitor at driving current of 2mA and 3.3V/5V power supply.

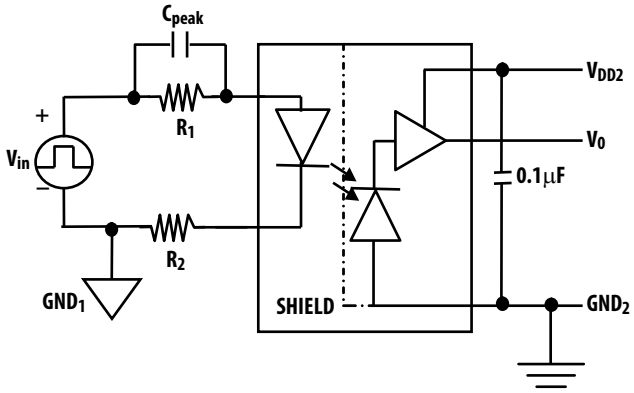
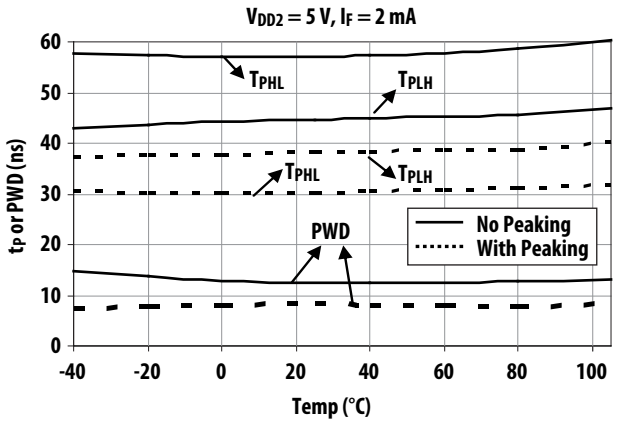
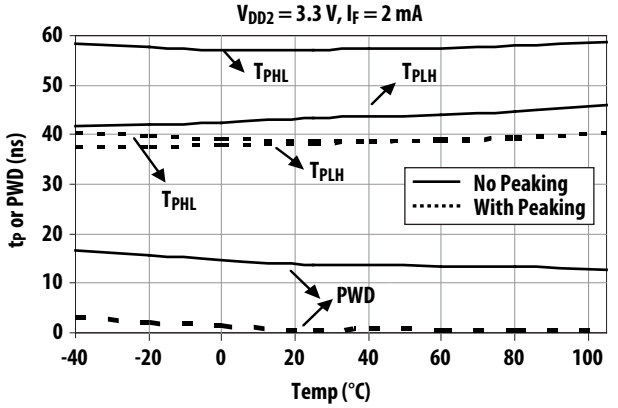


Figure 16. Connection of peaking capacitor (C_{peak}) in parallel of the input limiting resistor (R_1) to improve speed performance



(i) V_{DD} = 5V, C_{peak} = 47pF, R_1 = 845Ω



(ii) V_{DD} = 3.3V, C_{peak} = 47pF, R_1 = 430Ω

Figure 17. Improvement of t_p and PWD with added 100pF peaking capacitor in parallel of input limiting resistor.

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