

 <b>ABRACON</b> CORPORATION <i>the Power of Linking Together</i>	<b>AB08X5 Real-Time Clock Family</b>	 <b>RoHS</b> Compliant
<b>Date of Issue: September 16, 2014</b>	<b>3.0 x 3.0 mm</b>	 <b>ESD Sensitive</b>
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## Source Control Drawing




<b>Part Description:</b>	3 x 3 x 0.9 mm Ultra Low Power RTC IC User's Guide
<b>Customer Part Number:</b>	
<b>Abracon Part Number:</b>	

<b>Customer Approval</b> <b>(Please return this copy as a certification of your approval.)</b>	
<b>Approved By:</b>	
<b>Approval Date:</b>	




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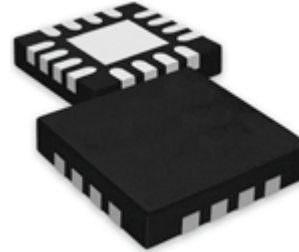
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Revision History							
Rev.	ECO	Description	Date	Prep'd By	Ck'd By	Ck'd By	Appr'd By
A		<ul style="list-style-type: none"> <li>- Added limits and/or temperature range specifications for the following parameters:  <math>V_{CC,ABS MAX}</math>, <math>V_{BAT,ABS MAX}</math>, <math>V_{CCIO}</math>, <math>V_{CCRST}</math>, <math>V_{CCSWR}</math>, <math>V_{CCSWF}</math>, <math>V_{CCRS}</math>, <math>V_{CCFS}</math>, <math>V_{BATRST}</math>, <math>V_{T+}</math>, <math>V_{T-}</math>, <math>I_{LEAK}</math>, <math>I_{OH}</math>, <math>I_{OL}</math>, <math>R_{DSON}</math>, <math>I_{OLEAK}</math>, <math>C_{EX}</math>, <math>O_{A XT}</math>, <math>F_{RC}</math>, <math>F_{RCU}</math>, <math>T_{AC}</math>, <math>I_{VCC: I2C}</math>, <math>I_{VCC: SPIW}</math>, <math>I_{VCC: SPIR}</math>, <math>I_{VCC: XT}</math>, <math>I_{VCC: RC}</math>, <math>I_{VCC: ACAL}</math>, <math>I_{VCC: CK32}</math>, <math>I_{VCC: CLK128}</math>, <math>I_{VBAT: XT}</math>, <math>I_{VBAT: RC}</math>, <math>I_{VBAT: ACAL}</math>, <math>I_{VBAT: VCC}</math>, <math>V_{BRF}</math>, <math>V_{BRR}</math>, <math>V_{BRH}</math>, <math>T_{BR}</math>, <math>I_{LOW: VCC}</math>, <math>I_{VL: FOUT}</math>, <math>I_{VH: FOUT}</math>, <math>I_{XTST}</math>, <math>I_{VL: NRST}</math>, <math>I_{VH: NRST}</math>, <math>I_{RL: NRST}</math>, <math>I_{RH: NRST}</math></li> <li>- Removed <math>t_{BREF}</math> parameter</li> <li>- Additional note on autocalibration operating temperature range in the electrical specification section</li> <li>- Added additional text to the Autocalibration Fail section</li> <li>- Updated XT digital calibration adjustment value equation</li> <li>- Removed <math>V_{CCRS}</math> parameter as there is no requirement for the <math>V_{CC}</math> rising slew rate</li> <li>- Added curves to the electrical specification section: VCC Current vs. Voltage in different operating modes, VCC Current vs. Voltage During I<sup>2</sup>C/SPI burst read/write, VCC Current vs. Voltage with 32.768kHz Clock Output, VBAT Current vs. Voltage in different operating modes, VBAT current vs. Voltage in VCC power state</li> <li>- Removed typ. values at 1.5V and 3.6V in VCC supply current table and replaced with VCC supply current vs. voltage curves</li> <li>- Removed typical values at 1.5V and 3.6V in VBAT supply current table and replaced with VBAT current vs. voltage curve</li> </ul>	10/31/2013	SR	YH	CB	JE
B		<ul style="list-style-type: none"> <li>- Reduced part selection to AB0805 and AB0815</li> <li>- Updated RCPLS value to be consistent across the datasheet</li> <li>- Renamed datasheet to AB08X5</li> </ul>	05/08/2014	SR	YH	CB	JE
C		<ul style="list-style-type: none"> <li>- Corrected a few typographical errors</li> <li>- Added additional text to PWGT bit description</li> <li>- Specified VCC voltage range for <math>I_{OLEAK}</math> parameter</li> <li>- Updated the AB0805 and AB0815 number of output pins in the Family Summary Table</li> <li>- Removed CLKOUT feature</li> <li>- Clarified pin descriptions in Table 3</li> </ul>	09/16/2014	SR	YH	CB	JE

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## Features

- Ultra-low supply current (all at 3V):
  - 14 nA with RC oscillator
  - 22 nA with RC oscillator and Autocalibration
  - 55 nA with crystal oscillator
- Baseline timekeeping features:
  - 32.768 kHz crystal oscillator with integrated load capacitor/resistor
  - Counters for hundredths, seconds, minutes, hours, date, month, year, century, and week-day
  - Alarm capability on all counters
  - Programmable output clock generation (32.768 kHz to 1 year)
  - Countdown timer with repeat function
  - Automatic leap year calculation
- Advanced timekeeping features:
  - Integrated power optimized RC oscillator
  - Advanced crystal calibration to  $\pm 2$  ppm
  - Advanced RC calibration to  $\pm 16$  ppm
  - Automatic calibration of RC oscillator to crystal oscillator
  - Watchdog timer with hardware reset
  - 256 bytes of general purpose RAM
- Power management features:
  - Automatic switchover to VBAT
  - External interrupt monitor
  - Programmable low battery detection threshold
  - Programmable analog voltage comparator
- I<sup>2</sup>C (up to 400 kHz) and 3-wire or 4-wire SPI (up to 2 MHz) serial interfaces available
- Operating voltage 1.5-3.6 V
- Clock and RAM retention voltage 1.5-3.6 V
- Operating temperature -40 to 85 °C
- All inputs include Schmitt Triggers
- 3x3 mm QFN-16 package






## Applications

- Smart cards
- Wireless sensors and tags
- Medical electronics
- Utility meters
- Data loggers
- Appliances
- Handsets
- Consumer electronics
- Communications equipment

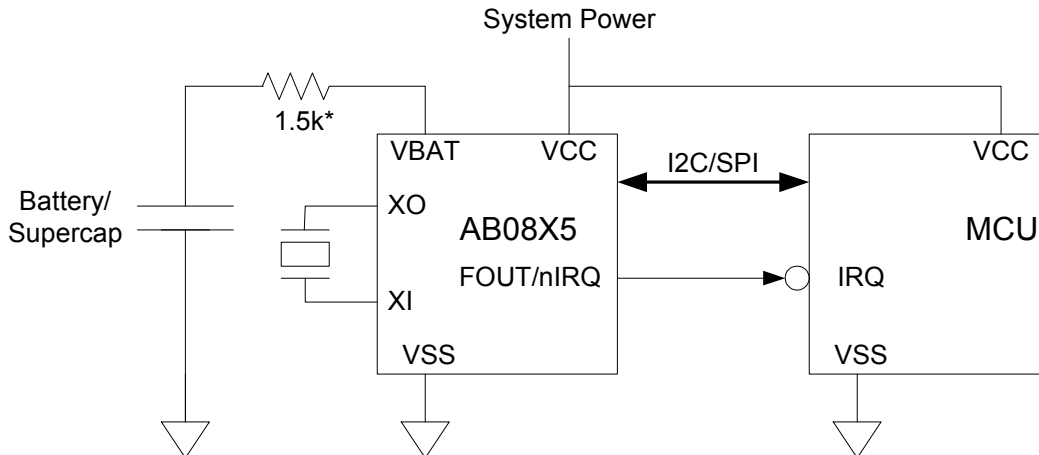
## Description

The ABRACON AB08X5 Real-Time Clock family provides a groundbreaking combination of ultra-low power coupled with a highly sophisticated feature set. With power requirements significantly lower than any other industry RTC (as low as 14 nA), these are the first semiconductors based on innovative SPOT™ (Subthreshold Power Optimized Technology) CMOS platform. The AB08X5 includes on-chip oscillators to provide minimum power consumption, full RTC functions including battery backup and programmable counters and alarms for timer and watchdog functions, and either an I<sup>2</sup>C or SPI serial interface for communication with a host controller.

**Disclaimer:** AB08X5 series of devices are based on innovative SPOT technology, proprietary to Ambiq Micro.




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## Typical Application Circuit






\* Total battery series impedance = 1.5k ohms, which may require an external resistor

Note: Recommended tuning fork crystal is ABS07-120-32.768kHz-T.




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## 1. Family Summary

The AB08X5 family consists of several members (see Table 1). All devices are supplied in a standard 3x3 mm QFN-16 package. Members of the software and pin compatible AB18X5 RTC family are also listed.

**Table 1: Family Summary**

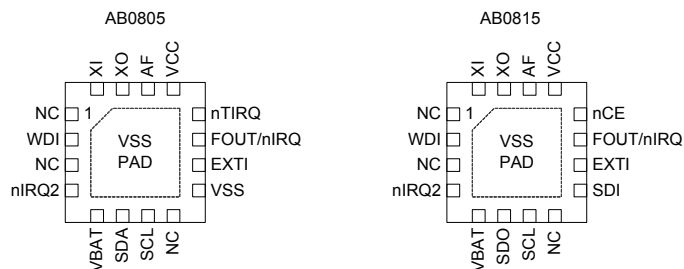
Part #	Baseline Timekeeping		Advanced Timekeeping				Power Management				Interface
	XT Osc	Number of GP Outputs	RC Osc	Calib/ Auto-calib	Watch-dog	RAM (B)	VBAT Switch	Reset Mgmt	Ext Int	Power Switch and Sleep FSM	
AB0805	■	3	■	■	■	256	■		■		I <sup>2</sup> C
AB0815	■	2	■	■	■	256	■		■		SPI
<b>Software and Pin Compatible AB18X5 Family Components</b>											
AB1805	■	4	■	■	■	256	■	■	■	■	I <sup>2</sup> C
AB1815	■	3	■	■	■	256	■	■	■	■	SPI

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## 2. Package Pins

### 2.1 Pin Configuration and Connections




Figure 1 and Table 2 show the QFN-16 pin configurations for the AB08X5 parts. Pins labeled NC must be left unconnected. The thermal pad, pin 17, on the QFN-16 packages must be connected to VSS.



**Figure 1. Pin Configuration Diagram**

**Table 2: Pin Connections**

Pin Name	Pin Type	Function	Pin Number	
			AB0805	AB0815
VSS	Power	Ground	9,17	17
VCC	Power	System power supply	13	13
XI	XT	Crystal input	16	16
XO	XT	Crystal output	15	15
AF	Output	Autocalibration filter	14	14
VBAT	Power	Battery power supply	5	5
SCL	Input	I <sup>2</sup> C or SPI interface clock	7	7
SDO	Output	SPI data output		6
SDI	Input	SPI data input		9
nCE	Input	SPI chip select		12
SDA	Input	I <sup>2</sup> C data input/output	6	
EXTI	Input	External interrupt input	10	10
WDI	Input	Watchdog reset input	2	2
FOUT/nIRQ	Output	Int 1/function output	11	11
nIRQ2	Output	Int 2 output	4	4
nTIRQ	Output	Timer interrupt output	12	




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## 2.2 Pin Descriptions

Table 3 provides a description of the pin connections.




**Table 3: Pin Descriptions**

<b>Pin Name</b>	<b>Description</b>
VSS	Ground connection. In the QFN-16 packages the ground slug on the bottom of the package must be connected to VSS.
VCC	Primary power connection. If a single power supply is used, it must be connected to VCC.
VBAT	Battery backup power connection. If a backup battery is not present, VBAT must be connected directly to VSS, but it may also be used to provide the analog input to the internal comparator (see Analog-Comparator).
XI	Crystal oscillator input connection.
XO	Crystal oscillator output connection.
AF	Autocalibration filter connection. A 47pF ceramic capacitor must be placed between this pin and VSS for improved Autocalibration mode timing accuracy.
SCL	I/O interface clock connection. It provides the SCL input in both I <sup>2</sup> C and SPI interface parts. A pull-up resistor is required on this pin.
SDA (only available in I <sup>2</sup> C environments)	I/O interface I <sup>2</sup> C data connection. A pull-up resistor is required on this pin.
SDO (only available in SPI environments)	I/O interface SPI data output connection.
SDI	I/O interface SPI data input connection.
nCE (only available in SPI environments)	I/O interface SPI chip select input connection. It is an active low signal. A pull-up resistor is recommended to be connected to this pin to ensure it is not floating. A pull-up resistor also prevents inadvertent writes to the RTC during power transitions.
EXTI	External interrupt input connection. It may be used to generate an External 1 interrupt with polarity selected by the EX1P bit if enabled by the EX1E bit. The value of the EXTI pin may be read in the EXIN register bit. This pin does not have an internal pull-up or pull-down resistor and so one must be added externally. It must not be left floating or the RTC may consume higher current. Instead, it must be connected directly to either VCC or VSS if not used.
WDI	Watchdog Timer reset input connection. It may also be used to generate an External 2 interrupt with polarity selected by the EX2P bit if enabled by the EX2E bit. The value of the WDI pin may be read in the WDIN register bit. This pin does not have an internal pull-up or pull-down resistor and so one must be added externally. It must not be left floating or the RTC may consume higher current. Instead, it must be connected directly to either VCC or VSS if not used.

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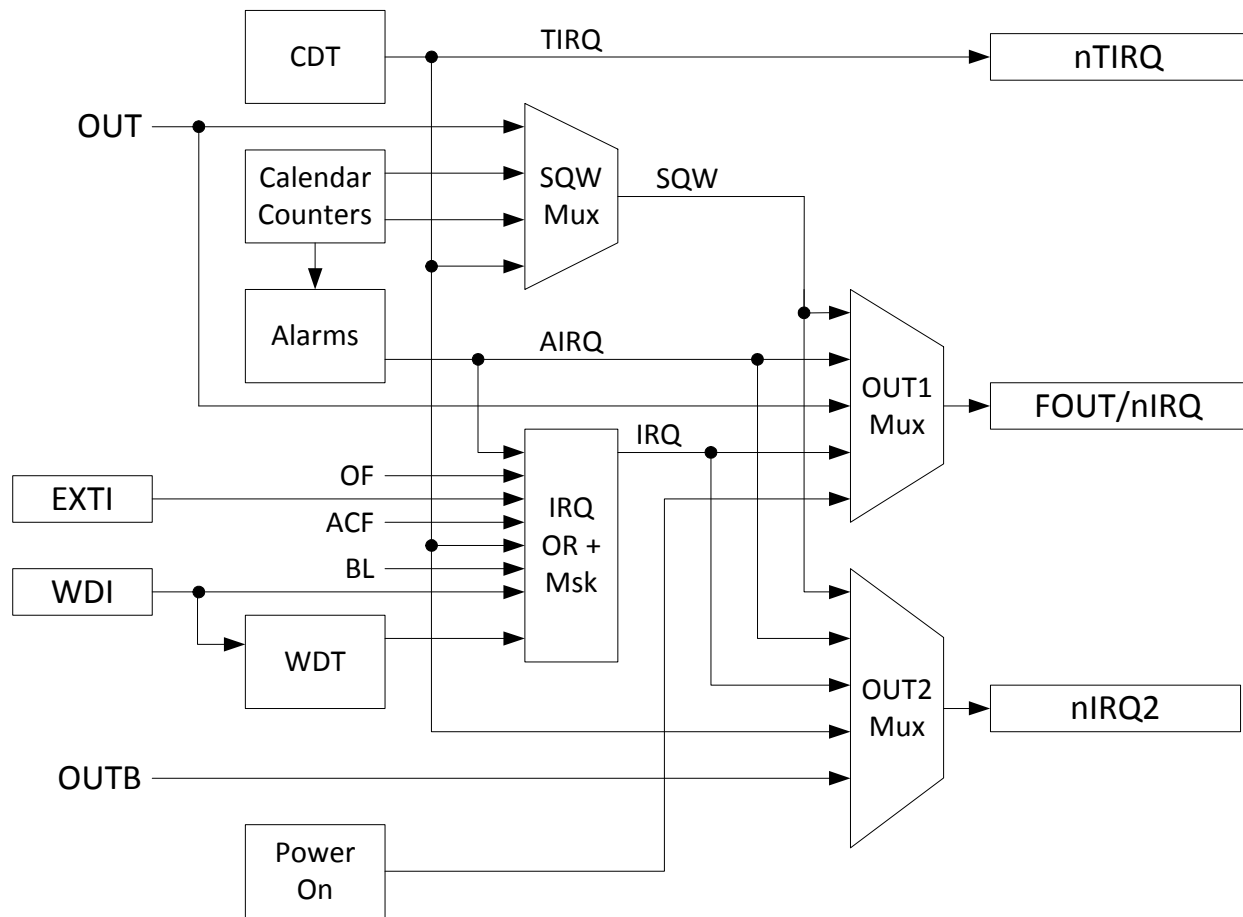
**Table 3: Pin Descriptions**

Pin Name	Description
FOUT/nIRQ	<p>Primary interrupt output connection. This pin is an open drain output. An external pull-up resistor must be added to this pin. It should be connected to the host device and is used to indicate when the RTC can be accessed via the serial interface. FOUT/nIRQ may be configured to generate several signals as a function of the OUT1S field(see 0x11 - Control2). FOUT/nIRQ is also asserted low on a power up until the AB08X5 has exited the reset state and is accessible via the I/O interface.</p> <ol style="list-style-type: none"> <li>1. FOUT/nIRQ can drive the value of the OUT bit.</li> <li>2. FOUT/nIRQ can drive the inverse of the combined interrupt signal IRQ (see Interrupts).</li> <li>3. FOUT/nIRQ can drive the square wave output (see 0x13 - SQW) if enabled by SQWE.</li> <li>4. FOUT/nIRQ can drive the inverse of the alarm interrupt signal AIRQ (see Interrupts).</li> </ol>
nIRQ2	<ol style="list-style-type: none"> <li>1. Secondary interrupt output connection. It is an open drain output. This pin can be left floating if not used. nIRQ2 may be configured to generate several signals as a function of the OUT2S field (see 0x11 - Control2). nIRQ2 can drive the value of the OUTB bit.</li> <li>2. nIRQ2 can drive the square wave output (see 0x13 - SQW) if enabled by SQWE.</li> <li>3. nIRQ2 can drive the inverse of the combined interrupt signal IRQ(see Interrupts).</li> <li>4. nIRQ2 can drive the inverse of the alarm interrupt signal AIRQ(see Interrupts).</li> <li>5. nIRQ2 can drive either sense of the timer interrupt signal TIRQ.</li> </ol>
nTIRQ (only available in I <sup>2</sup> C environments)	<p>Timer interrupt output connection. It is an open drain output. nTIRQ always drives the active low nTIRQ signal. If this pin is used, an external pull-up resistor must be added to this pin. If the pin is not used, it can be left floating.</p>

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### 3. Digital Architecture Summary

Figure 2 illustrates the overall architecture of the pin inputs and outputs of the AB08X5.



**Figure 2. Digital Architecture Summary**



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## 4. Electrical Specifications

### 4.1 Absolute Maximum Ratings

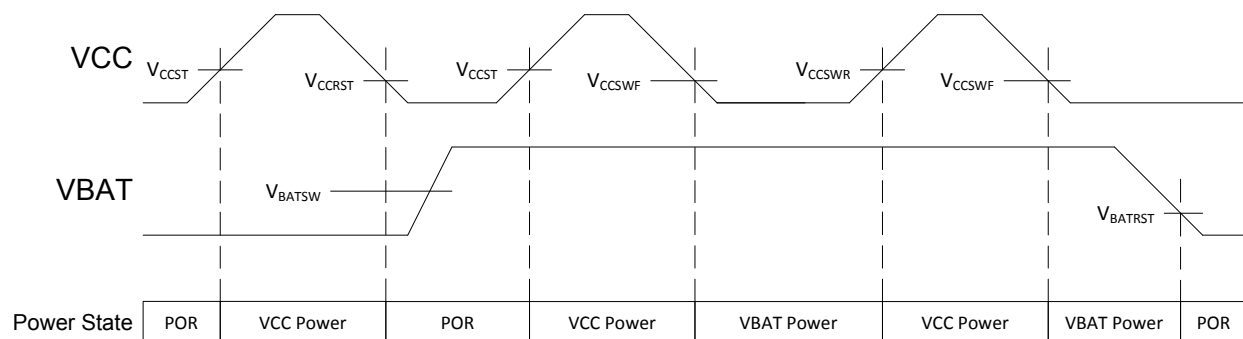
Table 4 lists the absolute maximum ratings.

**Table 4: Absolute Maximum Ratings**




SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	System Power Voltage		-0.3		3.8	V
V <sub>BAT</sub>	Battery Voltage		-0.3		3.8	V
V <sub>I</sub>	Input voltage	VCC Power state	-0.3		V <sub>CC</sub> + 0.3	V
V <sub>I</sub>	Input voltage	VBAT Power state	-0.3		V <sub>BAT</sub> + 0.3	V
V <sub>O</sub>	Output voltage	VCC Power state	-0.3		V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage	VBAT Power state	-0.3		V <sub>BAT</sub> + 0.3	V
I <sub>I</sub>	Input current		-10		10	mA
I <sub>O</sub>	Output current		-20		20	mA
V <sub>ESD</sub>	ESD Voltage	CDM			±500	V
		HBM			±4000	V
I <sub>LU</sub>	Latch-up Current				100	mA
T <sub>STG</sub>	Storage Temperature		-55		125	°C
T <sub>OP</sub>	Operating Temperature		-40		85	°C
T <sub>SLD</sub>	Lead temperature	Hand soldering for 10 seconds			300	°C
T <sub>REF</sub>	Reflow soldering temperature	Reflow profile per JEDEC J-STD-020D.1			260	°C

### 4.2 Power Supply Parameters

Figure 3 and Table 5 describe the power supply and switchover parameters. See Power Control and Switching for a detailed description of the operations.



**Figure 3. Power Supply Switchover**

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For Table 5,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ , TYP values at  $25\text{ }^{\circ}\text{C}$ .

**Table 5: Power Supply and Switchover Parameters**

SYMBOL	PARAMETER	PWR	TYPE	POWER STATE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}$	System Power Voltage	VCC	Static	VCC Power	Clocks operating and RAM and registers retained	1.5		3.6	V
$V_{CCIO}$	VCC I/O Interface Voltage	VCC	Static	VCC Power	I <sup>2</sup> C or SPI operation	1.5		3.6	V
$V_{CCST}$	VCC Start-up Voltage <sup>(1)</sup>	VCC	Rising	POR -> VCC Power		1.6			V
$V_{CCRST}$	VCC Reset Voltage	VCC	Falling	VCC Power -> POR	$V_{BAT} < V_{BAT,MIN}$ or no $V_{BAT}$		1.3	1.5	V
$V_{CCSWR}$	VCC Rising Switch-over Threshold Voltage	VCC	Rising	VBAT Power -> VCC Power	$V_{BAT} \geq V_{BATRST}$		1.6	1.7	V
$V_{CCSWF}$	VCC Falling Switch-over Threshold Voltage	VCC	Falling	VCC Power -> VBAT Power	$V_{BAT} \geq V_{BATSW,MIN}$	1.2	1.5		V
$V_{CCSWH}$	VCC Switchover Threshold Hysteresis <sup>(2)</sup>	VCC	Hyst.	VCC Power <-> VBAT Power			70		mV
$V_{CCFS}$	VCC Falling Slew Rate to switch to VBAT state <sup>(4)</sup>	VCC	Falling	VCC Power -> VBAT Power	$V_{CC} < V_{CCSW,MAX}$	0.7	1.4		V/ms
$V_{BAT}$	Battery Voltage	VBAT	Static	VBAT Power	Clocks operating and RAM and registers retained	1.4		3.6	V
$V_{BATSW}$	Battery Switchover Voltage Range <sup>(5)</sup>	VBAT	Static	VCC Power -> VBAT Power		1.6		3.6	V
$V_{BATRST}$	Falling Battery POR Voltage <sup>(7)</sup>	VBAT	Falling	VBAT Power -> POR	$V_{CC} < V_{CCSWF}$		1.1	1.4	V
$V_{BMRG}$	$V_{BAT}$ Margin above $V_{CC}$ <sup>(3)</sup>	VBAT	Static	$V_{BAT}$ Power		200			mV
$V_{BATESR}$	$V_{BAT}$ supply series resistance <sup>(6)</sup>	VBAT	Static	$V_{BAT}$ Power		1.0	1.5		k $\Omega$

<sup>(1)</sup>  $V_{CC}$  must be above  $V_{CCST}$  to exit the POR state, independent of the  $V_{BAT}$  voltage.

<sup>(2)</sup> Difference between  $V_{CCSWR}$  and  $V_{CCSWF}$ .




<sup>(3)</sup>  $V_{BAT}$  must be higher than  $V_{CC}$  by at least this voltage to ensure the AB08X5 remains in the VBAT Power state.

<sup>(4)</sup> Maximum VCC falling slew rate to guarantee correct switchover to VBAT Power state. There is no VCC falling slew rate requirement if switching to the VBAT power source is not required.

<sup>(5)</sup>  $V_{BAT}$  voltage to guarantee correct transition to VBAT Power state when  $V_{CC}$  falls.

<sup>(6)</sup> Total series resistance of the power source attached to the VBAT pin. The optimal value is 1.5k $\Omega$ , which may require an external resistor. VBAT power source ESR + external resistor value = 1.5k $\Omega$ .

<sup>(7)</sup>  $V_{BATRST}$  is also the static voltage required on  $V_{BAT}$  for register data retention.

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### 4.3 Operating Parameters




Table 6 lists the operating parameters.



For Table 6,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ , TYP values at  $25\text{ }^{\circ}\text{C}$ .

**Table 6: Operating Parameters**

SYMBOL	PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{T+}$	Positive-going Input Threshold Voltage		3.0V		1.5	2.0	V
			1.8V		1.1	1.25	
$V_{T-}$	Negative-going Input Threshold Voltage		3.0V	0.8	0.9		V
			1.8V	0.5	0.6		
$I_{LEAK}$	Input leakage current		3.0V		0.02	80	nA
$C_I$	Input capacitance				3		pF
$V_{OH}$	High level output voltage on push-pull outputs		1.7V – 3.6V	$0.8 \cdot V_{CC}$			V
$V_{OL}$	Low level output voltage		1.7V – 3.6V			$0.2 \cdot V_{CC}$	V
$I_{OH}$	High level output current on push-pull outputs	$V_{OH} = 0.8 \cdot V_{CC}$	1.7V	-2	-3.8		mA
			1.8V	-3	-4.3		
			3.0V	-7	-11		
			3.6V	-8.8	-15		
$I_{OL}$	Low level output current	$V_{OL} = 0.2 \cdot V_{CC}$	1.7V	3.3	5.9		mA
			1.8V	6.1	6.9		
			3.0V	17	19		
			3.6V	18	20		
$I_{OLEAK}$	Output leakage current		1.7V – 3.6V		0.02	80	nA

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#### 4.4 Oscillator Parameters

Table 7 lists the oscillator parameters.



For Table 7,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$  unless otherwise indicated.  
 $V_{CC} = 1.7$  to  $3.6\text{V}$ , TYP values at  $25\text{ }^{\circ}\text{C}$  and  $3.0\text{V}$ .

**Table 7: Oscillator Parameters**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$F_{XT}$	XI and XO pin Crystal Frequency			32.768		kHz
$F_{OF}$	XT Oscillator failure detection frequency			8		kHz
$C_{INX}$	Internal XI and XO pin capacitance			1		pF
$C_{EX}$	External XI and XO pin PCB capacitance			1		pF
$OA_{XT}$	XT Oscillation Allowance	At $25^{\circ}\text{C}$ using a 32.768 kHz crystal	270	320		k $\Omega$
$F_{RCC}$	Calibrated RC Oscillator Frequency <sup>(1)</sup>	Factory Calibrated at $25^{\circ}\text{C}$ , $V_{CC} = 2.8\text{V}$		128		Hz
$F_{RCU}$	Uncalibrated RC Oscillator Frequency	Calibration Disabled (OFF-SETR = 0)	89	122	220	Hz
$J_{RCCC}$	RC Oscillator cycle-to-cycle jitter	Calibration Disabled (OFF-SETR = 0) – 128 Hz		2000		ppm
		Calibration Disabled (OFF-SETR = 0) – 1 Hz		500		
$A_{XT}$	XT mode digital calibration accuracy <sup>(1)</sup>	Calibrated at an initial temperature and voltage	-2		2	ppm
$A_{AC}$	Autocalibration mode timing accuracy, 512 second period, $T_A = -10^{\circ}\text{C}$ to $60^{\circ}\text{C}$ <sup>(1)</sup>	24 hour run time		35		ppm
		1 week run time		20		
		1 month run time		10		
		1 year run time		3		
$T_{AC}$	Autocalibration mode operating temperature <sup>(2)</sup>		-10		60	$^{\circ}\text{C}$

<sup>(1)</sup> Timing accuracy is specified at  $25^{\circ}\text{C}$  after digital calibration of the internal RC oscillator and 32.768 kHz crystal. A typical 32.768 kHz tuning fork crystal has a negative temperature coefficient with a parabolic frequency deviation, which due to the crystal alone can result in a change of up to 150 ppm across the entire operating temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  in XT mode. Autocalibration mode timing accuracy is specified relative to XT mode timing accuracy from  $-10^{\circ}\text{C}$  to  $60^{\circ}\text{C}$ .

<sup>(2)</sup> Outside of this temperature range, the RC oscillator frequency change due to temperature may be outside of the allowable RC digital calibration range ( $\pm 12\%$ ) for autocalibration mode. If this happens, an autocalibration failure will occur and the ACF interrupt flag is set. The AB08X5 should be switched to use the XT oscillator as its clock source. Please see the Autocalibration Fail section for more details.




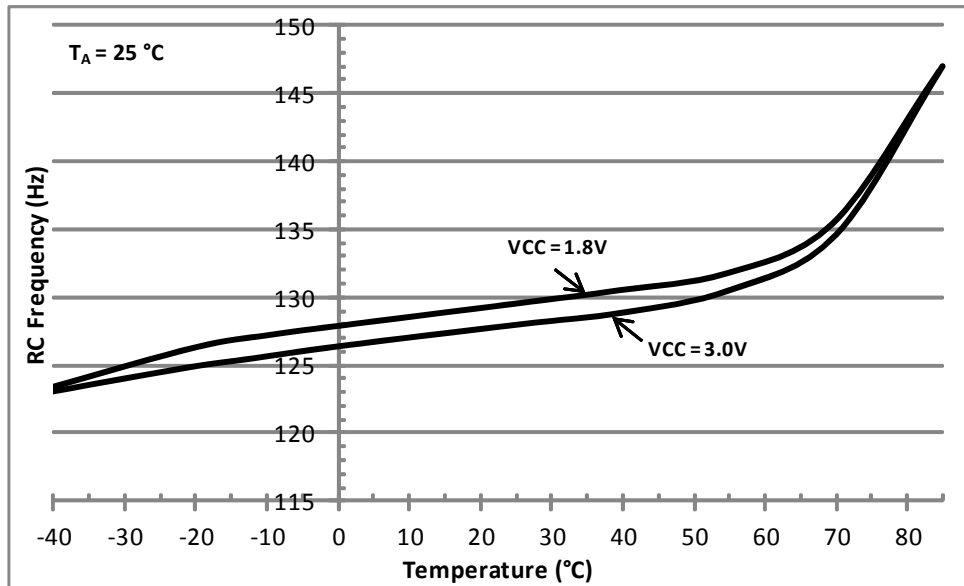
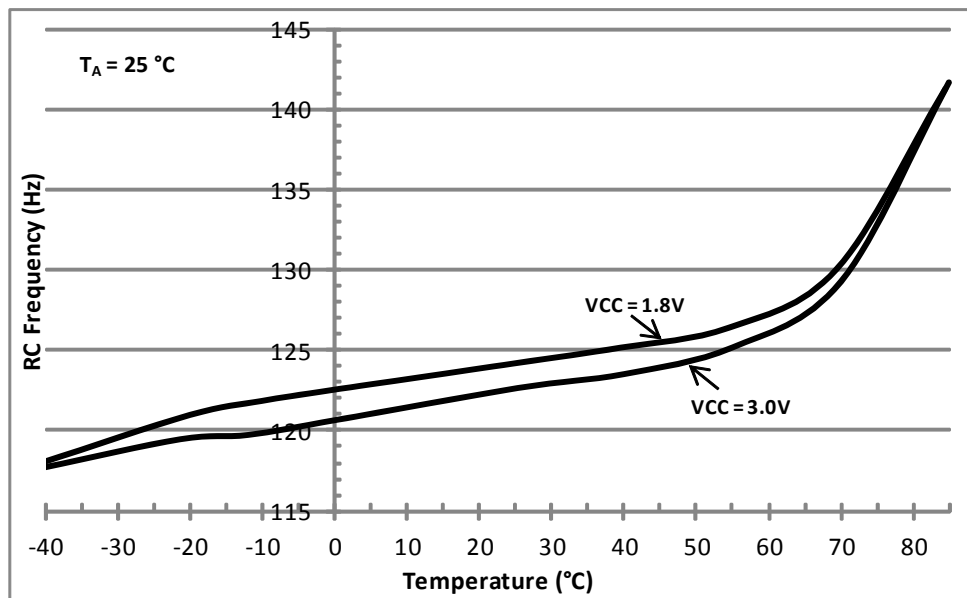
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Figure 4 shows the typical calibrated RC oscillator frequency variation vs. temperature. RC oscillator calibrated at 2.8V, 25°C.






**Figure 4. Calibrated RC Oscillator Typical Frequency Variation vs. Temperature**

Figure 5 shows the typical uncalibrated RC oscillator frequency variation vs. temperature.



**Figure 5. Uncalibrated RC Oscillator Typical Frequency Variation vs. Temperature**

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## 4.5 V<sub>CC</sub> Supply Current

Table 8 lists the current supplied into the VCC power input under various conditions.



For Table 8, T<sub>A</sub> = -40 °C to 85 °C, V<sub>BAT</sub> = 0 V to 3.6 V  
TYP values at 25 °C, MAX values at 85 °C, VCC Power state

**Table 8: V<sub>CC</sub> Supply Current**

SYMBOL	PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
I <sub>VCC:I2C</sub>	V <sub>CC</sub> supply current during I <sup>2</sup> C burst read/write	400kHz bus speed, 2.2k pull-up resistors on SCL/SDA <sup>(1)</sup>	3.0V		6	10	μA
			1.8V		1.5	3	
I <sub>VCC:SPIW</sub>	V <sub>CC</sub> supply current during SPI burst write	2 MHz bus speed <sup>(2)</sup>	3.0V		8	12	μA
			1.8V		4	6	
I <sub>VCC:SPIR</sub>	V <sub>CC</sub> supply current during SPI burst read	2 MHz bus speed <sup>(2)</sup>	3.0V		23	37	μA
			1.8V		13	21	
I <sub>VCC:XT</sub>	V <sub>CC</sub> supply current in XT oscillator mode	Time keeping mode with XT oscillator running <sup>(3)</sup>	3.0V		55	330	nA
			1.8V		51	290	
I <sub>VCC:RC</sub>	V <sub>CC</sub> supply current in RC oscillator mode	Time keeping mode with only the RC oscillator running (XT oscillator is off) <sup>(3)</sup>	3.0V		14	220	nA
			1.8V		11	170	
I <sub>VCC:ACAL</sub>	Average V <sub>CC</sub> supply current in Autocalibrated RC oscillator mode	Time keeping mode with only RC oscillator running and Auto-calibration enabled. ACP = 512 seconds <sup>(3)</sup>	3.0V		22	235	nA
			1.8V		18	190	

<sup>(1)</sup> Excluding external peripherals and pull-up resistor current. All other inputs (besides SDA and SCL) are at 0V or V<sub>CC</sub>. AB0805 only. Test conditions: Continuous burst read/write, 0x55 data pattern, 25 μs between each data byte, 20 pF load on each bus pin.

<sup>(2)</sup> Excluding external peripheral current. All other inputs (besides SDI, nCE and SCL) are at 0V or V<sub>CC</sub>. AB0815 only. Test conditions: Continuous burst write, 0x55 data pattern, 25 μs between each data byte, 20 pF load on each bus pin.

<sup>(3)</sup> All inputs and outputs are at 0 V or V<sub>CC</sub>




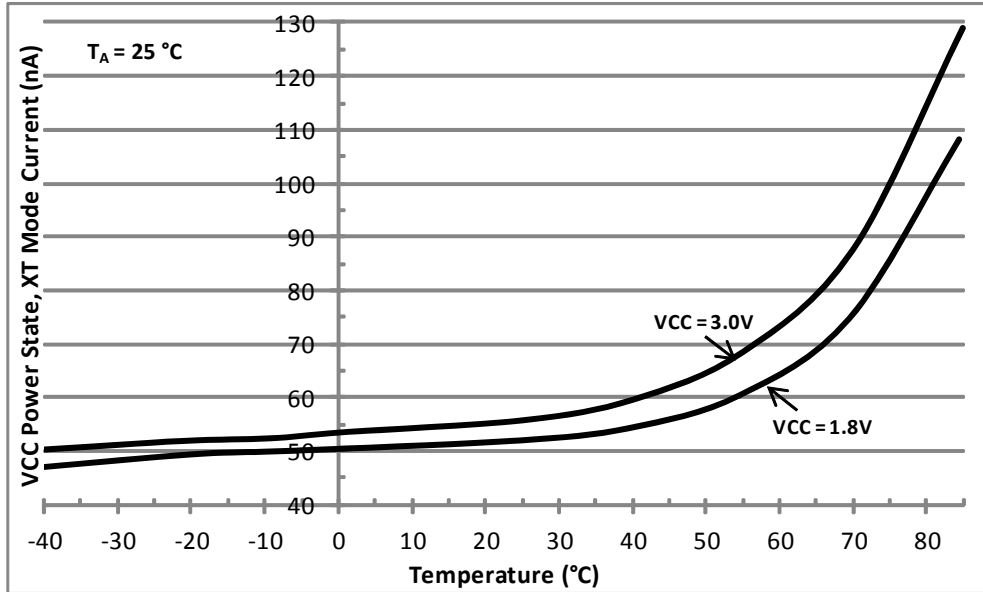
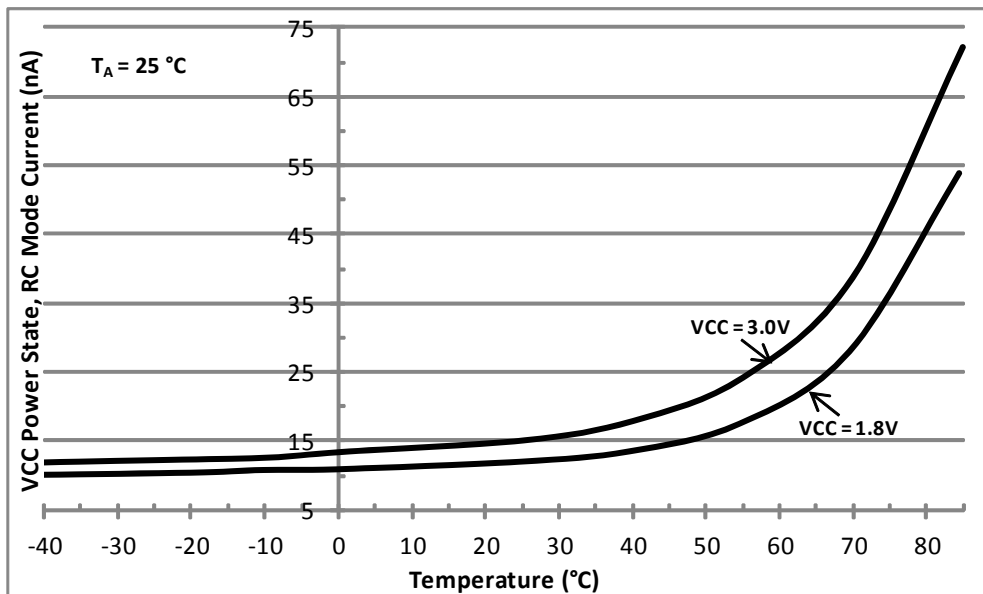
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Figure 6 shows the typical VCC power state operating current vs. temperature in XT mode.



**Figure 6. Typical VCC Current vs. Temperature in XT Mode**

Figure 7 shows the typical VCC power state operating current vs. temperature in RC mode.



**Figure 7. Typical VCC Current vs. Temperature in RC Mode**




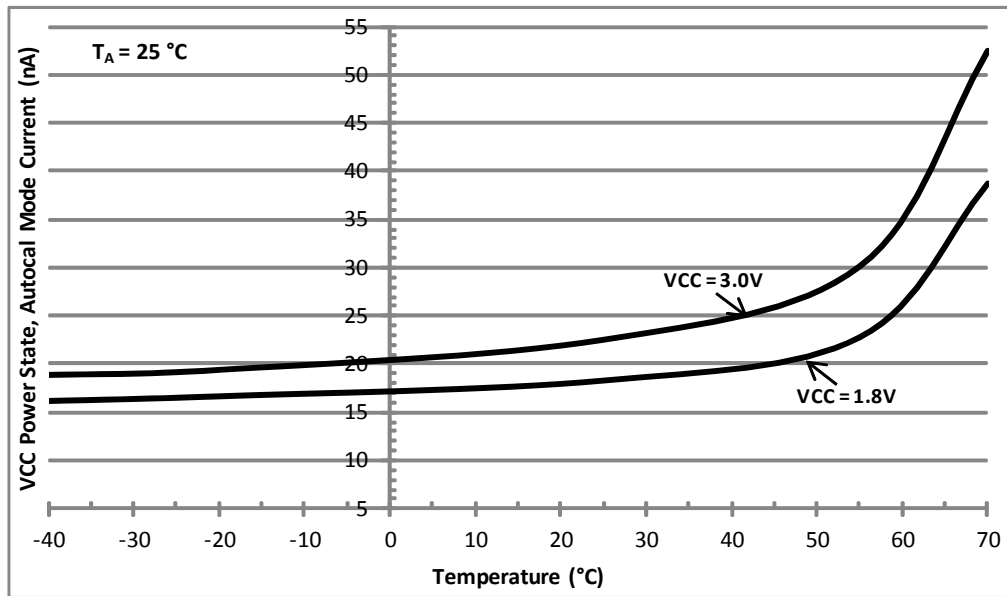
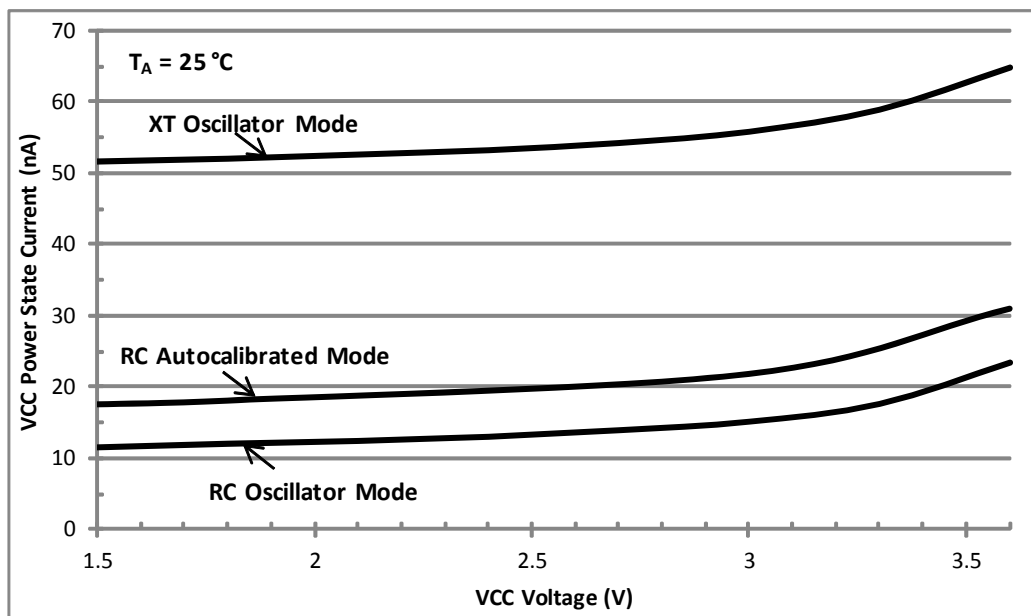
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Figure 8 shows the typical VCC power state operating current vs. temperature in RC Autocalibration mode.



**Figure 8. Typical VCC Current vs. Temperature in RC Autocalibration Mode**

Figure 9 shows the typical VCC power state operating current vs. voltage for XT Oscillator and RC Oscillator modes and the average current in RC Autocalibrated mode.



**Figure 9. Typical VCC Current vs. Voltage, Different Modes of Operation**






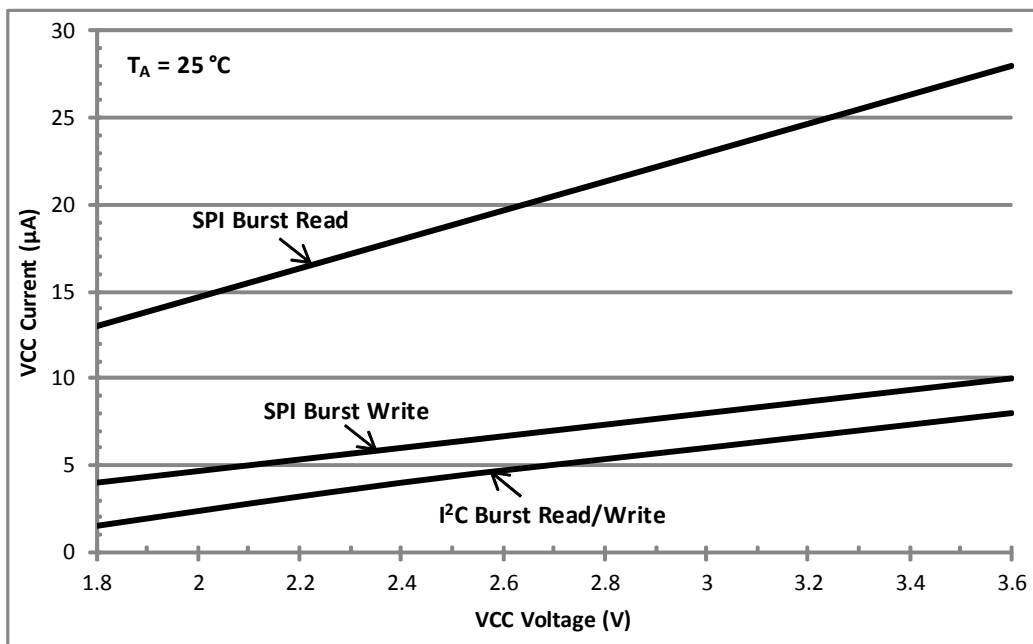



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Figure 10 shows the typical VCC power state operating current during continuous I<sup>2</sup>C and SPI burst read and write activity. Test conditions: T<sub>A</sub> = 25 °C, 0x55 data pattern, 25 μs between each data byte, 20 pF load on each bus pin, pull-up resistor current not included.



**Figure 10. Typical VCC Current vs. Voltage, I<sup>2</sup>C and SPI Burst Read/Write**

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## 4.6 VBAT Supply Current

Table 9 lists the current supplied into the VBAT power input under various conditions.



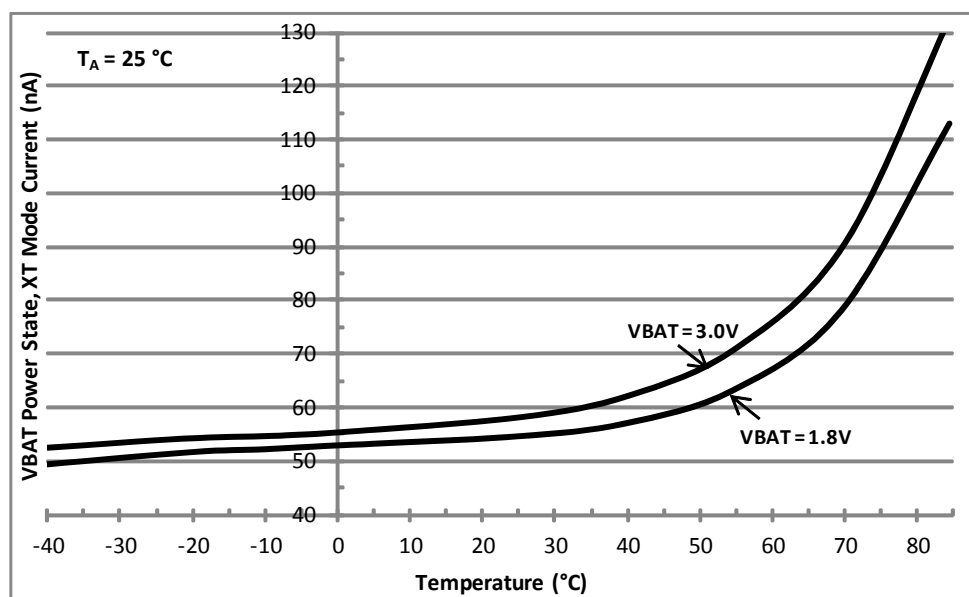
For Table 9,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ , TYP values at  $25\text{ }^{\circ}\text{C}$ , MAX values at  $85\text{ }^{\circ}\text{C}$ ,  $V_{BAT}$  Power state.

**Table 9:  $V_{BAT}$  Supply Current**

SYMBOL	PARAMETER	TEST CONDITIONS	$V_{CC}$	$V_{BAT}$	MIN	TYP	MAX	UNIT
$I_{VBAT:XT}$	VBAT supply current in XT oscillator mode	Time keeping mode with XT oscillator running <sup>(1)</sup>	$< V_{CCSWF}$	3.0V		56	330	nA
				1.8V		52	290	
$I_{VBAT:RC}$	VBAT supply current in RC oscillator mode	Time keeping mode with only the RC oscillator running (XT oscillator is off) <sup>(1)</sup>	$< V_{CCSWF}$	3.0V		16	220	nA
				1.8V		12	170	
$I_{VBAT:ACAL}$	Average VBAT supply current in Autocalibrated RC oscillator mode	Time keeping mode with the RC oscillator running. Autocalibration enabled. ACP = 512 seconds <sup>(1)</sup>	$< V_{CCSWF}$	3.0V		24	235	nA
				1.8V		20	190	
$I_{VBAT:VCC}$	VBAT supply current in VCC powered mode	$V_{CC}$ powered mode <sup>(1)</sup>	1.7 - 3.6 V	3.0V	-5	0.6	20	nA
				1.8V	-10	0.5	16	

<sup>(1)</sup> Test conditions: All inputs and outputs are at 0 V or  $V_{CC}$ .

Figure 11 shows the typical VBAT power state operating current vs. temperature in XT mode.



**Figure 11. Typical VBAT Current vs. Temperature in XT Mode**




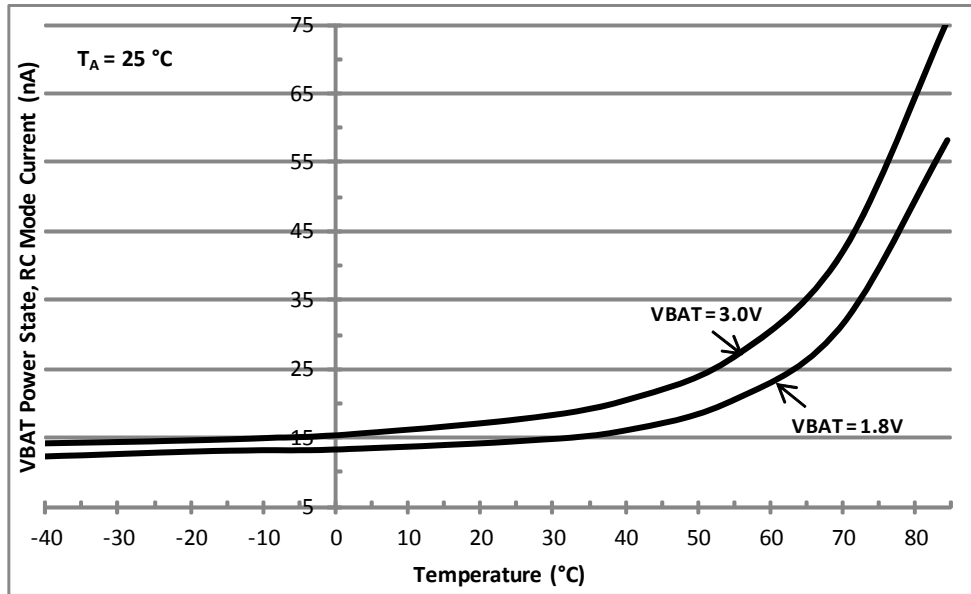
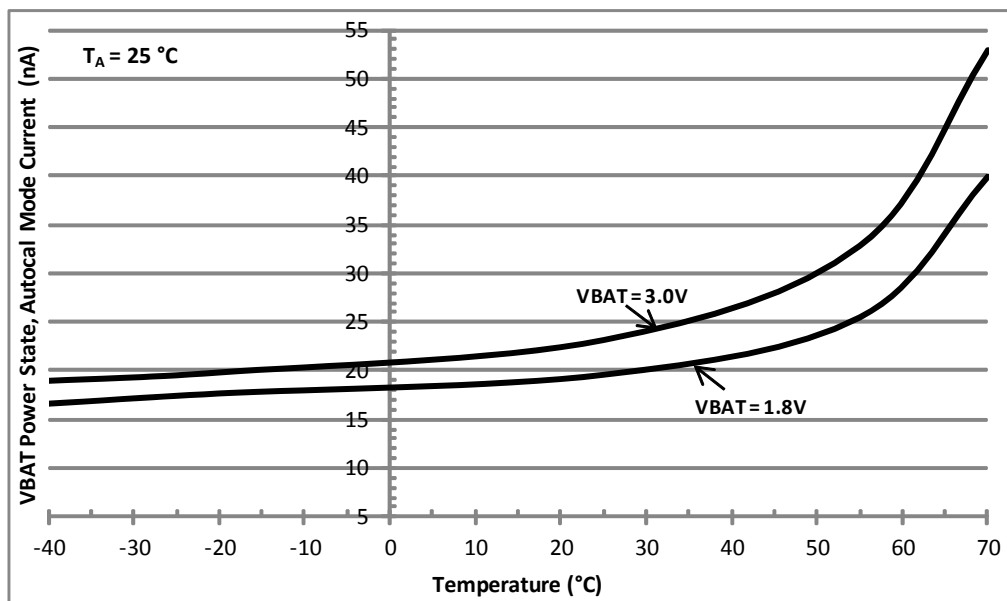
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Figure 12 shows the typical VBAT power state operating current vs. temperature in RC mode.



**Figure 12. Typical VBAT Current vs. Temperature in RC Mode**

Figure 13 shows the typical VBAT power state operating current vs. temperature in RC Autocalibration mode.



**Figure 13. Typical VBAT Current vs. Temperature in RC Autocalibration Mode**




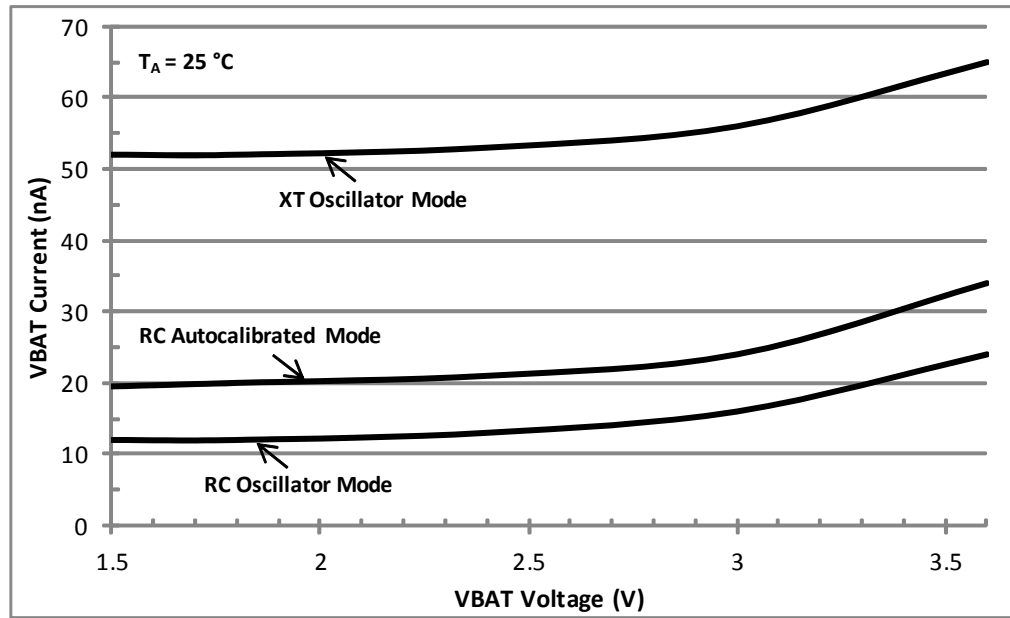
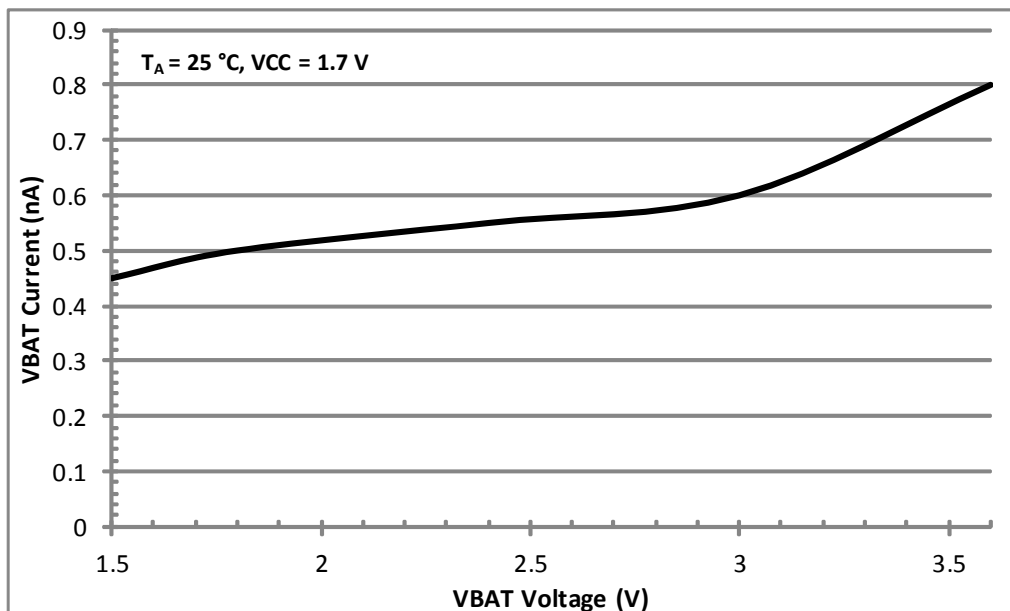
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Figure 14 shows the typical VBAT power state operating current vs. voltage for XT Oscillator and RC Oscillator modes and the average current in RC Autocalibrated mode, VCC = 0 V.






**Figure 14. Typical VBAT Current vs. Voltage, Different Modes of Operation**

Figure 15 shows the typical VBAT current when operating in the VCC power state, VCC = 1.7 V.



**Figure 15. Typical VBAT Current vs. Voltage in VCC Power State**

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## 4.7 BREF Electrical Characteristics




Table 10 lists the parameters of the VBAT voltage thresholds. BREF values other than those listed in the table are not supported.



For Table 10,  $T_A = -20\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ , TYP values at  $25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 1.7$  to  $3.6\text{V}$ .

**Table 10: BREF Parameters**

SYMBOL	PARAMETER	BREF	MIN	TYP	MAX	UNIT
$V_{BRF}$	VBAT falling threshold	0111	2.3	2.5	3.3	V
		1011	1.9	2.1	2.8	
		1101	1.6	1.8	2.5	
		1111		1.4		
$V_{BRR}$	VBAT rising threshold	0111	2.6	3.0	3.4	V
		1011	2.1	2.5	2.9	
		1101	1.9	2.2	2.7	
		1111		1.6		
$V_{BRH}$	VBAT threshold hysteresis	0111		0.5		V
		1011		0.4		
		1101		0.4		
		1111		0.2		
$T_{BR}$	VBAT analog comparator recommended operating temperature range	All values	-20		70	$^{\circ}\text{C}$

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## 4.8 I<sup>2</sup>C AC Electrical Characteristics

Figure 16 and Table 11 describe the I<sup>2</sup>C AC electrical parameters.

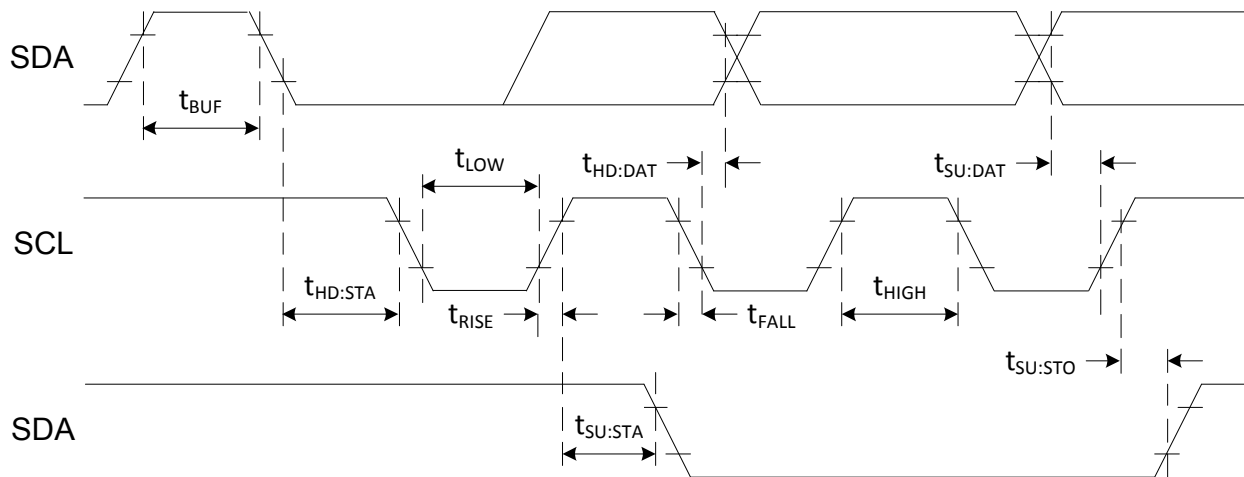





Figure 16. I<sup>2</sup>C AC Parameter Definitions



For Table 11,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ , TYP values at  $25\text{ }^{\circ}\text{C}$ .

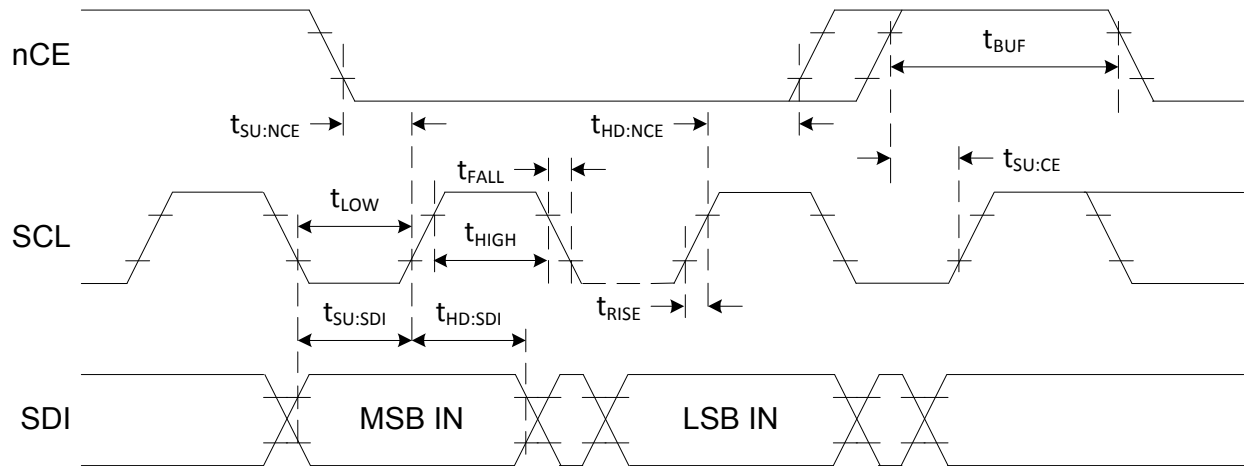
Table 11: I<sup>2</sup>C AC Electrical Parameters

SYMBOL	PARAMETER	VCC	MIN	TYP	MAX	UNIT
$f_{SCL}$	SCL input clock frequency	1.7V-3.6V	10		400	kHz
$t_{LOW}$	Low period of SCL clock	1.7V-3.6V	1.3			$\mu\text{s}$
$t_{HIGH}$	High period of SCL clock	1.7V-3.6V	600			ns
$t_{RISE}$	Rise time of SDA and SCL	1.7V-3.6V			300	ns
$t_{FALL}$	Fall time of SDA and SCL	1.7V-3.6V			300	ns
$t_{HD:STA}$	START condition hold time	1.7V-3.6V	600			ns
$t_{SU:STA}$	START condition setup time	1.7V-3.6V	600			ns
$t_{SU:DAT}$	SDA setup time	1.7V-3.6V	100			ns
$t_{HD:DAT}$	SDA hold time	1.7V-3.6V	0			ns
$t_{SU:STO}$	STOP condition setup time	1.7V-3.6V	600			ns
$t_{BUF}$	Bus free time before a new transmission	1.7V-3.6V	1.3			$\mu\text{s}$

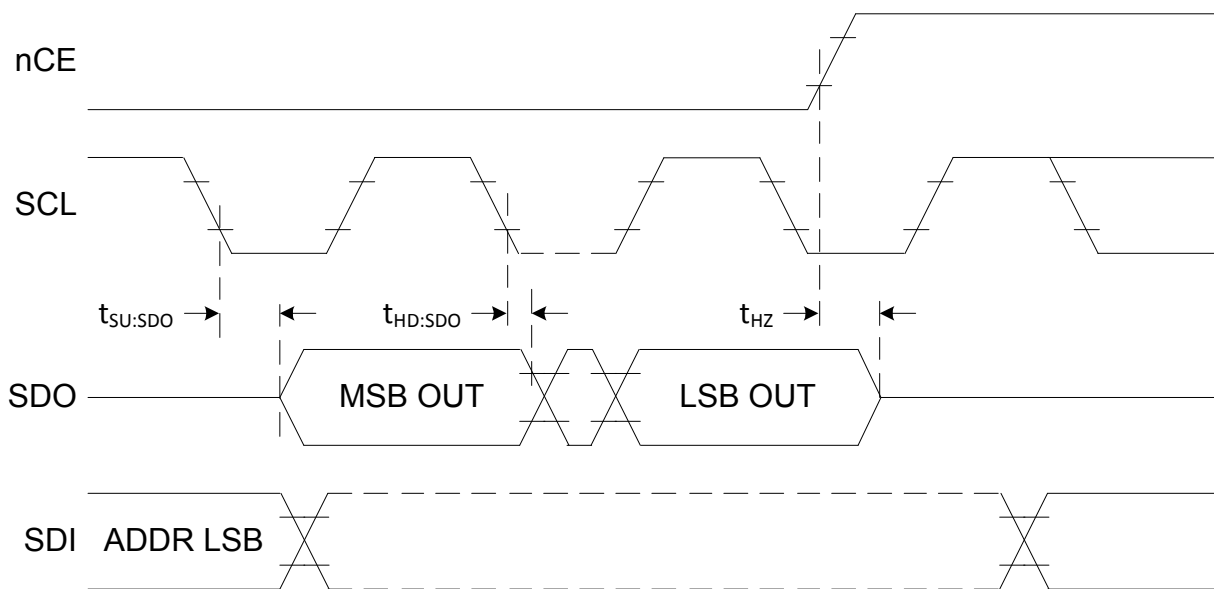
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## 4.9 SPI AC Electrical Characteristics

Figure 17, Figure 18, and Table 12 describe the SPI AC electrical parameters.






**Figure 17. SPI AC Parameter Definitions – Input**



**Figure 18. SPI AC Parameter Definitions – Output**






For Table 12,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ , TYP values at  $25\text{ }^{\circ}\text{C}$ .

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**Table 12: SPI AC Electrical Parameters**

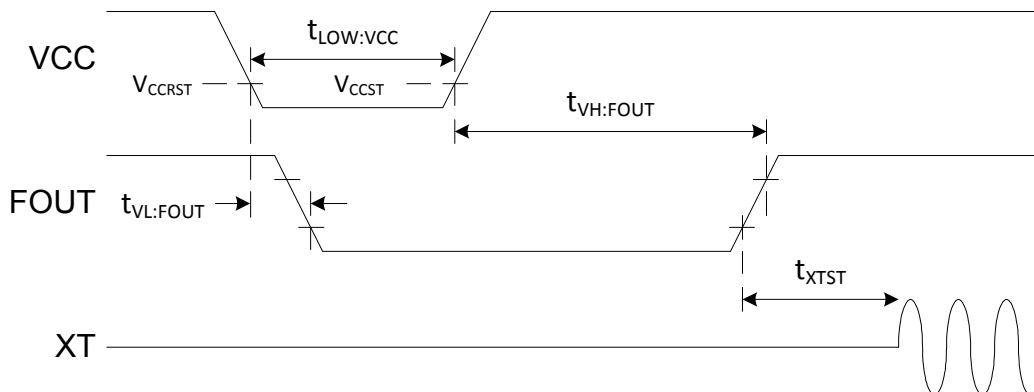
SYMBOL	PARAMETER	VCC	MIN	TYP	MAX	UNIT
f <sub>SCL</sub>	SCL input clock frequency	1.7V–3.6V	0.01		2	MHz
t <sub>LOW</sub>	Low period of SCL clock	1.7V–3.6V	200			ns
t <sub>HIGH</sub>	High period of SCL clock	1.7V–3.6V	200			ns
t <sub>RISE</sub>	Rise time of all signals	1.7V–3.6V			1	μs
t <sub>FALL</sub>	Fall time of all signals	1.7V–3.6V			1	μs
t <sub>SU:NCE</sub>	nCE low setup time to SCL	1.7V–3.6V	200			ns
t <sub>HD:NCE</sub>	nCE hold time to SCL	1.7V–3.6V	200			ns
t <sub>SU:CE</sub>	nCE high setup time to SCL	1.7V–3.6V	200			ns
t <sub>SU:SDI</sub>	SDI setup time	1.7V–3.6V	40			ns
t <sub>HD:SDI</sub>	SDI hold time	1.7V–3.6V	50			ns
t <sub>SU:SDO</sub>	SDO output delay from SCL	1.7V–3.6V			150	ns
t <sub>HD:SDO</sub>	SDO output hold from SCL	1.7V–3.6V	0			ns
t <sub>HZ</sub>	SDO output Hi-Z from nCE	1.7V–3.6V			250	ns
t <sub>BUF</sub>	nCE high time before a new transmission	1.7V–3.6V	200			ns




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#### 4.10 Power On AC Electrical Characteristics

Figure 19 and Table 13 describe the power on AC electrical characteristics for the FOUT pin and XT oscillator.






**Figure 19. Power On AC Electrical Characteristics**

	For Table 13, $T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ , $V_{BAT} < 1.2\text{ V}$
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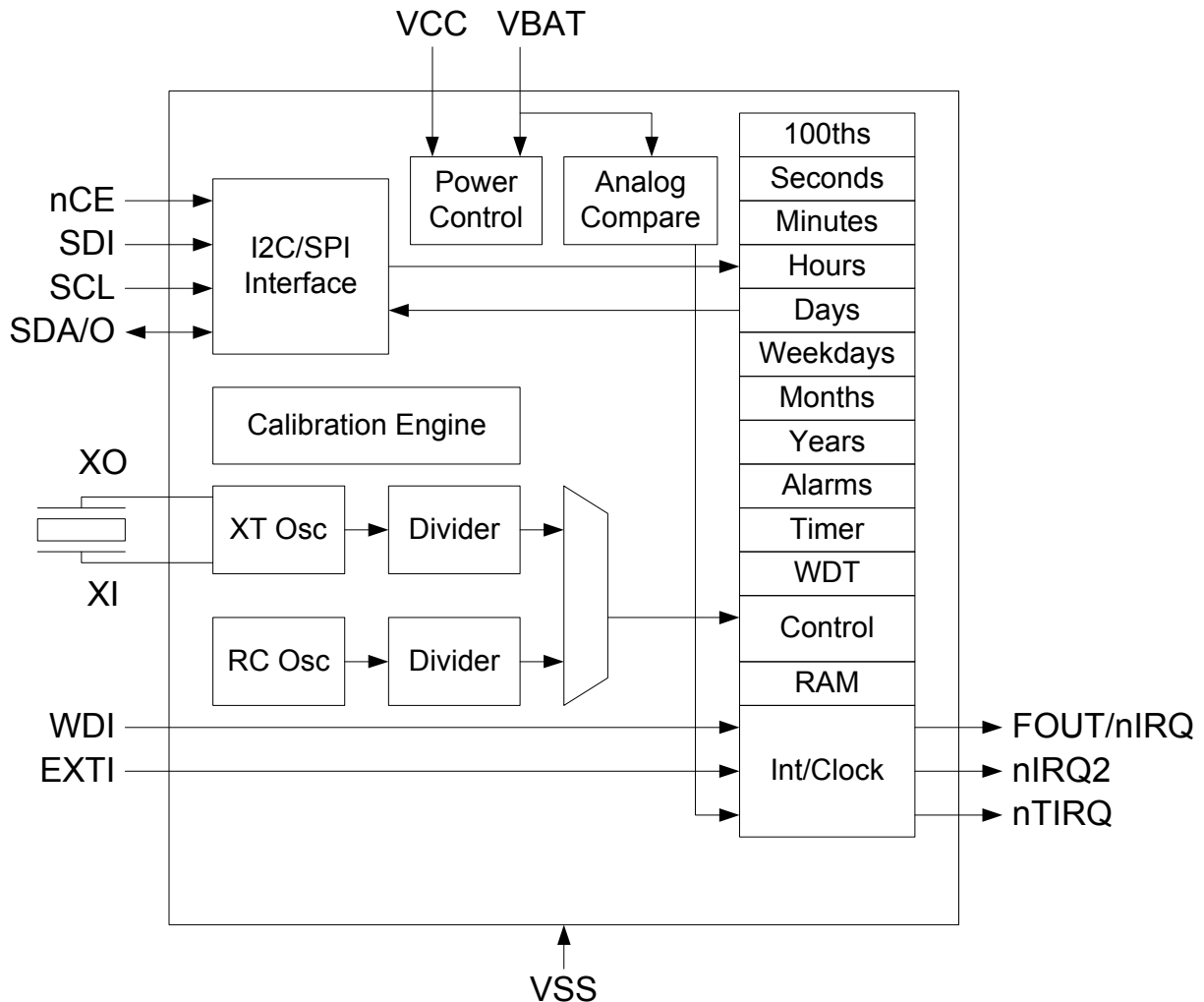
**Table 13: Power On AC Electrical Parameters**

SYMBOL	PARAMETER	VCC	$T_A$	MIN	TYP	MAX	UNIT
$t_{LOW:VCC}$	Low period of VCC to ensure a valid POR	1.7V–3.6V	85 °C		0.1		s
			25 °C		0.1		
			-20 °C		1.5		
			-40 °C		10		
$t_{VL:FOUT}$	VCC low to FOUT low	1.7V–3.6V	85 °C		0.1		s
			25 °C		0.1		
			-20 °C		1.5		
			-40 °C		10		
$t_{VH:FOUT}$	VCC high to FOUT high	1.7V–3.6V	85 °C		0.4		s
			25 °C		0.5		
			-20 °C		3		
			-40 °C		20		
$t_{XTST}$	FOUT high to XT oscillator start	1.7V–3.6V	85 °C		0.4		s
			25 °C		0.4		
			-20 °C		0.5		
			-40 °C		1.5		

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## 5. Functional Description

Figure 20 illustrates the AB08X5 functional design.






**Figure 20. Detailed Block Diagram**

The AB08X5 serves as a full function RTC for host processors such as microcontrollers. The AB08X5 includes 3 distinct feature groups: 1) baseline timekeeping features, 2) advanced timekeeping features, and 3) basic power management features. Functions from each feature group may be controlled via I/O offset mapped registers. These registers are accessed using either an I<sup>2</sup>C serial interface (e.g., in the AB0805) or a SPI serial interface (e.g., in the AB0815). Each feature group is described briefly below and in greater detail in subsequent sections.

The baseline timekeeping feature group supports the standard 32.786 kHz crystal (XT) oscillation mode for maximum frequency accuracy with an ultra-low current draw of 55 nA. The baseline timekeeping feature group also includes a standard set of counters monitoring hundredths of a second up through centuries. A complement of countdown timers and alarms may additionally be set to initiate interrupts or resets on several of the outputs.



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### 5.1.1 Bus Not Busy

Both SDA and SCL remain high.

### 5.1.2 Start Data Transfer

A change in the state of SDA from high to low, while SCL is high, defines the START condition. A START condition which occurs after a previous START but before a STOP is called a RESTART condition, and functions exactly like a normal STOP followed by a normal START.

### 5.1.3 Stop Data Transfer

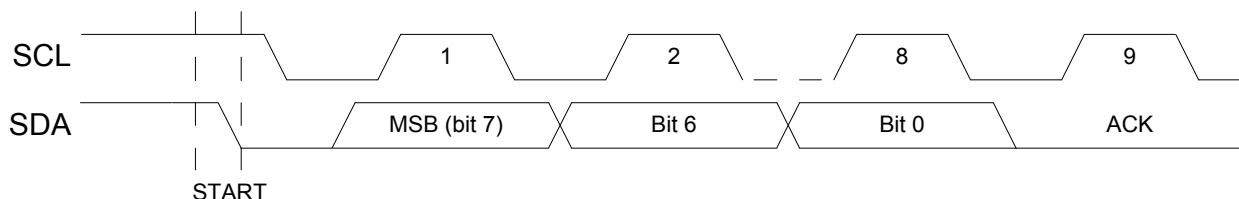
A change in the state of SDA from low to high, while SCL is high, defines the STOP condition.

### 5.1.4 Data Valid

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.




### 5.1.5 Acknowledge

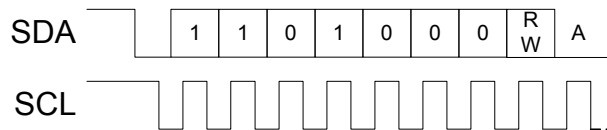
Each byte of eight bits is followed by one acknowledge (ACK) bit as shown in Figure 22. This acknowledge bit is a low level driven onto SDA by the receiver, whereas the master generates an extra acknowledge related SCL pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, on a read transfer a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related SCL pulse. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge (a NAK) on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.



**Figure 22. I<sup>2</sup>C Acknowledge Address Operation**

Figure 23 illustrates the operation with which the master addresses the AB08X5. After the START condition, a 7-bit address is transmitted MSB first. If this address is 0b1101001 (0xD2/3), the AB08X5 is selected, the eighth bit indicate a write (RW = 0) or a read (RW = 1) operation and the AB08X5 supplies the ACK. The AB08X5 ignores all other address values and does not respond with an ACK.

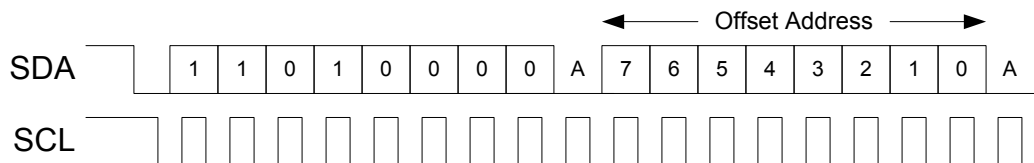
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**Figure 23. I<sup>2</sup>C Address Operation**

### 5.1.6 Offset Address Transmission

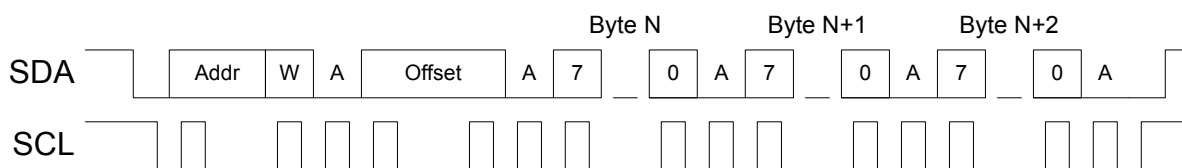
If the RW bit of the Address Operation indicates a write, the next byte transmitted from the master is the Offset Address as shown in Figure 24. This value is loaded into the Address Pointer of the AB08X5.



**Figure 24. I<sup>2</sup>C Offset Address Transmission**

### 5.1.7 Write Operation




In a write operation the master transmitter transmits to the AB08X5 slave receiver. The Address Operation has a RW value of 0, and the second byte contains the Offset Address as in Figure 24. The next byte is written to the register selected by the Address Pointer (which was loaded with the Offset Address) and the Address Pointer is incremented. Subsequent transfers write bytes into successive registers until a STOP condition is received, as shown in Figure 25.



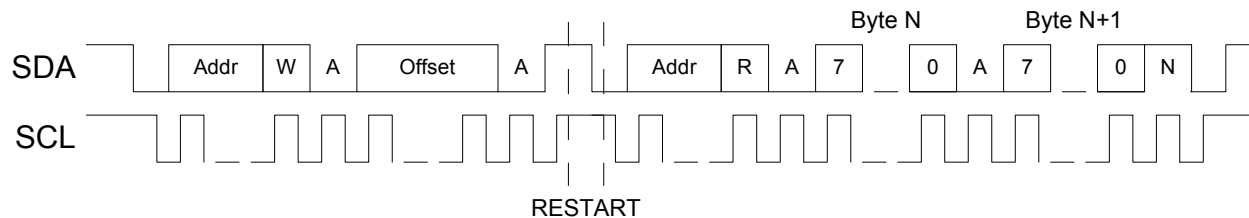
**Figure 25. I<sup>2</sup>C Write Operation**

### 5.1.8 Read Operation

In a read operation, the master first executes an Offset Address Transmission to load the Address Pointer with the desired Offset Address. A subsequent operation will again issue the address of the AB08X5 but with the RW bit as a 1 indicating a read operation. Figure 26 illustrates this transaction beginning with a RESTART condition, although a STOP followed by a START may also be used. After the address operation, the slave becomes the transmitter and sends the register value from the location pointed to by the Address Pointer, and the Address Pointer is incremented. Subsequent transactions produce successive register values, until the master receiver responds with a NAK and/or STOP or RESTART to

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complete the operation. Because the Address Pointer holds a valid register address, the master may initiate another read sequence at this point without performing another Offset Address operation.



**Figure 26. I<sup>2</sup>C Read Operation**

## 5.2 SPI Interface

The AB08X5 includes a standard 4-wire SPI interface. The serial peripheral interface (SPI) bus is intended for synchronous communication between different ICs. It typically consists of four signal lines: serial data input (SDI), serial data output (SDO), serial clock (SCL) and an active low chip enable (nCE).

The AB08X5 may be connected to a master with a 3-wire SPI interface by tying SDI and SDO together. By definition, a device that sends a message is called the “transmitter”, and the device that accepts the message is called the “receiver.” The device that controls the message transfer by driving SCL is called “master.” The devices that are controlled by the master are called “slaves”. The AB08X5 is always a slave device.




The nCE input is used to initiate and terminate a data transfer. The SCL input is used to synchronize data transfer between the master and the slave devices via the SDI (master to slave) and SDO (slave to master) lines. The SCL input, which is generated by the master, is active only during address and data transfer to any device on the SPI bus.

The AB08X5 supports clock frequencies up to 2 MHz, and responds to either (CPOL = 0, CPAH = 0 or CPOL = 1, CPAH = 1). For these two modes, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL. There is one clock for each bit transferred. Address and data bits are transferred in groups of eight bits. Some MCUs specify CPOL and CPAH in different ways, so care should be taken when configuring the SPI Master.

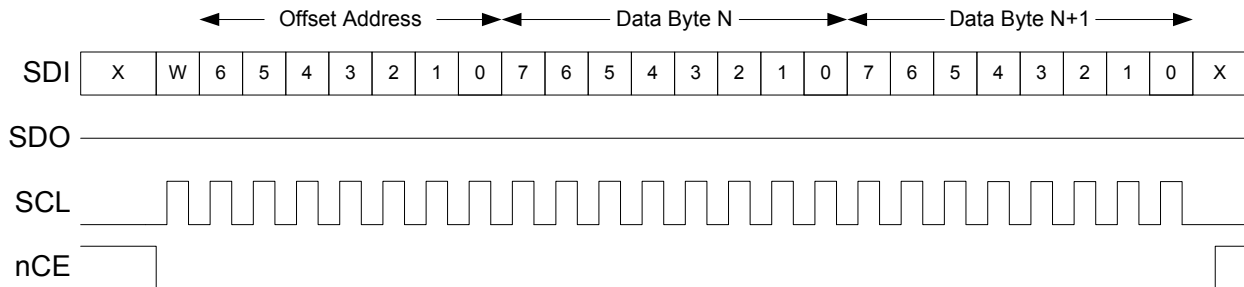
### 5.2.1 Write Operation

Figure 27 illustrates a SPI write operation. The operation is initiated when the nCE signal to the AB08X5 goes low. At that point an 8-bit Address byte is transmitted from the master on the SDI line, with the upper RW bit indicating read (if 0) or write (if 1). In this example the RW bit is a one selecting a write operation, and the lower 7 bits of the Address byte contain the Offset Address, which is loaded into the Address Pointer of the AB08X5.

Each subsequent byte is loaded into the register selected by the Address Pointer, and the Address Pointer is incremented. Because the address is only 7 bits long, only the lower 128 registers of the AB08X5 may be accessed via the SPI interface. The operation is terminated by the master by bringing the nCE signal

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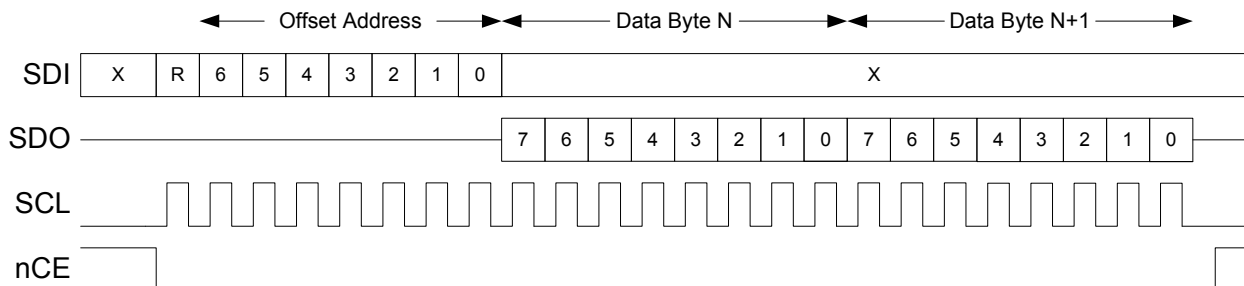
high. Note that the SDO line is not used in a write operation and is held in the high impedance state by the AB08X5.



**Figure 27. SPI Write Operation**

### 5.2.2 Read Operation

Figure 28 illustrates a read operation. The address is transferred from the master to the slave just as it is in a write operation, but in this case the RW bit is a 0 indicating a read. After the transfer of the last address bit, bit 0, the AB08X5 begins driving data from the register selected by the Address Pointer onto the SDO line, bit 7 first, and the Address Pointer is incremented. The transfer continues until the master brings the nCE line high.



**Figure 28. SPI Read Operation**

### 5.3 XT Oscillator

The AB08X5 includes a very power efficient crystal (XT) oscillator which runs at 32.786 kHz. This oscillator is selected by setting the OSEL bit to 0 and includes a low jitter calibration function.




### 5.4 RC Oscillator

The AB08X5 includes an extremely low power RC oscillator which runs at 128 Hz. This oscillator is selected by setting the OSEL bit to 1. Switching between the XT and RC Oscillators is guaranteed to produce less than one second of error in the Calendar Counters. The AB08X5 may be configured to automatically switch to the RC Oscillator when VCC drops below its threshold by setting the AOS bit, and/or be configured to automatically switch if an XT Oscillator failure is detected by setting the FOS bit.

### 5.5 RTC Counter Access

When reading any of the counters in the RTC using a burst operation, the 1 Hz and 100 Hz clocks are held off during the access. This guarantees that a single burst will either read or write a consistent timer value (other than the Hundredths Counter – see Hundredths Synchronization). There is a watchdog function to ensure that a very long pause on the interface does not cause the RTC to lose a clock.



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On a write to any of the Calendar Counters, the entire timing chain up to 100 Hz (if the XT Oscillator is selected) or up to 1Hz (if the RC Oscillator is selected) is reset to 0. This guarantees that the Counters will begin counting immediately after the write is complete, and that in the XT oscillator case the next 100 Hz clock will occur exactly 10 ms later. In the RC Oscillator case, the next 1 Hz clock will occur exactly 1 second later. This allows a burst write to configure all of the Counters and initiate a precise time start. Note that a Counter write may cause one cycle of a Square Wave output to be of an incorrect period.

The WRTC bit must be set in order to write to any of the Counter registers. This bit can be cleared to prevent inadvertent software access to the Counters.

## 5.6 Hundredths Synchronization

If the Hundredths Counter is read as part of the burst read from the counter registers, the following algorithm must be used to guarantee correct read information.

1. Read the Counters, using a burst read. If the Hundredths Counter is neither 00 nor 99, the read is correct.
2. If the Hundredths Counter was 00, perform the read again. The resulting value from this second read is guaranteed to be correct.
3. If the Hundredths Counter was 99, perform the read again.
  - A. If the Hundredths Counter is still 99, the results of the first read are guaranteed to be correct. Note that it is possible that the second read is not correct.
  - B. If the Hundredths Counter has rolled over to 00, and the Seconds Counter value from the second read is equal to the Seconds Counter value from the first read plus 1, both reads produced correct values. Alternatively, perform the read again. The resulting value from this third read is guaranteed to be correct.
  - C. If the Hundredths Counter has rolled over to 00, and the Seconds Counter value from the second read is equal to the Seconds Counter value from the first read, perform the read again. The resulting value from this third read is guaranteed to be correct.

## 5.7 Generating Hundredths of a Second

The generation of an exact 100 Hz signal for the Hundredths Counter requires a special logic circuit. The 2.048 kHz clock signal is divided by 21 for 12 iterations, and is alternately divided by 20 for 13 iterations. This produces an effective division of:

$$(21 * 12 + 20 * 13)/25 = 20.48$$

producing an exact long-term average 100 Hz output, with a maximum jitter of less than 1 ms. The Hundredths Counter is not available when the 128 Hz RC Oscillator is selected.




## 5.8 Watchdog Timer

The AB08X5 includes a Watchdog Timer (WDT), which can be configured to generate an interrupt or a reset if it times out. The WDT is controlled by the Watchdog Timer Register (see 0x1B - Watchdog Timer). The RB field selects the frequency at which the timer is decremented, and the BMB field determines the value loaded into the timer when it is restarted. If the timer reaches a value of zero, the WDS bit determines whether an interrupt is generated in nIRQ. The timer reaching zero sets the WDT flag in the Status Register, which may be cleared by setting the WDT flag to zero.

Two actions will restart the WDT timer:

1. Writing the Watchdog Timer Register with a new watchdog value.
2. A change in the level of the WDI pin.



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If the Watchdog Timer generates an interrupt or reset, the Watchdog Timer Register must be written in order to restart the Watchdog Timer function. If the BMB field is 0, the Watchdog Timer function is disabled.

The BMB field describes the maximum timeout delay. For example, if RB = 01 so that the clock period is 250 ms, a BMB value of 9 implies that the timeout will occur between 2000 ms and 2250 ms after writing the Watchdog Timer Register.

## 5.9 Digital Calibration




### 5.9.1 XT Oscillator Digital Calibration

In order to improve the accuracy of the XT oscillator, a Distributed Digital Calibration function is included (see 0x14 - Calibration XT). This function uses a calibration value, OFFSETX, to adjust the clock period over a 16 second or 32 second calibration period. When the 32.786 kHz XT oscillator is selected, the clock at the 16.384 kHz level of the divider chain is modified on a selectable interval. Clock pulses are either added or subtracted to ensure accuracy of the counters. If the CMDX bit is a 0 (normal calibration), OFFSETX cycles of the 16.384 kHz clock are gated (negative calibration) or replaced by 32.786 kHz pulses (positive calibration) within every 32 second calibration period. In this mode, each step in OFFSETX modifies the clock frequency by 1.907 ppm, with a maximum adjustment of ~+120/-122 ppm. If the CMDX bit is 1 (coarse calibration), OFFSETX cycles of the 16.384 kHz clock are gated or replaced by the 32.786 kHz clock within every 16 second calibration period. In this mode, each step in OFFSETX modifies the clock frequency by 3.814 ppm, with a maximum adjustment of ~+240/-244 ppm. OFFSETX contains a two's complement value, so the possible steps are from -64 to +63. Note that unlike other implementations, Distributed Digital Calibration guarantees that the clock is precisely calibrated every 32 seconds with normal calibration and every 16 seconds when coarse calibration is selected.

In addition to the normal calibration, the AB08X5 also includes an Extended Calibration field to compensate for low capacitance environments. The frequency generated by the Crystal Oscillator may be slowed by 122 ppm times the value in the XTCAL (see 0x1D – Oscillator Status Register) field (0, -122, -244 or -366 ppm). The clock is still precisely calibrated in 16 or 32 seconds. The pulses which are added to or subtracted from the 16.384 kHz clock are spread evenly over each 16 or 32 second period using the Ambiq Micro patented Distributed Calibration algorithm. This ensures that in XT mode the maximum cycle-to-cycle jitter in any clock of a frequency 16.384 kHz or lower caused by calibration will be no more than one 16.384 kHz period. This maximum jitter applies to all clocks in the AB08X5, including the Calendar Counter, Countdown Timer and Watchdog Timer clocks and any clock driven onto a clock output pin.

The XT oscillator calibration value is determined by the following process:

1. Set the OFFSETX, CMDX and XTCAL register fields to 0 to ensure calibration is not occurring.
2. Select the XT oscillator by setting the OSEL bit to 0.
3. Configure a 32768 Hz frequency square wave output on one of the output pins.
4. Precisely measure the exact frequency, Fmeas, at the output pin in Hz.
5. Compute the adjustment value required in ppm as  $((32768 - F_{meas}) * 1000000) / 32768 = P_{Adj}$
6. Compute the adjustment value in steps as  $P_{Adj} / (1000000 / 2^{19}) = P_{Adj} / (1.90735) = Adj$
7. If  $Adj < -320$ , the XT frequency is too high to be calibrated
8. Else if  $Adj < -256$ , set XTCAL = 3, CMDX = 1, OFFSETX =  $(Adj + 192) / 2$
9. Else if  $Adj < -192$ , set XTCAL = 3, CMDX = 0, OFFSETX =  $Adj + 192$
10. Else if  $Adj < -128$ , set XTCAL = 2, CMDX = 0, OFFSETX =  $Adj + 128$
11. Else if  $Adj < -64$ , set XTCAL = 1, CMDX = 0, OFFSETX =  $Adj + 64$
12. Else if  $Adj < 64$ , set XTCAL = 0, CMDX = 0, OFFSETX =  $Adj$
13. Else if  $Adj < 128$ , set XTCAL = 0, CMDX = 1, OFFSETX =  $Adj / 2$
14. Else the XT frequency is too low to be calibrated

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### 5.9.2 RC Oscillator Digital Calibration

The RC Oscillator has a patented Distributed Digital Calibration function similar to that of the XT Oscillator (see 0x14 - Calibration XT). However, because the RC Oscillator has a greater fundamental variability, the range of calibration is much larger, with four calibration ranges selected by the CMDR field. When the 128 Hz RC oscillator is selected, the clock at the 64 Hz level of the divider chain is modified on a selectable interval using the calibration value OFFSETR. Clock pulses are either added or subtracted to ensure accuracy of the counters. If the CMDR field is 00, OFFSETR cycles of the 64 Hz clock are gated (negative calibration) or replaced by 128 Hz pulses (positive calibration) within every 8,192 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 1.907 ppm, with a maximum adjustment of +15,623/-15,625 ppm (+/- 1.56%). If the CMDR field is 01, OFFSETR cycles of the 64 Hz clock are gated or replaced by the 128 Hz clock within every 4,096 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 3.82 ppm, with a maximum adjustment of +31,246/-31,250 ppm (+/-3.12%). If the CMDR field is 10, OFFSETR cycles of the 64 Hz clock are gated (negative calibration) or replaced by 128 Hz pulses (positive calibration) within every 2,048 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 7.64 ppm, with a maximum adjustment of +62,492/-62,500 ppm (+/- 6.25%). If the CMDR field is 11, OFFSETR cycles of the 64 Hz clock are gated or replaced by the 128 Hz clock within every 1,024 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 15.28 ppm, with a maximum adjustment of +124,984/-125,000 ppm (+/-12.5%). OFFSETR contains a two's complement value, so the possible steps are from -8,192 to +8,191.




The pulses which are added to or subtracted from the 64 Hz clock are spread evenly over each 8,192 second period using the Ambiq Micro patented Distributed Calibration algorithm. This ensures that in RC mode the maximum cycle-to-cycle jitter in any clock of a frequency 64 Hz or lower caused by calibration will be no more than one 64 Hz period. This maximum jitter applies to all clocks in the AB08X5 including the Calendar Counter, Countdown Timer and Watchdog Timer clocks and any clock driven onto a clock output pin.

The RC oscillator calibration value is determined by the following process:

1. Set the OFFSETR and CMDR register fields to 0 to ensure calibration is not occurring.
2. Select the RC oscillator by setting the OSEL bit to 1.
3. Configure a 128 Hz frequency square wave output on one of the output pins.
4. Precisely measure the exact frequency, Fmeas, at the output pin in Hz.
5. Compute the adjustment value required in ppm as  $((128 - F_{meas}) * 1000000) / F_{meas} = PAdj$
6. Compute the adjustment value in steps as  $PAdj / (1000000 / 2^{19}) = PAdj / (1.90735) = Adj$
7. If  $Adj < -65,536$ , the RC frequency is too high to be calibrated
8. Else if  $Adj < -32,768$ , set CMDR = 3, OFFSETR =  $Adj / 8$
9. Else if  $Adj < -16,384$ , set CMDR = 2, OFFSETR =  $Adj / 4$
10. Else if  $Adj < -8,192$ , set CMDR = 1, OFFSETR =  $Adj / 2$
11. Else if  $Adj < 8192$ , set CMDR = 0, OFFSETR =  $Adj$
12. Else if  $Adj < 16,384$ , set CMDR = 1, OFFSETR =  $Adj / 2$
13. Else if  $Adj < 32,768$ , set CMDR = 2, OFFSETR =  $Adj / 4$
14. Else if  $Adj < 65,536$ , set CMDR = 3, OFFSETR =  $Adj / 8$
15. Else the RC frequency is too low to be calibrated

### 5.10 Autocalibration

The AB08X5 includes a very powerful, patented automatic calibration feature, referred to as Autocalibration, which allows the RC Oscillator to be automatically calibrated to the XT Oscillator. The XT Oscillator typically has much better stability than the RC Oscillator but the RC Oscillator requires

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significantly less power. Autocalibration enables many system configurations to achieve accuracy and stability similar to that of the XT Oscillator while drawing current similar to that of the RC Oscillator. Autocalibration functions in two primary modes: XT Autocalibration Mode and RC Autocalibration Mode. See *Abracon Application Note – AB08X5/AB18X5 Family Autocalibration* for more details.

### 5.10.1 Autocalibration Operation

The Autocalibration operation counts the number of calibrated XT clock cycles within a specific period as defined by the RC Oscillator and then loads new values into the Calibration RC Upper and RC Lower registers which will then adjust the RC Oscillator output to match the XT frequency.

### 5.10.2 XT Autocalibration Mode

In XT Autocalibration Mode, the OSEL register bit is 0 and the AB08X5 uses the XT Oscillator whenever the system power VCC is above the  $V_{CCSWF}$  voltage. The RC Oscillator is periodically automatically calibrated to the XT Oscillator. If the AOS bit is set, when VCC drops below the  $V_{CCSWF}$  threshold the system will switch to using VBAT, the clocks will begin using the RC Oscillator, Autocalibration will be disabled and the XT Oscillator will be disabled to reduce power requirements. Because the RC Oscillator has been continuously calibrated to the XT Oscillator, it will be very accurate when the switch occurs. When VCC is again above the threshold, the system will switch back to use the XT Oscillator and restart Autocalibration.

### 5.10.3 RC Autocalibration Mode

In RC Autocalibration Mode, the OSEL register bit is 1 and the AB08X5 uses the RC Oscillator at all times. However, periodically the XT Oscillator is turned on and the RC Oscillator is calibrated to the XT Oscillator. This allows the system to operate most of the time with the XT Oscillator off but allow continuous calibration of the RC Oscillator.




### 5.10.4 Autocalibration Frequency and Control

The Autocalibration function is controlled by the ACAL field in the Oscillator Control register as shown in Table 14. If ACAL is 00, no Autocalibration occurs. If ACAL is 10 or 11, Autocalibration occurs every 1024 or 512 seconds, which is referred to as the Autocalibration Period (ACXP). In RC Autocalibration Mode, an Autocalibration operation results in the XT Oscillator being enabled for roughly 50 seconds. The 512 second Autocalibration cycles have the XT Oscillator enabled approximately 10% of the time, while 1024 second Autocalibration cycles have the XT Oscillator enabled approximately 4% of the time.

**Table 14: Autocalibration Modes**

ACAL Value	Calibration Mode
00	No Autocalibration
01	RESERVED
10	Autocalibrate every 1024seconds (~17minutes)
11	Autocalibrate every 512seconds (~9 minutes)

If ACAL is 00 and is then written with a different value, an Autocalibration cycle is immediately executed. This allows Autocalibration to be completely controlled by software. As an example, software could choose to execute an Autocalibration cycle every 2 hours by keeping ACAL at 00, getting a two hour interrupt using the alarm function, generating an Autocalibration cycle by writing ACAL to 10 or 11, and then returning ACAL to 00.

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### 5.10.5 Autocalibration Filter (AF) Pin

In order to produce the optimal accuracy for the Autocalibrated RC Oscillator, a filter pin AF is provided. A 47 pF capacitor should be connected between the AF pin and VSS. In order to enable the filter, the value 0xA0 must be written to the AFCTRL Register at address 0x26(see 0x26 – AFCTRL). The AF filter is disabled by writing 0x00 to the AFCTRL Register. No other values should be written to this register. The Configuration Key Register must be written with the value 0x9D immediately prior to writing the AFCTRL Register.

If the filter capacitor is not connected to the AF pin or is not enabled, the RC Oscillator frequency will typically be between 10 and 50 ppm slower than the XT Oscillator. If the capacitor is connected to the AF pin and enabled, the RC Oscillator frequency will be within the accuracy range specified in the Oscillator Parameters table of the XT Oscillator.

### 5.10.6 Autocalibration Fail

If the operating temperature of the AB08X5 exceeds the Autocalibration range specified in the Oscillator Parameters table or internal adjustment parameters are altered incorrectly, it is possible that the basic frequency of the RC Oscillator is so far away from the nominal 128 Hz value (off by more than 12%) that the RC Calibration circuitry does not have enough range to correctly calibrate the RC Oscillator. If this situation is detected during an Autocalibration operation, the ACF interrupt flag is set, an external interrupt is generated if the ACIE register bit is set and the Calibration RC registers are not updated.

If an Autocalibration failure is detected while running in RC Autocalibration mode, it is advisable to switch into XT Autocalibration mode to maintain the timing accuracy. This is done by first ensuring a crystal oscillator failure has not occurred (OF flag = 0) and then clearing the OSEL bit. The ACAL field should remain set to either 11 (512 second period) or 10 (1024 second period). After the switch occurs, the OMODE bit is cleared.

While continuing to operate in XT Autocalibration mode, the following steps can be used to determine when it is safe to return to RC Autocalibration mode.




1. Clear the ACF flag and ACIE register bit.
2. Setup the Countdown Timer or Alarm to interrupt after the next Autocalibration cycle completes or longer time period.
3. After the interrupt occurs, check the status of the ACF flag.
4. If the ACF flag is set, it is not safe to return to RC Autocalibration mode. Clear the ACF flag and repeat steps 2-4.
5. If the ACF flag is still cleared, it is safe to return to RC Autocalibration mode by setting the OSEL bit.

As mentioned in the RC oscillator section, switching between XT and RC oscillators is guaranteed to produce less than one second of error. However, this error needs to be considered and can be safely managed when implementing the steps above. For example, switching between oscillator modes every 48 hours will produce less than 6 ppm of error.

## 5.11 Oscillator Failure Detection

If the 32.786 kHz XT Oscillator generates clocks at less than 8 kHz for a period of more than 32 ms, the AB08X5 detects an Oscillator Failure. The Oscillator Failure function is controlled by several bits in the Oscillator Control Register (see 0x1C Oscillator Control) and the Oscillator Status Register (see 0x1D - Oscillator Status Register). The OF flag is set when an Oscillator Failure occurs, and is also set when the initially powers up. If the OFIE bit is set, the OF flag will generate an interrupt on IRQ.

If the FOS bit is set and the AB08X5 is currently using the XT Oscillator, it will automatically switch to the RC Oscillator on an Oscillator Failure. This guarantees that the system clock will not stop in any case. The

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OMODE bit indicates the currently selected oscillator, which will not match the oscillator requested by the OSEL bit if the XT Oscillator is not running.

The OF flag will be set when the AB08X5 powers up, and will also be set whenever the XT Oscillator is stopped. This can happen when the STOP bit is set or the OSEL bit is set to 1 to select the RC Oscillator. Since the XT Oscillator is stopped in RC Autocalibration mode (see RC Autocalibration Mode), OF will always be set in this mode. The OF flag should be cleared whenever the XT Oscillator is enabled prior to enabling the OF interrupt with OFIE.

## 5.12 Interrupts

The AB08X5 may generate a variety of interrupts which are ORed into the IRQ signal. This may be driven onto either the FOUT/nIRQ pin or the nIRQ2 pin depending on the configuration of the OUT1S and OUT2S fields (see 0x11 - Control2).

### 5.12.1 Interrupt Summary

The possible interrupts are summarized in Table 15. All enabled interrupts are ORed into the IRQ signal when their respective flags are set. Note that most interrupt outputs use the inverse of the interrupt (i.e. nIRQ). The fields are:

- Interrupt - the name of the specific interrupt.
- Function - the functional area which generates the interrupt.
- Enable - the register bit which enables the interrupt. Note that for the Watchdog interrupt, WDS is the steering bit, so that the flag generates an interrupt if WDS is 0 and a reset if WDS is 1. In either case, the BMB field must be non-zero to generate the interrupt or reset.
- Pulse/Level - some interrupts may be configured to generate a pulse based on the register bits in this column. "Level Only" implies that only a level may be generated, and the interrupt will only go away when the flag is reset by software.
- Flag - the register bit which indicates that the function has occurred. Note that the flag being set will only generate an interrupt signal on an external pin if the corresponding interrupt enable bit is also set.




**Table 15: Interrupt Summary**

Interrupt	Function	Enable	Pulse/Level	Flag
AIRQ	Alarm Match	AIE	IM	ALM
TIRQ	Countdown Timer	TIM	TM	TIM
WIRQ	Watchdog	!WDS	Level Only	WDT
BLIRQ	Battery Low	BLIE	Level Only	BL
X1IRQ	External 1	EX1E	Level Only	EX1
X2IRQ	External 2	EX2E	Level Only	EX2
OFIRQ	Oscillator Fail	OFIE	Level Only	OF
ACIRQ	Autocal Fail	ACIE	Level Only	ACF

### 5.12.2 Alarm Interrupt AIRQ

The AB08X5 may be configured to generate the AIRQ interrupt when the values in the Time and Date Registers match the values in the Alarm Registers. Which register comparisons are required to generate AIRQ is controlled by the RPT field as described in the Repeat Function table, allowing software to specify the interrupt interval. When an Alarm Interrupt is generated, the ALM flag is set and an external interrupt is



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generated based on the AIE bit and the pin configuration settings. The IM field controls the period of the external interrupt, including both level and pulse configurations.

### 5.12.3 Countdown Timer Interrupt TIRQ

The AB08X5 may be configured to generate the TIRQ interrupt when the Countdown Timer is enabled by the TE bit and reaches the value of zero, which will set the TIM flag. The TM, TRPT and TFS fields control the interrupt timing (see 0x18 - Countdown Timer Control), and the TIE bit and the pin configuration settings control external interrupt generation. The Timer interrupt is always driven onto the nTIRQ pin if it is available, and may also be driven onto a clock output pin by a configuration of the SQFS field (see 0x13 - SQW).

### 5.12.4 Watchdog Timer Interrupt WIRQ

The AB08X5 may be configured to generate the WIRQ interrupt when the Watchdog Timer reaches its timeout value. This sets the WDT flag and is described in Watchdog Timer.

### 5.12.5 Battery Low Interrupt BLIRQ

The AB08X5 may be configured to generate the BLIRQ when the voltage on the VBAT pin crosses one of the thresholds set by the BREF field. The polarity of the detected crossing is set by the BPOL bit.

### 5.12.6 External Interrupts X1IRQ and X2IRQ

The AB08X5 may be configured to generate the X1IRQ and X2IRQ interrupts when the EXTI (X1IRQ) or WDI (X2IRQ) inputs toggle. The register bits EX1P and EX2P control whether the rising or falling transitions generate the respective interrupt. Changing EX1P or EX2P may cause an immediate interrupt, so the corresponding interrupt flag should be cleared after changing these bits.

The values of the EXTI and WDI pins may be directly read in the EXIN and WDIN register bits (see 0x3F - Extension RAM Address). By connecting an input such as a pushbutton to both EXTI and WDI, software can debounce the switch input using software configurable delays.

### 5.12.7 Oscillator Fail Interrupt OFIRQ




The AB08X5 may be configured to generate the OFIRQ interrupt if the XT oscillator fails (see Oscillator Failure Detection).

### 5.12.8 Autocalibration Fail Interrupt ACIRQ

The AB08X5 may be configured to generate the ACIRQ interrupt if an Autocalibration operation fails (see Autocalibration Fail).

### 5.12.9 Servicing Interrupts

When an interrupt is detected, software must clear the interrupt flag in order to prepare for a subsequent interrupt. If only a single interrupt is enabled, software may simply write a zero to the corresponding interrupt flag to clear the interrupt. However, because all of the flags in the Status register are written at once, it is possible to clear an interrupt which has not been detected yet if multiple interrupts are enabled. The ARST register bit is provided to ensure that interrupts are not lost in this case. If ARST is a 1, a read of the Status register will produce the current state of all the interrupt flags and then clear them. An interrupt occurring at any time relative to this read is guaranteed to either produce a 1 on the Status read, or to set the corresponding flag after the clear caused by the Status read. After servicing all interrupts which produced 1s in the read, software should read the Status register again until it returns all zeros in the flags, and service any interrupts with flags of 1.

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Note that the OF and ACF interrupts are not handled with this process because they are in the Oscillator Status register, but error interrupts are very rare and typically do not create any problems if the interrupts are cleared by writing the flag directly.

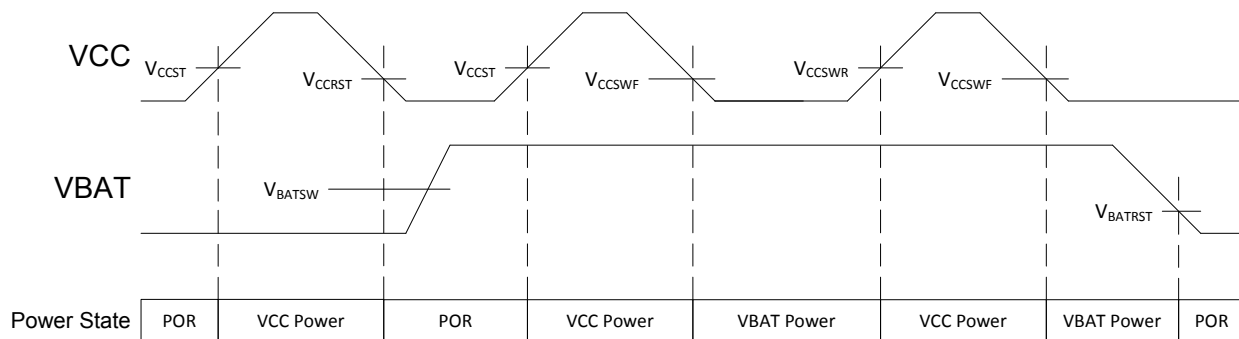
### 5.13 Power Control and Switching

The main power supply to the AB08X5 is the VCC pin, which operates over the range specified by the  $V_{CCIO}$  parameter if there are I/O interface operations required, and the range specified by the  $V_{CC}$  parameter if only timekeeping operations are required. Some versions also include a backup supply which is provided on the VBAT pin and must be in the range specified by the  $V_{BAT}$  parameter in order to supply battery power if  $V_{CC}$  is below  $V_{CCSWF}$ . Refer to the Power Supply and Switchover Parameters table for the specifications related to the power supplies and switchover. There are several functions which are directly related to the VBAT input. If a single power supply is used it must be connected to the VCC pin.

Figure 29 illustrates the various power states and the transitions between them. There are three power states:

1. POR – the power on reset state. If the AB08X5 is in this state, all registers including the Counter Registers are initialized to their reset values.
2. VCC Power – the AB08X5 is powered from the VCC supply.
3. VBAT Power – the AB08X5 is powered from the VBAT supply.




Initially, VCC is below the  $V_{CCST}$  voltage, VBAT is below the  $V_{BATSW}$  voltage and the AB08X5 is in the POR state. VCC rising above the  $V_{CCST}$  voltage causes the AB08X5 to enter the VCC Power state. If VBAT remains below  $V_{BATSW}$ , VCC falling below the  $V_{CCRST}$  voltage returns the AB08X5 to the POR state.



**Figure 29. Power States**

If VBAT rises above  $V_{BATSW}$  in the POR state, the AB08X5 remains in the POR state. This allows the AB08X5 to be built into a module with a battery included, and minimal current will be drawn from the battery until VCC is applied to the module the first time.

If the AB08X5 is in the VCC Power state and VBAT rises above  $V_{BATSW}$ , the AB08X5 remains in the VCC Power state but automatic switchover becomes available. VBAT falling below  $V_{BATSW}$  has no effect on the power state as long as VCC remains above  $V_{CCSWF}$ . If VCC falls below the  $V_{CCSWF}$  voltage while VBAT is above  $V_{BATSW}$  the AB08X5 switches to the VBAT Power state. VCC rising above  $V_{CCSWR}$  returns the AB08X5 to the VCC Power state. There is hysteresis in the rising and falling VCC thresholds to ensure that the AB08X5 does not switch back and forth between the supplies if VCC is near the thresholds.  $V_{CCSWF}$  and  $V_{CCSWR}$  are independent of the VBAT voltage and allow the AB08X5 to minimize the current drawn

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from the VBAT supply by switching to VBAT only at the point where VCC is no longer able to power the device.

If the AB08X5 is in the VBAT Power state and VBAT falls below  $V_{BATRST}$ , the AB08X5 will return to the POR state.

Whenever the AB08X5 enters the VBAT Power state, the BAT flag in the Status Register (see 0x0F - Status (Read Only)) is set and may be polled by software. If the XT oscillator is selected and the AOS bit (see 0x1C - Oscillator Control) is set, the AB08X5 will automatically switch to the RC oscillator in the VBAT Power state in order to conserve battery power. If the IOBM bit (see 0x27 – Batmode IO Register) is clear, the I<sup>2</sup>C or SPI interface is disabled in the VBAT Power state in order to prevent erroneous accesses to the AB08X5 if the bus master loses power.

### 5.13.1 Battery Low Flag and Interrupt

If the VBAT voltage drops below the Falling Threshold selected by the BREF field (see 0x21 - BREF Control), the BL flag in the Status Register (see 0x0F - Status (Read Only)) is set. If the BLIE interrupt enable bit (see 0x12 - Interrupt Mask) is set, the IRQ interrupt is generated. This allows software to determine if a backup battery has been drained. Note that the BPOL bit must be set to 0. The algorithm in the Analog Comparator section should be used when configuring the BREF value.

If the VBAT voltage is above the rising voltage which corresponds to the current BREF setting, BBOD will be set. At that point the VBAT voltage must fall below the falling voltage in order to clear the BBOD bit, set the BAT flag and generate a falling edge BL interrupt. If BBOD is clear, the VBAT voltage must rise above the rising voltage in order to clear the BBOD bit and generate a rising edge BL interrupt.

### 5.13.2 Analog Comparator

If a backup battery is not required, the VBAT pin may be used as an analog comparator input. The voltage comparison level is set by the BREF field. If the BPOL bit is 0, the BL flag will be set when the VBAT voltage crosses from above the BREF Falling Threshold to below it. If the BPOL bit is 1, the BL flag will be set when the VBAT voltage crosses from below the BREF Rising Threshold to above it. The BBOD bit in the Analog Status Register (see 0x2F – Analog Status Register (Read Only)) may be read to determine if the VBAT voltage is currently above the BREF threshold (BBOD = 1) or below the threshold (BBOD = 0).

There is a reasonably large delay (on the order of seconds) between changing the BREF field and a valid value of the BBOD bit. Therefore, the algorithm for using the Analog Comparator should comprise the following steps:




1. Set the BREF and BPOL fields to the desired values.
2. Wait longer than the maximum  $t_{BREF}$  time.
3. Clear the BL flag, which may have been erroneously set as BBOD settles.
4. Check the BBOD bit to ensure that the VBAT pin is at a level for which an interrupt can occur. If a falling interrupt is desired (BPOL = 0), BBOD should be 1. If a rising interrupt is desired (BPOL = 1), BBOD should be 0.

If the comparison voltage on the VBAT pin can remain when VCC goes to 0, it is recommended that a Software Reset be generated to the AB08X5 after power up.

### 5.13.3 Pin Control and Leakage Management

Like most ICs, the AB08X5 may draw unnecessary leakage current if an input pin floats to a value near the threshold or an output pin is pulled to a power supply. Because external devices may be powered from VCC, extra care must be taken to ensure that any input or output pins are handled correctly to avoid extraneous leakage when VCC goes away and the AB08X5 is powered from VBAT. The Output Control



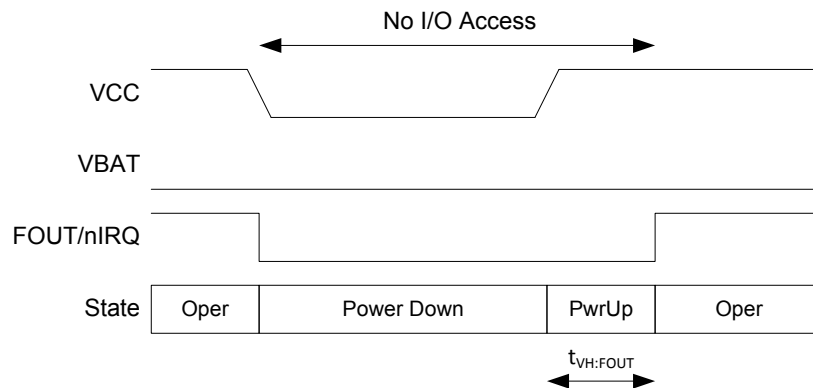
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register (see 0x30 – Output Control Register), the Batmode IO register (see 0x27 – Batmode IO Register) and the Extension RAM Address register (see 0x3F - Extension RAM Address) include bits to manage this leakage, which should be used as follows:




1. EXBM should be cleared if the EXTI pin is connected to a device which is powered down when the AB08X5 is in the VBAT Power state.
2. WDBM should be cleared if the WDI pin is connected to a device which is powered down when the AB08X5 is in the VBAT Power state.
3. IOBM should be cleared if the I<sup>2</sup>C or SPI bus master is powered down when the AB08X5 is in the VBAT Power state.

### 5.13.4 Power Up Timing

When the voltage levels on both the VCC and VBAT signals drop below  $V_{CCRST}$ , the AB08X5 will enter the POR state. Once VCC rises above  $V_{CCST}$ , the AB08X5 will enter the VCC Power state. I/O accesses via the I<sup>2</sup>C or SPI interface will be disabled for a period of  $t_{VH:FOUT}$ . The FOUT/nIRQ pin will be low at power up, and will go high when  $t_{VH:FOUT}$  expires. Software should poll the FOUT/nIRQ value to determine when the AB08X5 may be accessed. Figure 30 illustrates the timing of a power down/up operation.



**Figure 30. Power Up Timing**

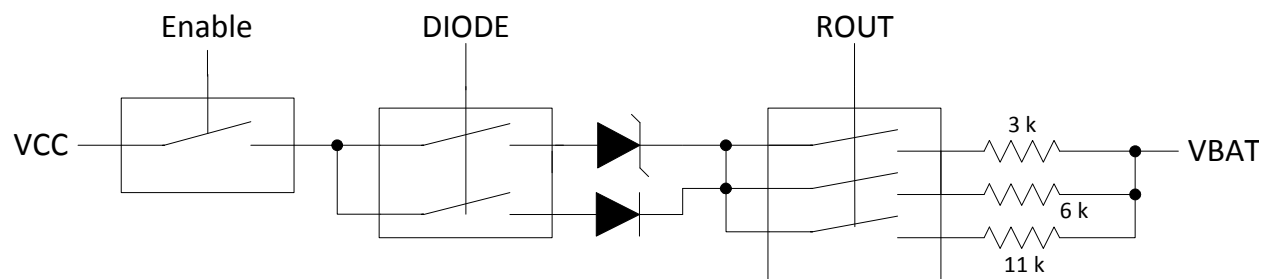
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## 5.14 Software Reset




Software may reset the AB08X5 by writing the special value of 0x3C to the Configuration Key register at offset 0x1F. This will provide the equivalent of a power on reset by initializing all of the AB08X5 registers.

## 5.15 Trickle Charger

The devices supporting the VBAT pin include a trickle charging circuit which allows a battery or supercapacitor connected to the VBAT pin to be charged from the power supply connected to the VCC pin. The circuit of the Trickle Charger is shown in Figure 31. The Trickle Charger configuration is controlled by the Trickle register (see 0x20 - Trickle). The Trickle Charger is enabled if a) the TCS field is 1010, b) the DIODE field is 01 or 10 and c) the ROUT field is not 00. A diode, with a typical voltage drop of 0.6V, is inserted in the charging path if DIODE is 10. A Schottky diode, with a typical voltage drop of 0.3V, is inserted in the charging path if DIODE is 01. The series current limiting resistor is selected by the ROUT field as shown in the figure.



**Figure 31. Trickle Charger**

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## 6. Registers

Registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte. Table 16 and Table 17 summarize the function of each register. In Table 16, the GPx bits (where x is between 0 and 27) are 28 register bits which may be used as general purpose storage. These bits are described in the sections below. All of the GPx bits are cleared when the AB08X5 powers up and they can therefore be used to allow software to determine if a true Power On Reset has occurred or hold other initialization data.

### 6.1 Register Definitions and Memory Map




**Table 16: Register Definitions (0x00 to 0x0F)**

Offset	Register	7	6	5	4	3	2	1	0
0x00	Hundredths	Seconds - Tenths				Seconds - Hundredths			
0x01	Seconds	GP0	Seconds - Tens			Seconds - Ones			
0x02	Minutes	GP1	Minutes - Tens			Minutes - Ones			
0x03	Hours (24 hour)	GP3	GP2	Hours - Tens		Hours - Ones			
0x03	Hours (12 hour)	GP3	GP2	AM/PM	Hours - Tens	Hours - Ones			
0x04	Date	GP5	GP4	Date - Tens		Date - Ones			
0x05	Months	GP8	GP7	GP6	Months - Tens	Months - Ones			
0x06	Years	Years - Tens				Years - Ones			
0x07	Weekdays	GP13	GP12	GP11	GP10	GP9	Weekdays		
0x08	Hundredths Alarm	Hundredths Alarm - Tenths				Hundredths Alarm - Hundredths			
0x09	Seconds Alarm	GP14	Seconds Alarm - Tens			Seconds Alarm - Ones			
0x0A	Minutes Alarm	GP15	Minutes Alarm - Tens			Minutes Alarm - Ones			
0x0B	Hours Alarm (24 hour)	GP17	GP16	Hours Alarm - Tens		Hours Alarm - Ones			
0x0B	Hours Alarm (12 hour)	GP17	GP16	AM/PM	Hours Alarm - Tens	Hours Alarm - Ones			
0x0C	Date Alarm	GP19	GP18	Date Alarm - Tens		Date Alarm - Ones			
0x0D	Months Alarm	GP22	GP21	GP20	Months Alarm - Tens	Months Alarm - Ones			
0x0E	Weekdays Alarm	GP27	GP26	GP25	GP24	GP23	Weekdays Alarm		
0x0F	Status	CB	BAT	WDT	BL	TIM	ALM	EX2	EX1

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**Table 17: Register Definitions (0x10 to 0xFF)**

Offset	Register	7	6	5	4	3	2	1	0	
0x10	Control1	STOP	12/24	OUTB	OUT	-	ARST	-	WRTC	
0x11	Control2	-	-	-	OUT2S			OUT1S		
0x12	IntMask	CEB	IM		BLIE	TIE	AIE	EX2E	EX1E	
0x13	SQW	SQWE	-		SQFS					
0x14	Cal_XT	CMDX	OFFSETX							
0x15	Cal_RC_Hi	CMDR		OFFSETR[13:8]						
0x16	Cal_RC_Low	OFFSETR[7:0]								
0x17	Int Polarity	-	-	EX2P	EX1P	-	-	-	-	
0x18	Timer Control	TE	TM	TRPT	RPT			TFS		
0x19	Timer	Countdown Timer								
0x1A	Timer_Initial	Timer Initial Value								
0x1B	WDT	WDS	BMB					WRB		
0x1C	Osc. Control	OSEL	ACAL		AOS	FOS	-	OFIE	ACIE	
0x1D	Osc. Status	XTCAL		LKO2	OMODE	-	-	OF	ACF	
0x1E	RESERVED	RESERVED								
0x1F	Configuration Key	Configuration Key								
0x20	Trickle	TCS			DIODE			ROUT		
0x21	BREF Control	BREF			-					
0x22	RESERVED	RESERVED								
0x23	RESERVED	RESERVED								
0x24	RESERVED	RESERVED								
0x25	RESERVED	RESERVED								
0x26	AFCTRL	AFCTRL								
0x27	BATMODE I/O	IOBM	RESERVED							
0x28	ID0 (Read only)	Part Number –MS Byte = 00001000 (0x08)								
0x29	ID1 (Read only)	Part Number – LS Byte (e.g. 00000101 for AB0805)								
0x2A	ID2 (Read only)	Revision – Major = 00010					Revision – Minor = 011			
0x2B	ID3 (Read only)	Lot[7:0]								
0x2C	ID4 (Read only)	Lot[9]	Unique ID[14:8]							
0x2D	ID5 (Read only)	Unique ID[7:0]								
0x2E	ID6 (Read only)	Lot[8]	Wafer					-	-	
0x2F	ASTAT	BBOD	BMIN	-	-	-	-	VINIT	-	
0x30	OCTRL	WDBM	EXBM	-	-	-	-	-	-	
0x3F	Extension Address	-	BPOL	WDIN	EXIN	-	XADA	XADS		
0x40–7F	RAM	Normal RAM Data								
0x80–FF	RAM	Alternate RAM Data (I <sup>2</sup> C Mode Only)								

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## 6.2 Time and Date Registers

### 6.2.1 0x00 - Hundredths

This register holds the count of hundredths of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 99. Note that in order to divide from 32.786 kHz, the hundredths register will not be fully accurate at all times but will be correct every 500 ms. Maximum jitter of this register will be less than 1 ms. The Hundredths Counter is not valid if the 128 Hz RC Oscillator is selected.

**Table 18: Hundredths Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	Seconds - Tenths				Seconds - Hundredths			
<b>Reset</b>	1	0	0	1	1	0	0	1

**Table 19: Hundredths Register Bits**

Bit	Name	Function
7:4	Seconds - Tenths	Holds the tenths place in the hundredths counter.
3:0	Seconds - Hundredths	Holds the hundredths place in the hundredths counter.

### 6.2.2 0x01 - Seconds




This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

**Table 20: Seconds Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	GP0	Seconds - Tens			Seconds - Ones			
<b>Reset</b>	0	0	0	0	0	0	0	0

**Table 21: Seconds Register Bits**

Bit	Name	Function
7	GP0	Register bit for general purpose use.
6:4	Seconds - Tens	Holds the tens place in the seconds counter.
3:0	Seconds - Ones	Holds the ones place in the seconds counter.

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### 6.2.3 0x02 - Minutes

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

**Table 22: Minutes Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	GP1	Minutes - Tens			Minutes - Ones			
<b>Reset</b>	0	0	0	0	0	0	0	0

**Table 23: Minutes Register Bits**

Bit	Name	Function
7	GP1	Register bit for general purpose use.
6:4	Minutes - Tens	Holds the tens place in the minutes counter.
3:0	Minutes - Ones	Holds the ones place in the minutes counter.

### 6.2.4 0x03 - Hours




This register holds the count of hours, in two binary coded decimal (BCD) digits. Values will be from 00 to 23 if the 12/24 bit (see 0x10 - Control1) is clear. If the 12/24 bit is set, the AM/PM bit will be 0 for AM hours and 1 for PM hours, and hour values will range from 1 to 12.

**Table 24: Hours Register (12 Hour Mode)**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	GP3	GP2	AM/PM	Hours - Tens	Hours - Ones			
<b>Reset</b>	0	0	0	0	0	0	0	0

**Table 25: Hours Register Bits (12 Hour Mode)**

Bit	Name	Function
7	GP3	Register bit for general purpose use.
6	GP2	Register bit for general purpose use.
5	AM/PM	0 = AM hours. 1 = PM hours.
4	Hours - Tens	Holds the tens place in the hours counter.
3:0	Hours - Ones	Holds the ones place in the hours counter.

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**Table 26: Hours Register (24 Hour Mode)**

Bit	7	6	5	4	3	2	1	0
Name	GP3	GP2	Hours - Tens		Hours - Ones			
Reset	0	0	0	0	0	0	0	0

**Table 27: Hours Register Bits (24 Hour Mode)**

Bit	Name	Function
7	GP3	Register bit for general purpose use.
6	GP2	Register bit for general purpose use.
5:4	Hours - Tens	Holds the tens place in the hours counter.
3:0	Hours - Ones	Holds the ones place in the hours counter.

### 6.2.5 0x04 - Date




This register holds the current day of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 1900 to 2199.

**Table 28: Date Register**

Bit	7	6	5	4	3	2	1	0
Name	GP5	GP4	Date - Tens		Date - Ones			
Reset	0	0	0	0	0	0	0	1

**Table 29: Date Register Bits**

Bit	Name	Function
7	GP5	Register bit for general purpose use.
6	GP4	Register bit for general purpose use.
5:4	Date - Tens	Holds the tens place in the date counter.
3:0	Date - Ones	Holds the ones place in the date counter.

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### 6.2.6 0x05 - Months

This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

**Table 30: Months Register**

Bit	7	6	5	4	3	2	1	0
Name	GP8	GP7	GP6	Months - Tens	Months - Ones			
Reset	0	0	0	0	0	0	0	1

**Table 31: Months Register Bits**

Bit	Name	Function
7	GP8	Register bit for general purpose use.
6	GP7	Register bit for general purpose use.
5	GP6	Register bit for general purpose use.
4	Months - Tens	Holds the tens place in the months counter.
3:0	Months - Ones	Holds the ones place in the months counter.

### 6.2.7 0x06 - Years

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.




**Table 32: Years Register**

Bit	7	6	5	4	3	2	1	0
Name	Years - Tens				Years - Ones			
Reset	0	0	0	0	0	0	0	0

**Table 33: Years Register Bits**

Bit	Name	Function
7:4	Years - Tens	Holds the tens place in the years counter.
3:0	Years - Ones	Holds the ones place in the years counter.



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### 6.2.8 0x07 - Weekday

This register holds the current day of the week. Values will range from 0 to 6.

**Table 34: Weekdays Register**

Bit	7	6	5	4	3	2	1	0
Name	GP13	GP12	GP11	GP10	GP9	Weekdays		
Reset	0	0	0	0	0	0	0	0

**Table 35: Weekdays Register Bits**

Bit	Name	Function
7	GP13	Register bit for general purpose use.
6	GP12	Register bit for general purpose use.
5	GP11	Register bit for general purpose use.
4	GP10	Register bit for general purpose use.
3	GP9	Register bit for general purpose use.
2:0	Weekdays	Holds the weekday counter value.

## 6.3 Alarm Registers

### 6.3.1 0x08 - Hundredths Alarm




This register holds the alarm value for hundredths of seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.

**Table 36: Hundredths Alarm Register**

Bit	7	6	5	4	3	2	1	0
Name	Seconds Alarm - Tenths				Seconds Alarm - Hundredths			
Reset	0	0	0	0	0	0	0	0

**Table 37: Hundredths Alarm Register Bits**

Bit	Name	Function
7:4	Seconds Alarm - Tenths	Holds the tenths place for the hundredths alarm.
3:0	Seconds Alarm - Hundredths	Holds the hundredths place for the hundredths alarm.

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### 6.3.2 0x09 - Seconds Alarm

This register holds the alarm value for seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

**Table 38: Seconds Alarm Register**

Bit	7	6	5	4	3	2	1	0
Name	GP14	Seconds Alarm - Tens			Seconds Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

**Table 39: Seconds Alarm Register Bits**

Bit	Name	Function
7	GP14	Register bit for general purpose use.
6:4	Seconds Alarm - Tens	Holds the tens place for the seconds alarm.
3:0	Seconds Alarm - Ones	Holds the ones place for the seconds alarm.

### 6.3.3 0x0A - Minutes Alarm




This register holds the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

**Table 40: Minutes Alarm Register**

Bit	7	6	5	4	3	2	1	0
Name	GP15	Minutes Alarm - Tens			Minutes Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

**Table 41: Minutes Alarm Register Bits**

Bit	Name	Function
7	GP15	Register bit for general purpose use.
6:4	Minute Alarm - Tens	Holds the tens place for the minutes alarm.
3:0	Minutes Alarm - Ones	Holds the ones place for the minutes alarm.

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### 6.3.4 0x0B - Hours Alarm

This register holds the alarm value for hours, in two binary coded decimal (BCD) digits. Values will range from 00 to 23 if the 12/24 bit (see 0x10 - Control1) is clear. If the 12/24 bit is set, the AM/PM bit will be 0 for AM hours and 1 for PM hours, and hour values will be from 1 to 12.

**Table 42: Hours Alarm Register (12 Hour Mode)**

Bit	7	6	5	4	3	2	1	0
Name	GP17	GP16	AM/PM	Hours Alarm - Tens	Hours Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

**Table 43: Hours Alarm Register Bits (12 Hour Mode)**




Bit	Name	Function
7	GP17	Register bit for general purpose use.
6	GP16	Register bit for general purpose use.
5	AM/PM	0 = AM hours. 1 = PM hours.
4	Hours Alarm - Tens	Holds the tens place for the hours alarm.
3:0	Hour Alarm - Ones	Holds the ones place for the hours alarm.

**Table 44: Hours Alarm Register (24 Hour Mode)**

Bit	7	6	5	4	3	2	1	0
Name	GP17	GP16	Hours Alarm - Tens		Hours Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

**Table 45: Hours Alarm Register Bits (24 Hour Mode)**

Bit	Name	Function
7	GP17	Register bit for general purpose use.
6	GP16	Register bit for general purpose use.
5:4	Hours Alarm - Tens	Holds the tens place for the hours alarm.
3:0	Hours Alarm - Ones	Holds the ones place for the hours alarm.

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### 6.3.5 0x0C - Date Alarm

This register holds alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 1900 to 2199.

**Table 46: Date Alarm Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	GP19	GP18	Date Alarm - Tens		Date Alarm - Ones			
<b>Reset</b>	0	0	0	0	0	0	0	0

**Table 47: Date Alarm Register Bits**

Bit	Name	Function
7	GP19	Register bit for general purpose use.
6	GP18	Register bit for general purpose use.
5:4	Date Alarm - Tens	Holds the tens place for the date alarm.
3:0	Date Alarm - Ones	Holds the ones place for the date alarm.

### 6.3.6 0x0D - Months Alarm




This register holds alarm value for months, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

**Table 48: Months Alarm Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	GP22	GP21	GP20	Months Alarm - Tens	Months Alarm - Ones			
<b>Reset</b>	0	0	0	0	0	0	0	0

**Table 49: Months Alarm Register Bits**

Bit	Name	Function
7	GP22	Register bit for general purpose use.
6	GP21	Register bit for general purpose use.
5	GP20	Register bit for general purpose use.
4	Months Alarm - Tens	Holds the tens place for the months alarm.
3:0	Months Alarm - Ones	Holds the ones place for the months alarm.

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### 6.3.7 0x0E - Weekday Alarm

This register holds the alarm value for the day of the week. Values will range from 0 to 6.

**Table 50: Weekdays Alarm Register**

Bit	7	6	5	4	3	2	1	0
Name	GP27	GP26	GP25	GP24	GP23	Weekdays Alarm		
Reset	0	0	0	0	0	0	0	0

**Table 51: Weekdays Alarm Register Bits**

Bit	Name	Function
7	GP27	Register bit for general purpose use.
6	GP26	Register bit for general purpose use.
5	GP25	Register bit for general purpose use.
4	GP24	Register bit for general purpose use.
3	GP23	Register bit for general purpose use.
2:0	Weekdays Alarm	Holds the weekdays alarm value.

## 6.4 Configuration Registers

### 6.4.1 0x0F - Status (Read Only)




This register holds a variety of status bits. The register may be written at any time to clear or set any status flag. If the ARST bit is set, any read of the Status Register will clear all of the bits except the CB bit.

**Table 52: Status Register**

Bit	7	6	5	4	3	2	1	0
Name	CB	BAT	WDT	BL	TIM	ALM	EX2	EX1
Reset	0	0	0	0	0	0	0	0

**Table 53: Status Register Bits**

Bit	Name	Function
7	CB	Century. This bit will be toggled when the Years register rolls over from 99 to 00 if the CEB bit is a 1. A 0 assumes the century is 19xx or 21xx, and a 1 assumes it is 20xx for leap year calculations.
6	BAT	Set when the system switches to the VBAT Power state.
5	WDT	Set when the Watchdog Timer is enabled and is triggered, and the WDS bit is 0.
4	BL	Set if the battery voltage VBAT crosses the reference voltage selected by BREF in the direction selected by BPOL.
3	TIM	Set when the Countdown Timer is enabled and reaches zero.

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**Table 53: Status Register Bits**

Bit	Name	Function
2	ALM	Set when the Alarm function is enabled and all selected Alarm registers match their respective counters.
1	EX2	Set when an external trigger is detected on the WDI pin. The EX2E bit must be set in order for this interrupt to occur, but subsequently clearing EX2E will not automatically clear this flag.
0	EX1	Set when an external trigger is detected on the EXT1 pin. The EX1E bit must be set in order for this interrupt to occur, but subsequently clearing EX1E will not automatically clear this flag.

### 6.4.2 0x10 - Control1




This register holds some major control signals.

**Table 54: Control1 Register**

Bit	7	6	5	4	3	2	1	0
Name	STOP	12/24	OUTB	OUT	RESERVED	ARST	RESERVED	WRTC
Reset	0	0	0	1	0	0	0	1

**Table 55: Control1 Register Bits**

Bit	Name	Function
7	STOP	When 1, stops the clocking system. The XT and RC Oscillators are not stopped. In XT Mode the 32.786 kHz clock output will continue to run. In RC Mode, the 128 Hz clock output will continue to run. Other clock output selections will produce static outputs. This bit allows the clock system to be precisely started, by setting it to 1 and back to 0.
6	12/24	When 0, the Hours register operates in 24 hour mode. When 1, the Hours register operates in 12 hour mode.
5	OUTB	A static value which may be driven on the nIRQ2 pin. The OUTB bit cannot be set to 1 if the LKO2 bit is 1.
4	OUT	A static value which may be driven on the FOUT/nIRQ pin. This bit also defines the default value for the Square Wave output when SQWE is not asserted.
3	RESERVED	RESERVED
2	ARST	Auto reset enable. When 1, a read of the Status register will cause any interrupt bits (TIM, BL, ALM, WDT, XT1, XT2) to be cleared. When 0, the bits must be explicitly cleared by writing the Status register.
1	RESERVED	RESERVED
0	WRTC	Write RTC. This bit must be set in order to write any of the Counter registers (Hundredths, Seconds, Minutes, Hours, Date, Months, Years or Weekdays).

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### 6.4.3 0x11 - Control2

This register holds additional control and configuration signals for the flexible output pins FOUT/nIRQ and nIRQ2. Note that nIRQ2 and FOUT/nIRQ are open drain outputs.

**Table 56: Control2 Register**

Bit	7	6	5	4	3	2	1	0
Name	RESERVED			OUT2S			OUT1S	
Reset	0	0	0	0	0	0	0	0

**Table 57: Control2 Register Bits**




Bit	Name	Function
7:5	RESERVED	RESERVED
4:2	OUT2S	Controls the function of the nIRQ2 pin, as shown in Table 58.
1:0	OUT1S	Controls the function of the FOUT/nIRQ pin, as shown in Table 59.

**Table 58: nIRQ2 Pin Control**

OUT2S Value	nIRQ2 Pin Function
000	nIRQ if at least one interrupt is enabled, else OUTB
001	SQW if SQWE = 1, else OUTB
010	RESERVED
011	nAIRQ if AIE is set, else OUTB
100	TIRQ if TIE is set, else OUTB
101	nTIRQ if TIE is set, else OUTB
110	RESERVED
111	OUTB

**Table 59: FOUT/nIRQ Pin Control**

OUT1S Value	FOUT/nIRQ Pin Function
00	nIRQ if at least one interrupt is enabled, else OUT
01	SQW if SQWE = 1, else OUT
10	SQW if SQWE = 1, else nIRQ if at least one interrupt is enabled, else OUT
11	nAIRQ if AIE is set, else OUT

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#### 6.4.4 0x12 - Interrupt Mask

This register holds the interrupt enable bits and other configuration information.




**Table 60: Interrupt Mask Register**

Bit	7	6	5	4	3	2	1	0
Name	CEB	IM		BLIE	TIE	AIE	EX2E	EX1E
Reset	1	1	1	0	0	0	0	0

**Table 61: Interrupt Mask Register Bits**

Bit	Name	Function
7	CEB	Century Enable. 0: The CB bit will never be automatically updated. 1: The CB bit will toggle when the Years register rolls over from 99 to 00.
6:5	IM	Interrupt Mode. This controls the duration of the nAIRQ interrupt as shown below. The interrupt output always goes high when the corresponding flag in the Status Register is cleared. In order to minimize current drawn by the AB08X5 this field should be kept at 0x3. 00: Level (static) for both XT mode and RC mode. 01: 1/8192 seconds for XT mode. 1/64 seconds for RC mode. 10: 1/64 seconds for both XT mode and RC mode. 11: 1/4 seconds for both XT mode and RC mode.
4	BLIE	Battery Low Interrupt Enable. 0: Disable the battery low interrupt. 1: The battery low detection will generate an interrupt.
3	TIE	Timer Interrupt Enable. 0: Disable the timer interrupt. 1: The Countdown Timer will generate an IRQ interrupt signal and set the TIM flag when the timer reaches 0.
2	AIE	Alarm Interrupt Enable. 0: Disable the alarm interrupt. 1: A match of all the enabled alarm registers will generate an IRQ interrupt signal.
1	EX2E	XT2 Interrupt Enable. 0: Disable the XT2 interrupt. 1: The WDI input pin will generate the XT2 interrupt when the edge specified by EX2P occurs.
0	EX1E	XT1 Interrupt Enable. 0: Disable the XT1 interrupt. 1: The EX1I input pin will generate the XT1 interrupt when the edge specified by EX1P occurs.



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### 6.4.5 0x13 - SQW

This register holds the control signals for the square wave output. Note that some frequency selections are not valid if the 128 Hz RC Oscillator is selected.

**Table 62: SQW Register**




Bit	7	6	5	4	3	2	1	0
Name	SQWE	RESERVED		SQFS				
Reset	0	0	1	0	0	1	1	0

**Table 63: SQW Register Bits**

Bit	Name	Function
7	SQWE	When 1, the square wave output is enabled. When 0, the square wave output is held at the value of OUT.
6:5	RESERVED	RESERVED
4:0	SQFS	Selects the frequency of the square wave output, as shown in Table 64. Note that some selections are not valid if the 128 Hz oscillator is selected. Some selections also produce short pulses rather than square waves, and are intended primarily for test usage.

**Table 64: Square Wave Function Select**

SQFS Value	Square Wave Output
00000	1 century <sup>(2)</sup>
00001	32.768 kHz <sup>(1)</sup>
00010	8.192 kHz <sup>(1)</sup>
00011	4.096 kHz <sup>(1)</sup>
00100	2.048 kHz <sup>(1)</sup>
00101	1.024 kHz <sup>(1)</sup>
00110	512 Hz <sup>(1)</sup> – Default value
00111	256 Hz <sup>(1)</sup>
01000	128 Hz
01001	64 Hz
01010	32 Hz
01011	16 Hz
01100	8 Hz
01101	4 Hz
01110	2 Hz
01111	1 Hz

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**Table 64: Square Wave Function Select**

SQFS Value	Square Wave Output
10000	½ Hz
10001	¼ Hz
10010	1/8 Hz
10011	1/16 Hz
10100	1/32 Hz
10101	1/60 Hz (1 minute)
10110	16.384 kHz <sup>(1)</sup>
10111	100 Hz <sup>(1)(2)</sup>
11000	1 hour <sup>(2)</sup>
11001	1 day <sup>(2)</sup>
11010	TIRQ
11011	NOT TIRQ
11100	1 year <sup>(2)</sup>
11101	1 Hz to Counters <sup>(2)</sup>
11110	1/32 Hz from Acal <sup>(2)</sup>
11111	1/8 Hz from Acal <sup>(2)</sup>

<sup>(1)</sup> NA if 128 Hz Oscillator selected.  
<sup>(2)</sup> Pulses for Test Usage.

## 6.5 Calibration Registers

### 6.5.1 0x14 - Calibration XT




This register holds the control signals for a digital calibration function of the XT Oscillator.

**Table 65: Calibration XT Register**

Bit	7	6	5	4	3	2	1	0
Name	CMDX	OFFSETX						
Reset	0	0	0	0	0	0	0	0

**Table 66: Calibration XT Register Bits**

Bit	Name	Function
7	CMDX	The calibration adjust mode. When 0 (Normal Mode), each adjustment step is +/- 2 ppm. When 1 (Coarse Mode), each adjustment step is +/- 4 ppm.
6:0	OFFSETX	The amount to adjust the effective time. This is a two's complement number with a range of -64 to +63 adjustment steps.

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### 6.5.2 0x15 - Calibration RC Upper

This register holds the control signals for the fine digital calibration function of the low power RC Oscillator. This register is initialized with a factory value which calibrates the RC Oscillator to 128 Hz.

**Table 67: Calibration RC Upper Register**

Bit	7	6	5	4	3	2	1	0
Name	CMDR		OFFSETRU					
Reset	Preconfigured		Preconfigured					

**Table 68: Calibration RC Upper Register Bits**

Bit	Name	Function
7:6	CMDR	The calibration adjust mode for the RC calibration adjustment. CMDR selects the highest frequency used in the RC Calibration process, as shown in Table 69.
5:0	OFFSETRU	The upper 6 bits of the OFFSETR field, which is used to set the amount to adjust the effective time. OFFSETR is a two's complement number with a range of $-2^{13}$ to $+2^{13}-1$ adjustment steps.

**Table 69: CMDR Function**




CMDR	Calibration Period	Minimum Adjustment	Maximum Adjustment
00	8,192 seconds	+/-1.91 ppm	+/-1.56%
01	4,096 seconds	+/-3.82 ppm	+/-3.13%
10	2,048 seconds	+/-7.64 ppm	+/-6.25%
11	1,024 seconds	+/-15.28 ppm	+/-12.5%

### 6.5.3 0x16 - Calibration RC Lower

This register holds the lower 8 bits of the OFFSETR field for the digital calibration function of the low power RC Oscillator. This register is initialized with a factory value which calibrates the RC Oscillator to 128 Hz.

**Table 70: Calibration RC Lower Register**

Bit	7	6	5	4	3	2	1	0
Name	OFFSETRL							
Reset	Preconfigured							

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**Table 71: Calibration RC Lower Register Bits**

Bit	Name	Function
7:0	OFFSETRL	The lower 8 bits of the OFFSETR field, which is used to set the amount to adjust the effective time. OFFSETR is a two's complement number with a range of $-2^{13}$ to $+2^{13}-1$ adjustment steps.

## 6.6 Interrupt Polarity Control Register

### 6.6.1 0x17 - Interrupt Polarity Control

This register controls the external interrupt polarity.

**Table 72: Interrupt Polarity Control Register**

Bit	7	6	5	4	3	2	1	0
Name	RESERVED		EX2P	EX1P	RESERVED			
Reset	0	0	0	0	0	0	0	0




**Table 73: Interrupt Polarity Control Register Bits**

Bit	Name	Function
7:6	RESERVED	RESERVED
5	EX2P	When 1, the external interrupt XT2 will trigger on a rising edge of the WDI pin. When 0, the external interrupt XT2 will trigger on a falling edge of the WDI pin.
4	EX1P	When 1, the external interrupt XT1 will trigger on a rising edge of the EXTI pin. When 0, the external interrupt XT1 will trigger on a falling edge of the EXTI pin.
3:0	RESERVED	RESERVED

## 6.7 Timer Registers

### 6.7.1 0x18 - Countdown Timer Control

This register controls the Countdown Timer function. Note that the 00 frequency selection is slightly different depending on whether the 32.786 kHz XT Oscillator or the 128 Hz RC Oscillator is selected. In some RC Oscillator modes, the interrupt pulse output is specified as RCPLS. In these cases the interrupt output will be a short negative going pulse which is typically between 100 and 400  $\mu$ s. This allows control

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of external devices which require pulses shorter than the minimum 7.8 ms pulse created directly by the RC Oscillator.

**Table 74: Countdown Timer Control Register**




Bit	7	6	5	4	3	2	1	0
<b>Name</b>	TE	TM	TRPT	RPT			TFS	
<b>Reset</b>	0	0	1	0	0	0	1	1

**Table 75: Countdown Timer Control Register Bits**

Bit	Name	Function
7	TE	Timer Enable. When 1, the Countdown Timer will count down. When 0, the Countdown Timer retains the current value. If TE is 0, the clock to the Timer is disabled for power minimization.
6	TM	Timer Interrupt Mode. Along with TRPT, this controls the Timer Interrupt function as shown in Table 28. A Level Interrupt will cause the nIRQ signal to be driven low by a Countdown Timer interrupt until the associated flag is cleared. A Pulse interrupt will cause the nIRQ signal to be driven low for the time shown in Table 77 or until the flag is cleared.
5	TRPT	Along with TM, this controls the repeat function of the Countdown Timer. If Repeat is selected, the Countdown Timer reloads the value from the Timer_Initial register upon reaching 0, and continues counting. If Single is selected, the Countdown Timer will halt when it reaches zero. This allows the generation of periodic interrupts of virtually any frequency.
4:2	RPT	These bits enable the Alarm Interrupt repeat function, as shown in Table 76. HA is the Hundredths_Alarm register value.
1:0	TFS	Select the clock frequency and interrupt pulse width of the Countdown Timer, as defined in Table 77. RCPLS is a 100-400 $\mu$ s pulse.

**Table 76: Repeat Function**

RPT	HA	Repeat When
7	FF	Once per hundredth (*)
7	F[9-0]	Once per tenth (*)
7	[9-0][9-0]	Hundredths match (once per second)
6		Hundredths and seconds match (once per minute)
5		Hundredths, seconds and minutes match (once per hour)
4		Hundredths, seconds, minutes and hours match (once per day)
3		Hundredths, seconds, minutes, hours and weekday match (once per week)
2		Hundredths, seconds, minutes, hours and date match (once per month)
1		Hundredths, seconds, minutes, hours, date and month match (once per year)
0		Alarm Disabled
(*)Once per second if 128 Hz Oscillator selected		

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**Table 77: Countdown Timer Function Select**

TM	TRPT	TFS	Int	Repeat	Countdown Timer Frequency		Interrupt Pulse Width	
					32.786 kHz Oscillator	128 Hz Oscillator	32.786 kHz Oscillator	128 Hz Oscillator
0	0	00	Pulse	Single	4.096 kHz	128 Hz	1/4096 s	1/128 s
0	0	01	Pulse	Single	64 Hz	64 Hz	1/128 s	1/128 s
0	0	10	Pulse	Single	1 Hz	1 Hz	1/64 s	1/64 s
0	0	11	Pulse	Single	1/60 Hz	1/60 Hz	1/64 s	1/64 s
0	1	00	Pulse	Repeat	4.096 kHz	128 Hz	1/4096 s	1/128 s
0	1	01	Pulse	Repeat	64 Hz	64 Hz	1/128 s	1/128 s
0	1	10	Pulse	Repeat	1 Hz	1 Hz	1/64 s	1/64 s
0	1	11	Pulse	Repeat	1/60 Hz	1/60 Hz	1/64 s	1/64 s
1	0	00	Level	Single	4.096 kHz	128 Hz	N/A	N/A
1	0	01	Level	Single	64 Hz	64 Hz	N/A	N/A
1	0	10	Level	Single	1 Hz	1 Hz	N/A	N/A
1	0	11	Level	Single	1/60 Hz	1/60 Hz	N/A	N/A
1	1	00	Pulse	Repeat	4.096 kHz	128 Hz	1/4096 s	RCPLS
1	1	01	Pulse	Repeat	64 Hz	64 Hz	1/4096 s	RCPLS
1	1	10	Pulse	Repeat	1 Hz	1 Hz	1/4096 s	RCPLS
1	1	11	Pulse	Repeat	1/60 Hz	1/60 Hz	1/4096 s	RCPLS

### 6.7.2 0x19 - Countdown Timer




This register holds the current value of the Countdown Timer. It may be loaded with the desired starting value when the Countdown Timer is stopped.

**Table 78: Countdown Timer Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	Countdown Timer							
<b>Reset</b>	0	0	0	0	0	0	0	0

**Table 79: Countdown Timer Register Bits**

Bit	Name	Function
7:0	Countdown Timer	The current value of the Countdown Timer.

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### 6.7.3 0x1A - Timer Initial Value

This register holds the value which will be reloaded into the Countdown Timer when it reaches zero if the TRPT bit is a 1. This allows for periodic timer interrupts, and a period of  $(\text{Timer\_initial} + 1) * (1/\text{Countdown\_frequency})$ .

**Table 80: Timer Initial Value Register**

Bit	7	6	5	4	3	2	1	0
Name	Timer Initial Value							
Reset	0	0	0	0	0	0	0	0

**Table 81: Timer Initial Value Register Bits**

Bit	Name	Function
7:0	Timer Initial Value	The value reloaded into the Countdown Timer when it reaches zero if the TRPT bit is a 1.

### 6.7.4 0x1B - Watchdog Timer




This register controls the Watchdog Timer function.

**Table 82: Watchdog Timer Register**

Bit	7	6	5	4	3	2	1	0
Name	WDS	BMB				WRB		
Reset	0	0	0	0	0	0	0	0

**Table 83: Watchdog Timer Register Bits**

Bit	Name	Function
7	WDS	Watchdog Steering. When 0, the Watchdog Timer will generate WIRQ when it times out. When 1, the Watchdog Timer will generate a reset when it times out.
6:2	BMB	The number of clock cycles which must occur before the Watchdog Timer times out. A value of 00000 disables the Watchdog Timer function.
1:0	WRB	The clock frequency of the Watchdog Timer, as shown in Table 84.

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**Table 84: Watchdog Timer Frequency Select**

WRB Value	Watchdog Timer Frequency
00	16 Hz
01	4 Hz
10	1 Hz
11	1/4 Hz

## 6.8 Oscillator Registers

### 6.8.1 0x1C - Oscillator Control

This register controls the overall Oscillator function. It may only be written if the Configuration Key register contains the value 0xA1. An Autocalibration cycle is initiated immediately whenever this register is written with a value in the ACAL field which is not zero.

**Table 85: Oscillator Control Register**




Bit	7	6	5	4	3	2	1	0
<b>Name</b>	OSEL	ACAL		AOS	FOS	RESERVED	OFIE	ACIE
<b>Reset</b>	0	0	0	0	0	0	0	0

**Table 86: Oscillator Control Register Bits**

Bit	Name	Function
7	OSEL	When 1, request the RC Oscillator to generate a 128 Hz clock for the timer circuits. When 0, request the XT Oscillator to generate a 32.786 kHz clock to the timer circuit. Note that if the XT Oscillator is not operating, the oscillator switch will not occur. The OMODE field in the Oscillator Status register indicates the actual oscillator which is selected.
6:5	ACAL	Controls the automatic calibration function, as described in Autocalibration.
4	AOS	When 1, the oscillator will automatically switch to RC oscillator mode when the system is powered from the battery. When 0, no automatic switching occurs.
3	FOS	When 1, the oscillator will automatically switch to RC oscillator mode when an oscillator failure is detected. When 0, no automatic switching occurs.
2	RESERVED	RESERVED
1	OFIE	Oscillator Fail interrupt enable. When 1, an Oscillator Failure will generate an IRQ signal.
0	ACIE	When 1, an Autocalibration Failure will generate an interrupt.





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**Table 90: Configuration Key Register Bits**

Bit	Name	Function
7:0	Configuration Key	Written with specific values in order to access some registers and functions.

1. Writing a value of 0xA1 enables write access to the Oscillator Control register
2. Writing a value of 0x3C does not update the Configuration Key register, but generates a Software Reset (see Software Reset).
3. Writing a value of 0x9D enables write access to the Trickle Register (0x20), the BREF Register (0x21), the AFCTRL Register (0x26), the Batmode I/O Register (0x27) and the Output Control Register (0x30).

## 6.10 Analog Control Registers

### 6.10.1 0x20 - Trickle

This register controls the Trickle Charger. The Key Register must be written with the value 0x9D in order to enable access to this register.

**Table 91: Trickle Register**




Bit	7	6	5	4	3	2	1	0
Name	TCS				DIODE		ROUT	
Reset	0	0	0	0	0	0	0	0

**Table 92: Trickle Register Bits**

Bit	Name	Function
7:4	TCS	A value of 1010 enables the trickle charge function. All other values disable the Trickle Charger.
3:2	DIODE	Diode Select. A value of 10 inserts a standard diode into the trickle charge circuit, with a voltage drop of 0.6V. A value of 01 inserts a schottky diode into the trickle charge circuit, with a voltage drop of 0.3V. Other values disable the Trickle Charger.
1:0	ROUT	Output Resistor. This selects the output resistor of the trickle charge circuit, as shown in Table 93.

**Table 93: Trickle Charge Output Resistor**

ROUT Value	Series Resistor
00	Disable
01	3 K $\Omega$
10	6 K $\Omega$
11	11 K $\Omega$

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### 6.10.2 0x21 - BREF Control

This register controls the reference voltages used in the Wakeup Control system. The Key Register must be written with the value 0x9D in order to enable access to this register.

**Table 94: BREF Control Register**

Bit	7	6	5	4	3	2	1	0
Name	BREF				RESERVED			
Reset	1	1	1	1	0	0	0	0

**Table 95: BREF Control Register Bits**

Bit	Name	Function
7:4	BREF	This selects the voltage reference which is compared to the battery voltage VBAT to produce the BBOD signal. Typical values are shown in Table 96. The valid BREF values are 0x7, 0xB, 0xD, and 0xF. The reset value is 0xF. All other values are RESERVED.
3:0	RESERVED	RESERVED

**Table 96: VBAT Reference Voltage**

BREF Value	VBAT Falling Voltage (TYP)	VBAT Rising Voltage (TYP)
0111	2.5V	3.0V
1011	2.1V	2.5V
1101	1.8V	2.2V
1111	1.4V	1.6V




### 6.10.3 0x26 – AFCTRL

This register holds the enable code for the Autocalibration Filter (AF) filter capacitor connected to the AF pin. Writing the value 0xA0 to this register enables the AF pin. Writing the value 0x00 to this register disables the AF pin. No other value may be written to this register. The Configuration Key Register must be written with the value 0x9D prior to writing the AFCTRL Register.

**Table 97: AFCTRL Register**

Bit	7	6	5	4	3	2	1	0
Name	AFCTRL							
Reset	0	0	0	0	0	0	0	0



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**Table 102: Analog Status Register Bits**

Bit	Name	Function
7	BBOD	If 1, the VBAT input voltage is above the BREF threshold.
6	BMIN	If 1, the VBAT input voltage is above the minimum operating voltage (1.2 V).
5:2	RESERVED	RESERVED
1	VINIT	If 1, the VCC input voltage is above the minimum power up voltage (1.6 V).
0	RESERVED	RESERVED

### 6.10.6 0x30 – Output Control Register

This register holds bits which control the behavior of the I/O pins under various power down conditions. The Key Register must be written with the value 0x9D in order to enable access to this register.

**Table 103: Output Control Register**

Bit	7	6	5	4	3	2	1	0
Name	WDBM	EXBM	RESERVED					
Reset	0	0	0	0	0	0	0	0

**Table 104: Output Control Register Bits**

Bit	Name	Function
7	WDBM	If 1, the WDI input is enabled when the AB08X5 is powered from VBAT. If 0, the WDI input is disabled when the AB08X5 is powered from VBAT.
6	EXBM	If 1, the EXTI input is enabled when the AB08X5 is powered from VBAT. If 0, the EXTI input is disabled when the AB08X5 is powered from VBAT.
5:0	RESERVED	




## 6.11 ID Registers

### 6.11.1 0x28 – ID0 - Part Number Upper Register (Read Only)

This register holds the upper eight bits of the part number in BCD format, which is always 0x08 for the AB08X5 family.

**Table 105: 28 – ID0 – Part Number Upper Register**

Bit	7	6	5	4	3	2	1	0
Name	Part Number - Digit 3				Part Number - Digit 2			
Reset	0	0	0	0	1	0	0	0

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### 6.11.2 0x29 – ID1 - Part Number Lower Register (Read Only)

This register holds the lower eight bits of the part number in BCD format.

**Table 106: 28 – ID1 – Part Number Lower Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	Part Number - Digit 1				Part Number - Digit 0			
<b>Reset</b>	Preconfigured Digit 1				Preconfigured Digit 0			

### 6.11.3 0x2A – ID2 - Part Revision (Read Only)

This register holds the Revision number of the part.

**Table 107: 2A – ID2 – Part Revision Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	MAJOR					MINOR		
<b>Reset</b>	0	0	0	1	0	0	1	1

**Table 108: 2A – ID2 – Part Revision Register Bits**

Bit	Name	Function
7:3	MAJOR	This field holds the major revision of the AB08X5.
2:0	MINOR	This field holds the minor revision of the AB08X5.

### 6.11.4 0x2B – ID3 – Lot Lower (Read Only)




This register holds the lower 8 bits of the manufacturing lot number.

**Table 109: 2B – ID3 – Lot Lower Register**

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	Lot[7:0]							
<b>Reset</b>	Preconfigured Lot Number							

**Table 110: 2B – ID3 – Lot Lower Register Bits**

Bit	Name	Function
7:0	Lot[7:0]	This field holds the lower 8 bits of the manufacturing lot number.

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### 6.11.5 0x2C – ID4 – ID Upper (Read Only)

This register holds part of the manufacturing information of the part, including bit 9 of the manufacturing lot number and the upper 7 bits of the unique part identifier. The 15-bit ID field contains a unique value for each AB08X5 part.

**Table 111: 2C – ID4 – ID Upper Register**

Bit	7	6	5	4	3	2	1	0
Name	Lot[9]	ID[14:8]						
Reset	Preconfigured Value							

**Table 112: 2C – ID4 – ID Upper Register Bits**

Bit	Name	Function
7	Lot[9]	This field holds bit 9 of the manufacturing lot number.
1:0	ID[14:8]	This field holds the upper 7 bits of the unique part ID.

### 6.11.6 0x2D – ID5 – Unique Lower (Read Only)




This register holds the lower 8 bits of the unique part identifier. The 15-bit ID field contains a unique value for each AB08X5 part.

**Table 113: 2D – ID5 – ID Lower Register**

Bit	7	6	5	4	3	2	1	0
Name	ID[7:0]							
Reset	Preconfigured Value							

**Table 114: 2D – ID5 – ID Lower Register Bits**

Bit	Name	Function
7:0	ID[7:0]	This field holds the lower 8 bits of the unique part ID.

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### 6.11.7 0x2E – ID6 – Wafer (Read Only)

**Table 115: 2E – ID6 – Wafer Register**

Bit	7	6	5	4	3	2	1	0	
Name	Lot[8]	Wafer					RESERVED		
Reset	Preconfigured Value								

**Table 116: 2E – ID6 – Wafer Register Bits**

Bit	Name	Function
7	Lot[8]	This field holds bit 8 of the manufacturing lot number.
6:2	Wafer	This field holds the manufacturing wafer number.
1:0	RESERVED	RESERVED

## 6.12 Ram Registers

### 6.12.1 0x3F - Extension RAM Address

This register controls access to the Extension RAM, and includes some miscellaneous control bits.




**Table 117: 3F – Extension RAM Address Register**

Bit	7	6	5	4	3	2	1	0
Name	RSVD	BPOL	WDIN	EXIN	RSVD	XADA	XADS	
Reset	0	0	Read Only		0	0	0	0

**Table 118: 3F – Extension RAM Address Register Bits**

Bit	Name	Function
7	RSVD	RESERVED.
6	BPOL	BL Polarity. When 0, the Battery Low flag BL is set when the VBAT voltage goes below the BREF threshold. When 1, the Battery Low flag BL is set when the VBAT voltage goes above the BREF threshold.
5	WDIN	(read only) – this bit supplies the current level of the WDI pin.
4	EXIN	(read only) – this bit supplies the current level of the EXTI pin.
3	RSVD	RESERVED.
2	XADA	This field supplies the upper bit for addresses to the Alternate RAM address space.
1:0	XADS	This field supplies the upper two address bits for the Standard RAM address space.






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### **6.12.2 0x40 - 0x7F – Standard RAM**

64 bytes of RAM space which may be accessed in either I<sup>2</sup>C or SPI interface mode. The data in the RAM is held when using battery power. The upper 2 bits of the RAM address are taken from the XADS field, and the lower 6 bits are taken from the address offset, supporting a total RAM of 256 bytes. The initial values of the RAM locations are undefined.

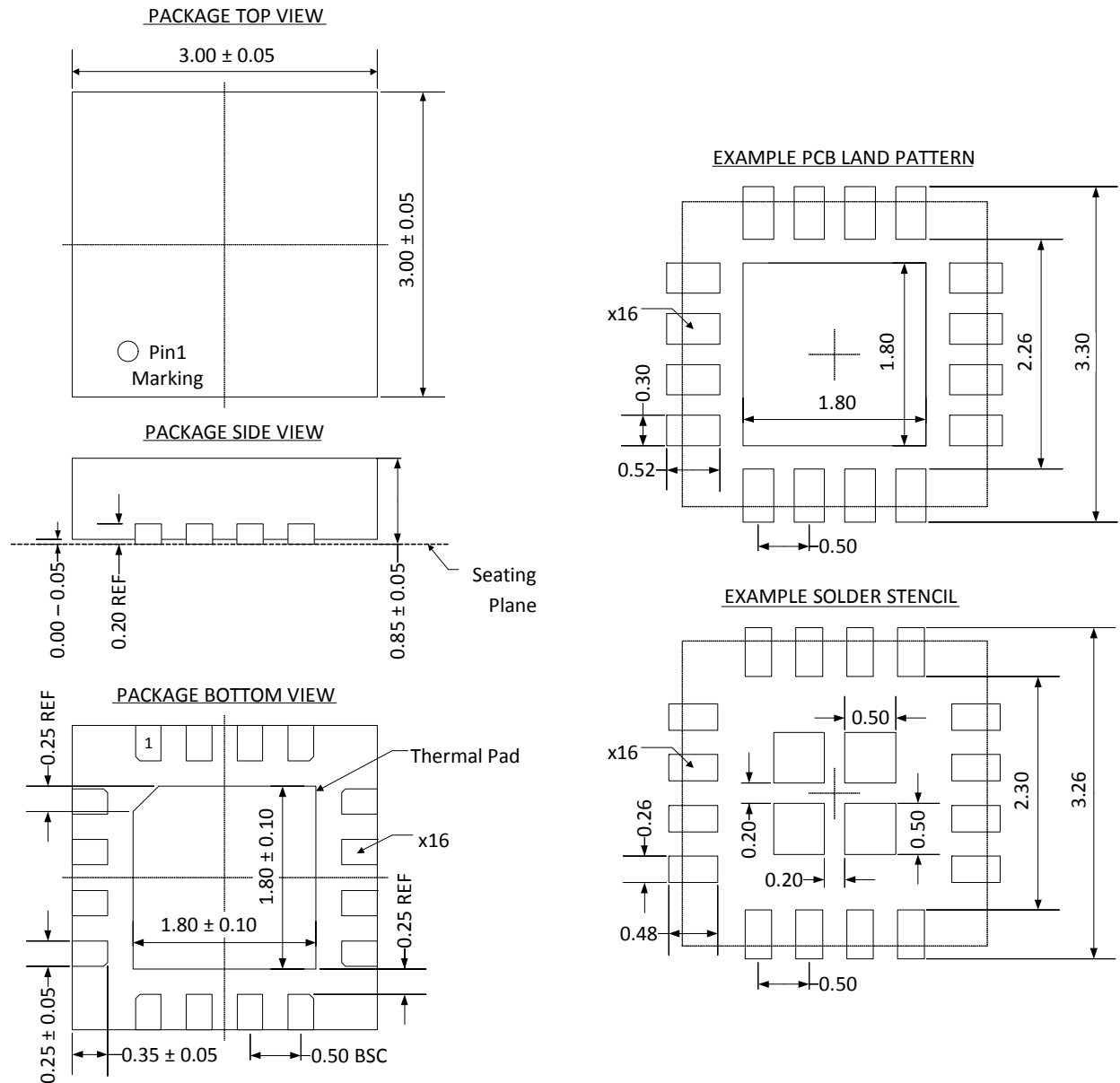
### **6.12.3 0x80 - 0xFF – Alternate RAM**

128 bytes of RAM which may be accessed only in I<sup>2</sup>C interface mode. The data in the RAM is held when using battery power. The upper bit of the RAM address is taken from the XADA field, and the lower 7 bits are taken from the address offset, supporting a total RAM of 256 bytes. The initial values of the RAM locations are undefined.

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## 7. Package Mechanical Information




Figure 32 illustrates the package mechanical information.



**Drawing Notes:**

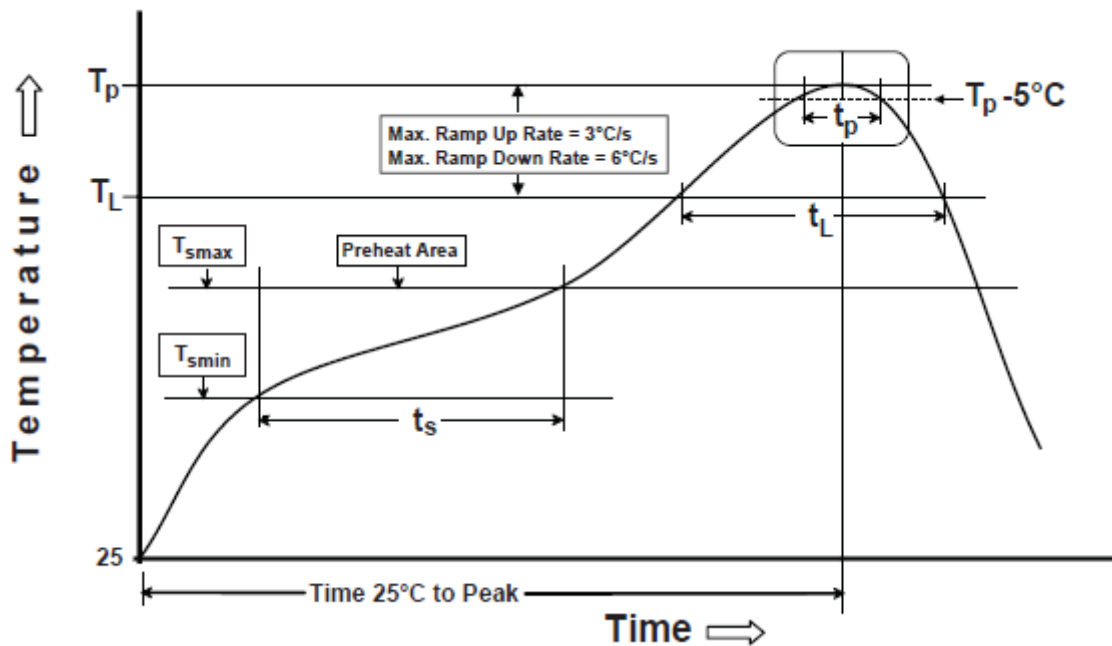
1. All dimensions are in millimeters.
2. These drawings are subject to change without notice.
3. Quad Flat-pack, No-leads (QFN) package configuration.
4. The package thermal pad must be soldered to the board for connectivity and mechanical performance.
5. Customers should contact their board fabricator for minimum solder mask tolerances between signal pads.

**Figure 32. Package Mechanical Diagram**

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## 8. Reflow Profile




Figure 33 illustrates the reflow soldering requirements.



**Figure 33. Reflow Soldering Diagram**

**Table 119: Reflow Soldering Requirements (Pb-free assembly)**




Profile Feature	Requirement
Preheat/Soak Temperature Min ( $T_{smin}$ ) Temperature Max ( $T_{smax}$ ) Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ )	150 °C 200 °C 60-120 seconds
Ramp-up rate ( $T_L$ to $T_p$ )	3 °C/second max.
Liquidous temperature ( $T_L$ ) Time ( $t_L$ ) maintained above $T_L$	217 °C 60-150 seconds
Peak package body temperature ( $T_p$ )	260 °C max.
Time ( $t_p$ ) within 5 °C of $T_p$	30 seconds max.
Ramp-down rate ( $T_p$ to $T_L$ )	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

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## 9. Ordering Information

**Table 120: Ordering Information**




<b>AB08X5 Orderable Part Numbers</b>		<b>Package</b>	<b>Temperature Range</b>	<b>MSL Level<sup>(2)</sup></b>
<b>P/N</b>	<b>Tape and Reel Qty</b>			
AB0805-T3	3000pcs/reel	Pb-Free <sup>(1)</sup> 16-Pin QFN 3 x 3 mm	-40 to +85 °C	1
AB0815-T3	3000pcs/reel			
<p><sup>(1)</sup> Compliant and certified with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in raw homogeneous materials. The package was designed to be soldered at high temperatures (per reflow profile) and can be used in specified lead-free processes.</p> <p><sup>(2)</sup> Moisture Sensitivity Level rating according to the JEDEC J-STD-020D.1 industry standard classifications.</p>				

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