

## 14-stage binary ripple counter with oscillator

## 74HC/HCT4060

## FEATURES

- All active components on chip
- RC or crystal oscillator configuration
- Output capability: standard (except for  $R_{TC}$  and  $C_{TC}$ )
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT4060 are high-speed Si-gate CMOS devices and are pin compatible with "4060" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator

terminals ( $RS$ ,  $R_{TC}$  and  $C_{TC}$ ), ten buffered outputs ( $Q_3$  to  $Q_9$  and  $Q_{11}$  to  $Q_{13}$ ) and an overriding asynchronous master reset ( $MR$ ).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input  $RS$ . In this case keep the other oscillator pins ( $R_{TC}$  and  $C_{TC}$ ) floating.

The counter advances on the negative-going transition of  $RS$ . A HIGH level on  $MR$  resets the counter ( $Q_3$  to  $Q_9$  and  $Q_{11}$  to  $Q_{13} = LOW$ ), independent of other input conditions.

In the HCT version, the  $MR$  input is TTL compatible, but the  $RS$  input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to  $V_{CC}$ .

## QUICK REFERENCE DATA

$GND = 0 V$ ;  $T_{amb} = 25 ^\circ C$ ;  $t_r = t_f = 6 ns$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay RS to $Q_3$	$C_L = 15 pF$ ; $V_{CC} = 5 V$	31	31	ns
	$Q_n$ to $Q_{n+1}$		6	6	ns
$t_{PHL}$	MR to $Q_n$		17	18	ns
$f_{max}$	maximum clock frequency		87	88	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1, 2 and 3	40	40	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 V$
3. For formula on dynamic power dissipation see next pages.

## ORDERING INFORMATION

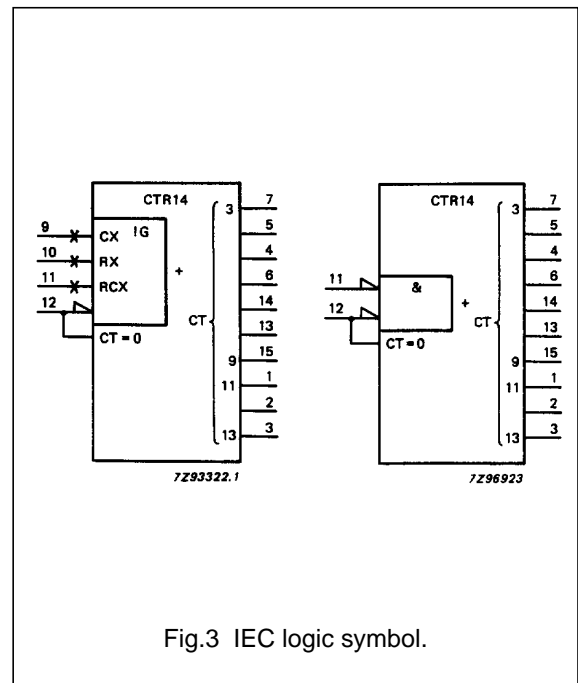
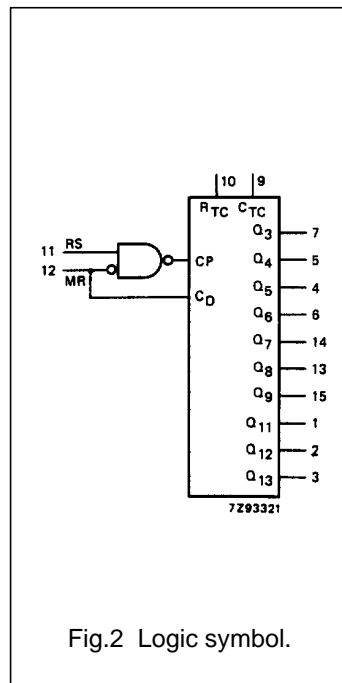
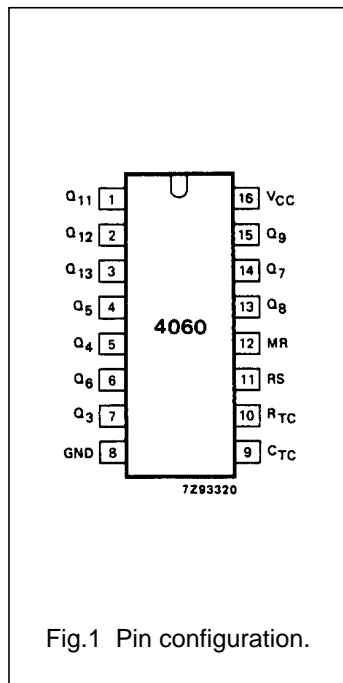
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q <sub>11</sub> to Q <sub>13</sub>	counter outputs
7, 5, 4, 6, 14, 13, 15	Q <sub>3</sub> to Q <sub>9</sub>	counter outputs
8	GND	ground (0 V)
9	C <sub>TC</sub>	external capacitor connection
10	R <sub>TC</sub>	external resistor connection
11	RS	clock input/oscillator pin
12	MR	master reset
16	V <sub>CC</sub>	positive supply voltage



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## DYNAMIC POWER DISSIPATION FOR 74HC

PARAMETER	V <sub>CC</sub> (V)	TYPICAL FORMULA FOR P <sub>D</sub> (μW) (note 1)
total dynamic power	2.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 60 \times V_{CC}$
dissipation when using the on-chip oscillator (P <sub>D</sub> )	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$
	6.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 3\,800 \times V_{CC}$

**Note**

- GND = 0 V; T<sub>amb</sub> = 25 °C

## DYNAMIC POWER DISSIPATION FOR 74HCT

PARAMETER	V <sub>CC</sub> (V)	TYPICAL FORMULA FOR P <sub>D</sub> (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P <sub>D</sub> )	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$

**Notes**

- GND = 0 V; T<sub>amb</sub> = 25 °C
- Where: f<sub>o</sub> = output frequency in MHz  
 f<sub>osc</sub> = oscillator frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 C<sub>L</sub> = output load capacitance in pF  
 C<sub>t</sub> = timing capacitance in pF  
 V<sub>CC</sub> = supply voltage in V

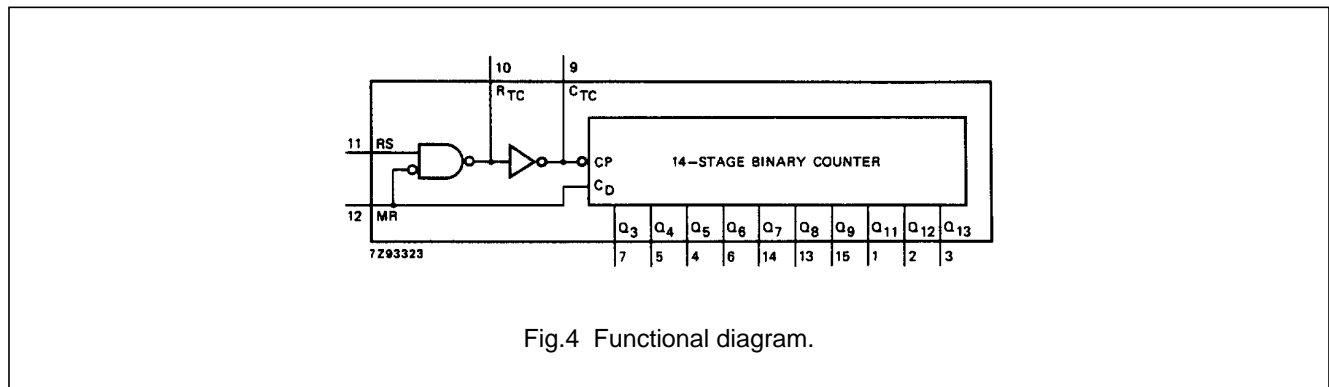


Fig.4 Functional diagram.

## APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits