

Presettable synchronous 4-bit binary up/down counter

74HC/HCT191

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT191 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT191 are asynchronously presettable 4-bit binary up/down counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D₀ to D₃) is loaded into the counter and appears on the outputs when the parallel load (\overline{PL}) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable (\overline{CE}) input. When \overline{CE} is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U/D}$) input signal determines the direction of counting as indicated in the function table. The \overline{CE} input may go LOW when the clock is in either state, however, the LOW-to-HIGH \overline{CE} transition must occur only when the clock is HIGH. Also, the $\overline{U/D}$ input should be changed only when either \overline{CE} or CP is HIGH.

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock (\overline{RC}). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "15" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U/D}$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the \overline{RC} output. When TC is HIGH and \overline{CE} is LOW, the \overline{RC} output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

In Fig.5, each \overline{RC} output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on \overline{CE} inhibits the \overline{RC} output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Fig.6 shows a method of causing state changes to occur simultaneously in all stages. The \overline{RC} outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the \overline{RC} output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Fig.7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the \overline{CE} input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own \overline{CE} signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.

Presettable synchronous 4-bit binary up/down counter

74HC/HCT191

QUICK REFERENCE DATAGND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	22	22	ns
f_{max}	maximum clock frequency		36	36	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	31	33	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

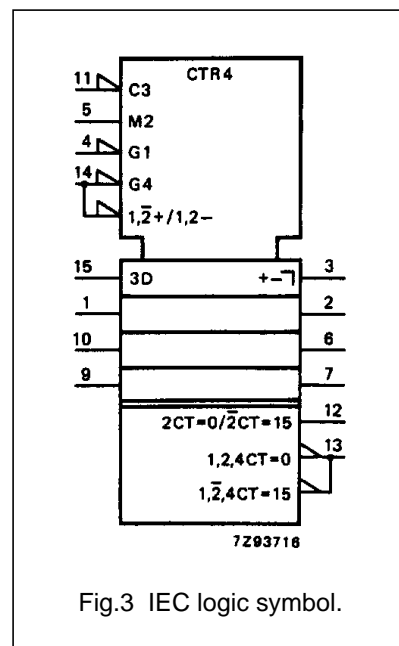
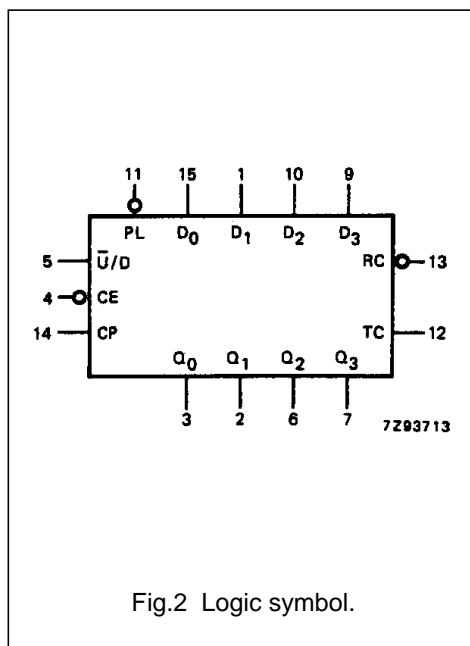
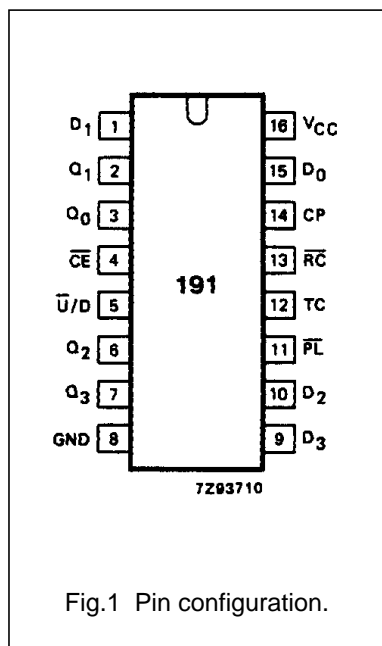
See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Pre-settable synchronous 4-bit binary
up/down counter

74HC/HCT191

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q ₀ to Q ₃	flip-flop outputs
4	\overline{CE}	count enable input (active LOW)
5	$\overline{U/D}$	up/down input
8	GND	ground (0 V)
11	\overline{PL}	parallel load input (active LOW)
12	TC	terminal count output
13	\overline{RC}	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	D ₀ to D ₃	data inputs
16	V _{CC}	positive supply voltage



Pre-settable synchronous 4-bit binary up/down counter

74HC/HCT191

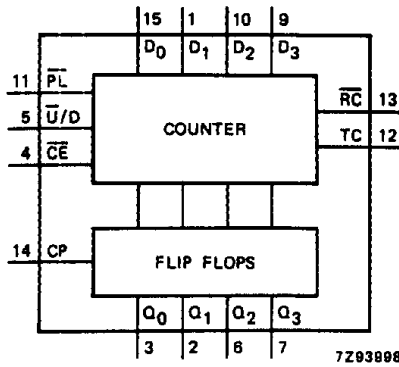


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	\overline{PL}	$\overline{U/D}$	\overline{CE}	CP	D_n	Q_n
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	I	↑	X	count up
count down	H	H	I	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

TC AND RC FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	\overline{CE}	CP	Q_0	Q_1	Q_2	Q_3	TC	\overline{RC}
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L		H	H	H	H		
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L		L	L	L	L		

Notes

- H = HIGH voltage level
 L = LOW voltage level
 I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
 X = don't care
 ↑ = LOW-to-HIGH CP transition
 = one LOW level pulse
 = TC goes LOW on a LOW-to-HIGH CP transition