CYFCT Parameter Measurement Information

features

- **Function, Pinout, Speed, and Drive Compatible With F Logic**
- **All Products Capable of Live Insertion**
- **All Products Meet FCT Logic JEDEC Standard No. 8A**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-Off Disable Feature on All Families**
- **Matched Output Signal Rise and Fall Times**
- **CMOS for Low Power Consumption: Typically 1/3 of the Fastest Advanced Schottky TTL Logic**
- **Inputs and Outputs Interface Directly With TTL, NMOS, and CMOS Devices**
- **Typically 64-mA Sink and 32-mA Source Drive Capability**
- **3-State Outputs on Most Devices**
- **Operational Over the Full Commercial and Military Temperature Ranges (Octal)**
- **Industrial Temperature Range of –40°C to 85°C (16-Bit Family)**
- **Products Available to Latest Revision of MIL-STD-833 Class B Compliance**

functional description

introduction

The CYxxFCT-T logic families acquired from Cypress offer the lowest power solution for the design of high-speed systems. All logic families are TTL compatible, which means that they conform to the industry-standard TTL voltage levels and TTL threshold point of 1.5 V. All inputs have hysteresis. The benefit to the user is increased static and dynamic noise immunity, as well as less sensitivity to noise superimposed on slowly rising or falling inputs.

the original FCT

The outputs of the original (non-Cypress) FCT family swung rail-to-rail, i.e., from V_{OL} = 0.4 V to $V_{OH} = V_{CC} – 0.2$ V. The data sheets specify V_{OH} minimum as 2.4 V when sourcing 15 mA and typical as 4.3 V. The output pullup transistor is a p-channel device. Typical unloaded output signal rise and fall times are 1 ns.

CYxxFCT-T from Cypress

The new, 5-V V_{CC} CYxxFCT-T logic families feature output buffers that use n-channel pullup transistors and controlled rise- and fall-time edge rates. Typical unloaded output signal rise and fall times are 1 ns. The maximum unloaded output high voltage, V_{OH}, is V_{CC} minus the n-channel threshold, V_T. The transistor drain is connected to V_{CC}, so V_T is approximately 1 V. The loaded V_{OH} typically is 3.3 V when sourcing 15 mA with a V_{CC} of 5 V.

The reduced output voltage swing of CYxxFCT-T results in lower crosstalk. The controlled edge rates reduce crosstalk, as well as ground bounce and, in addition, reduce output signal overshoot and undershoot.

These products have no diodes from input pins, output pins, or I/O pins to V_{CC}. This means that they all are capable of being inserted or withdrawn from operating systems without turning off the power.

These logic families produced by Cypress operate from a 5-V power source. The products consist of octals (8-bit data path), either with high-drive (source 32 mA/sink 64 mA) or 25-Ω (output) series resistors, and 16-bit-wide data-path products, either with high-drive or balanced-drive (24-mA source/sink) outputs. Some of these products have bus-hold inputs.

octal CYxxFCT; 5-V, high-drive, and 25-Ω outputs

This high-drive octal family consists of multiple logic functions. The CYxxFCT2-T logic family is identical to the CYxxFCT-T logic family, except that the CYxxFCT2-T devices have the equivalent of a 25-Ω resistor in series with the output. The purpose of the resistor is to provide series damping when driving a transmission line. These products with series damping resistors should be used only when driving lumped (single) loads, and should not be used for driving multiple or distributed loads.

16-bit CYxxFCT; 5-V, high-drive, and balanced-drive outputs

The CYxxFCT16-T logic family is a 16-bit version of the CYxxFCT-T family. The temperature range of the family has been extended to –40°C to 85°C, and V_{CC} tolerance has been loosened to ±10%. Multiple power and grounds have been added to reduce typical ground bounce to below 0.6 V.

The CYxxFCT162-T logic family is a 24-mA balanced-drive version of the CYxxFCT16-T family, and is intended for use in driving transmission lines. The dynamic output current is specified as ±60 mA at 1.5 V, which means that the output impedance is a maximum of 25 Ω.

bus hold

Bus hold is the ability of either an input (data) pin or an I/O pin to retain the last valid logic state (voltage level) after the source driving it either enters the high-impedance state or is removed. Bus hold is available on some 16-bit, 5-V, balanced-drive products. An example part number with bus hold is CY74FCT162H245TPA.

switching characteristics

The circuit shown in Figure 1 is used to load each output for specifying and measuring device propagation delays. It is a de facto industry standard and does not represent device behavior in any application.

The switch is open for all measurements except those having to do with the outputs entering or leaving the high-impedance state as a result of a control input changing.

These conditions are illustrated in Figures 7 and 8. The parameter t_{PZL} is the amount of time it takes an output to go from the high-impedance state to a low state. The parameter t_{PLZ} is the amount of time it takes an output to go from the low state to the high-impedance state; defined as 300 mV above V_{OL}. The parameter t_{PZH} is the amount of time it takes an output to go from a high-impedance state to the high state. The parameter t_{PHZ} is the amount of time it takes an output to go from a high state to the high-impedance state, defined as 300 mV below V_{OH}.

Figures 2–9 illustrate the various propagation delay, setup times, and hold times that are referred to in the switching-characteristics section of the various data sheets. Note that, except for entering the high-impedance state, all measurements are made between the 1.5-V amplitude voltage levels.

Figure 10 shows the input waveform amplitude levels recommended for ac testing of CYFCT-T logic products. Input signals should have maximum rise and fall times of 1 ns and signal swings of 0 to 3 V. Input signals with rise and fall times of 1 ns should be used for testing minimum pulse width or maximum frequency.

When performing ac tests, care must be taken to ensure that the input signals do not return to the transition region due to signal overshoot or undershoot. The load capacitor should be a leaderless chipcap. If this is not possible, keep the leads as short as possible to avoid signal overshoot and undershoot due to lead inductance. The same reasoning applies to the load resistors and power-supply decoupling and filtering capacitors. Solid grounding is required, and a ground plane is recommended.

power specifications

CYxxFCT-T logic devices do not use a substrate bias generator. As a result, the quiescent or standby current typically is a few microamperes when the voltage at the inputs is either less than 0.2 V or greater than V_{CC} – 0.2 V. On the data sheet, this current is described as quiescent power supply current, given the symbol I_{CC}, and specified on a per-IC basis. No inputs are switching, and all outputs are open and, if possible, disabled.

When the input signal transitions between the logic levels, both the p-channel pullup transistor and the n-channel pulldown transistor in the input TTL-to-CMOS translator are partially turned on, which creates a low-impedance path between V_{CC} and ground. On the data sheet, this current is described as "quiescent power supply current (TTL inputs)," given the symbol ΔI_{CC}, and specified on a per-input basis. One input is V_{IN} = 3.4 V, other inputs are at either V_{CC} or 0 V, and all outputs are open and, if possible, disabled.

The dynamic power supply current, given the symbol I_{CCD}, is not measured directly, but is provided so that the user can calculate total current. It is specified in mA per MHz at 50% duty cycle, with one input toggling and one output toggling [enabled but open (unloaded)].

The preceding three currents are specified with the outputs open. The ac CVf current required to charge and discharge parasitic capacitances (e.g., other inputs being driven by the outputs), as well as any dc load currents, must be calculated separately.

Total supply current, I_C, is specified on the data sheet for several different conditions. The inputs are switched between ground and either TTL (3.4 V) or CMOS (V_{CC} – 0.2 V) levels with rise and fall times of 2.5 ns. Slow rise and fall times can cause the dynamic current to increase, because the input signals are within the transition region for longer times. Figure 14 shows a characterization curve of normalized ($I_{CC}/\Delta I_{CC}$) currents versus V_{IN}.

Total supply current can be estimated by using the following formula. This equation implies calculating the current associated with each input and adding them up. The same procedure must be followed to calculate the CVf current required to charge and discharge the load capacitances.

$$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_{cp}/2 + f_n \times N_n)$$

Where:

I_C = Total supply current
I_{CC} = Power supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_{CP} = Clock frequency for registered devices, otherwise 0
f_n = Input signal frequency
N_n = Number of inputs changing at f_n

ESD (electrostatic discharge) precautions

Large electrical fields can damage the thin gate oxides of MOS transistors. Special input protection circuits are used at every input pin of all CYxxFCT-T products to provide protection against ESD. This circuitry has been designed to withstand repeated applications of high voltages without failure or performance degradation. This is accomplished by preventing the high voltage (ESD) from reaching the thin gate oxides of the internal transistors.

Precautions should be taken by persons handling CMOS devices. Individuals should wear a grounded wrist strap or ankle strap when handling these devices.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range to ground potential . . . . . – 0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Static discharge voltage (per MIL-STD-883, Method 3015) . . . . . >2001 V
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

NOTE 1: Unused inputs always must be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

OPERATING RANGE CYxxFCT-T, CYxxFCT2-T

RANGE	PRODUCT SUFFIX	AMBIENT TEMPERATURE	V_{CC}
Industrial	T, AT, BT	–40°C to 85°C	5 V ± 5%
Military†	All	–55°C to 125°C	5 V ± 10%

† T_A is the instant-on case temperature.

OPERATING RANGE

PRODUCT NAME	RANGE	AMBIENT TEMPERATURE	V_{CC}
CYxxFCT16-T	Industrial	–40°C to 85°C	5 V ± 5%

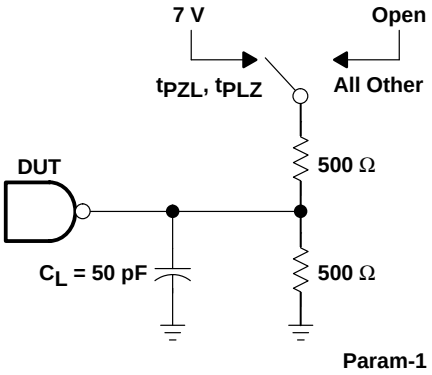

Figure 1. Test Load

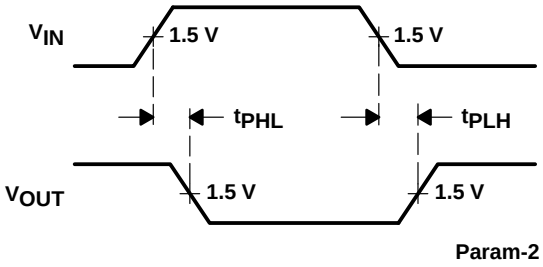

Figure 2. Waveform for Inverting Functions

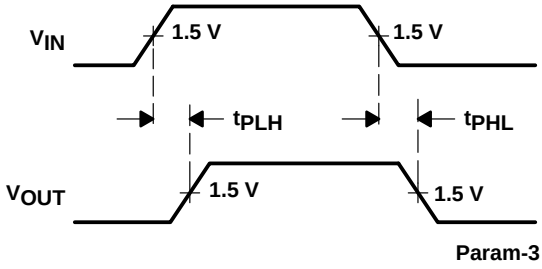

Figure 3. Waveform for Noninverting Functions

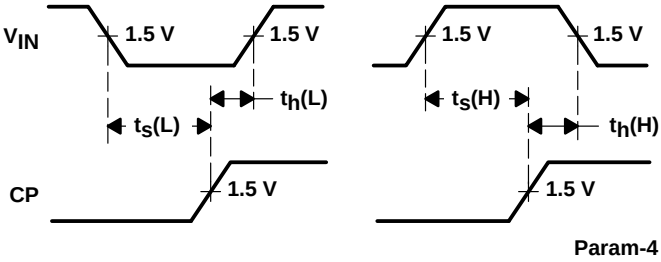

Figure 4. Setup and Hold Times, Rising-Edge Clock

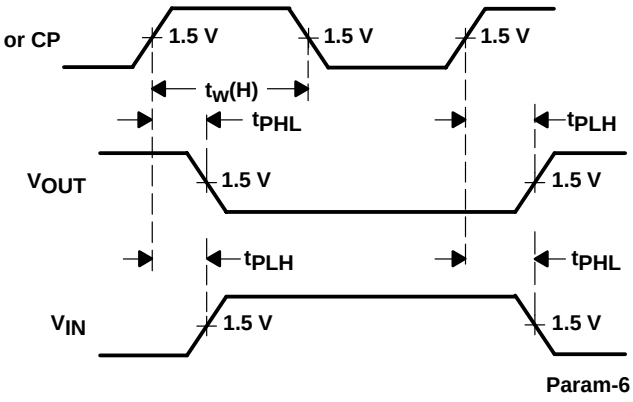

Figure 5. Propagation Delays From Rising-Edge Clock or Enable

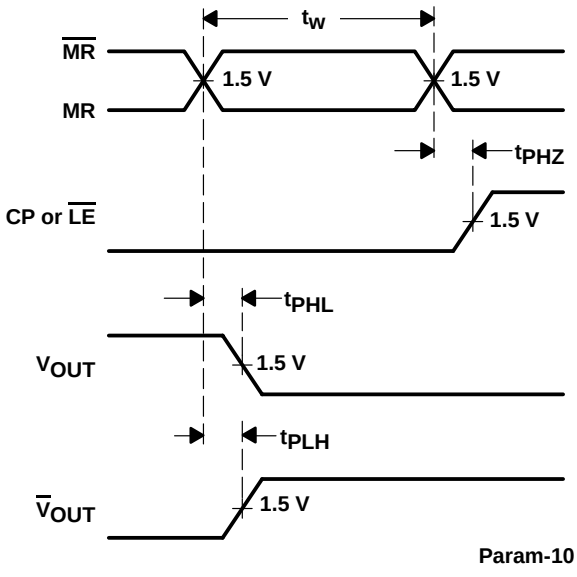

Figure 6. Asynchronous Reset, Active Rising-Edge Clock, or Active Low Enable

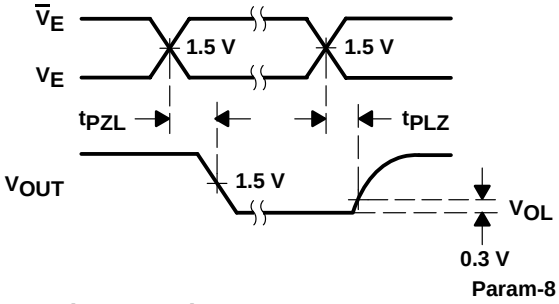

Figure 7. Three-State Output Low Enable and Disable Times

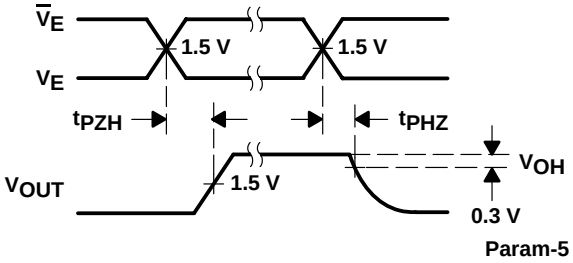

Figure 8. Three-State Output High Enable and Disable Times

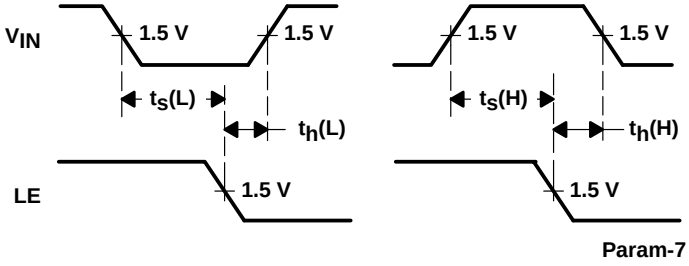

Figure 9. Setup and Hold Times to Active-High Enable or Parallel Load

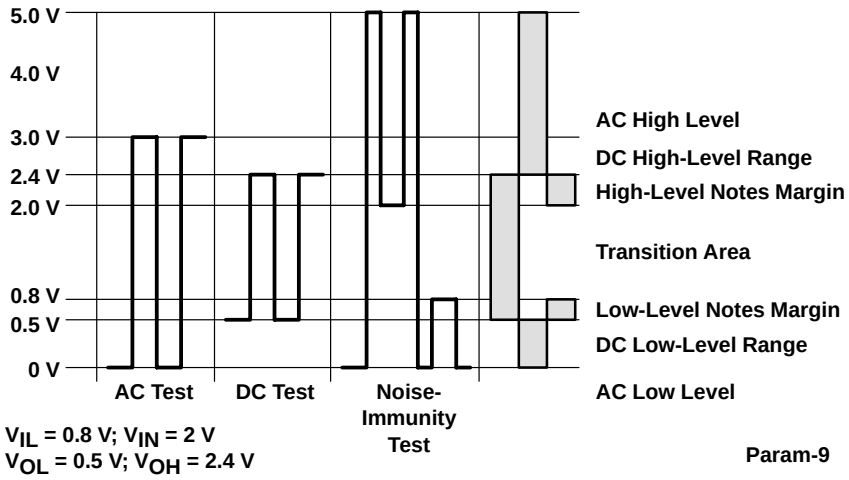

Figure 10. Input Signal Levels

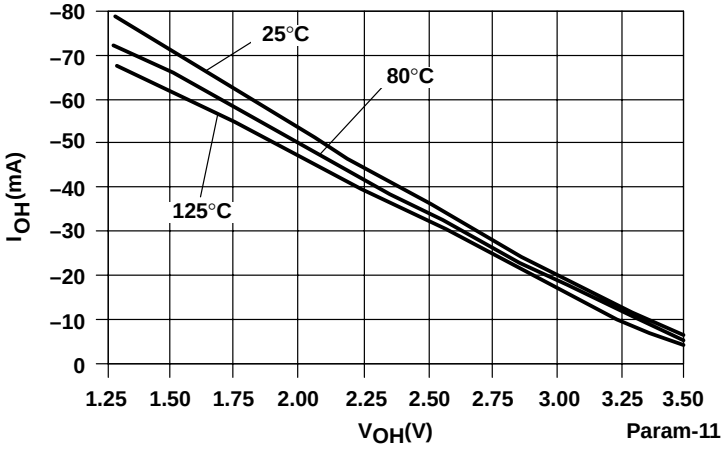

Figure 11. Output Source Current vs Output Voltage

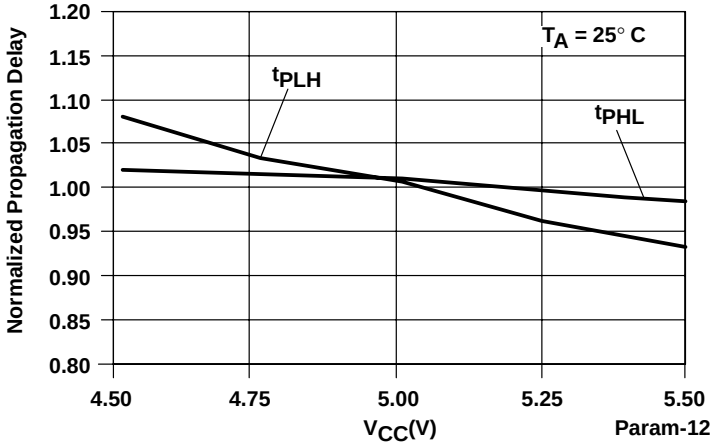

Figure 12. Normalized Propagation Delay vs V_{CC}

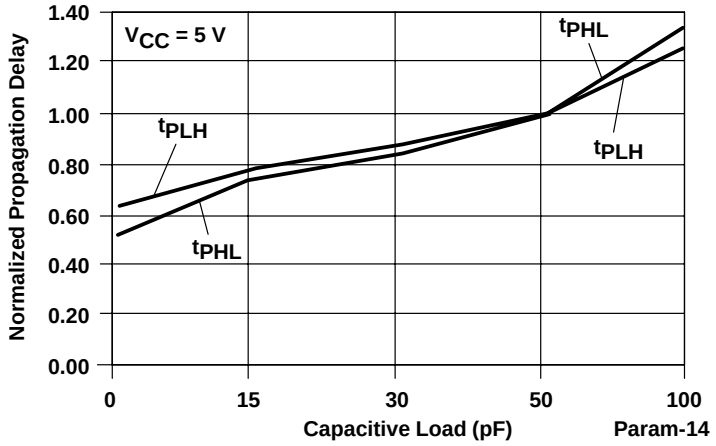

Figure 13. Normalized Propagation Delay vs Output Loading

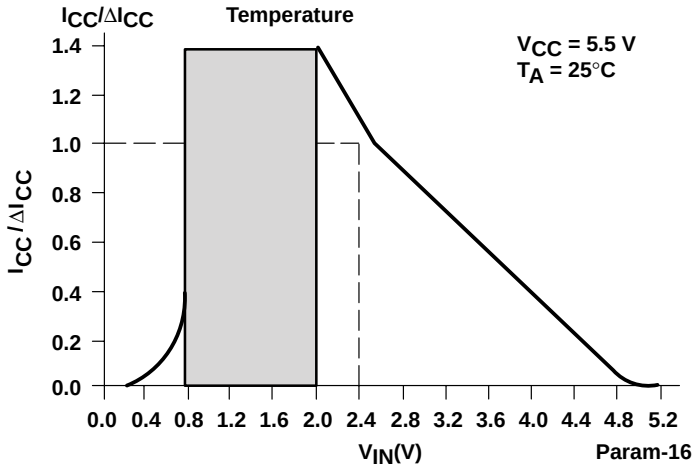

Figure 14. Normalized Current vs Input Voltage

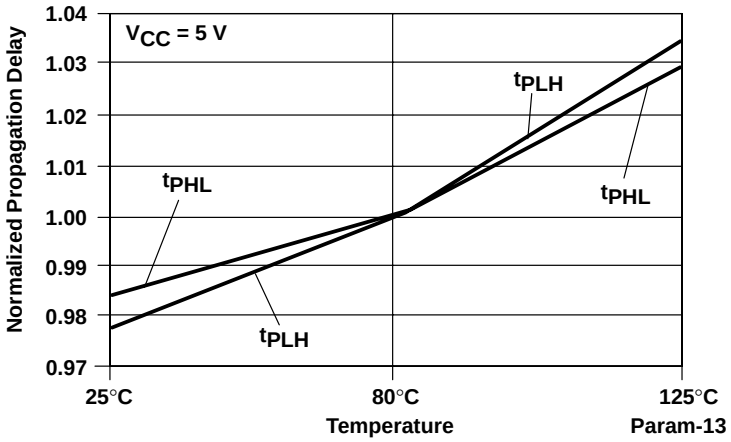

Figure 15. Normalized Propagation Delay vs Temperature

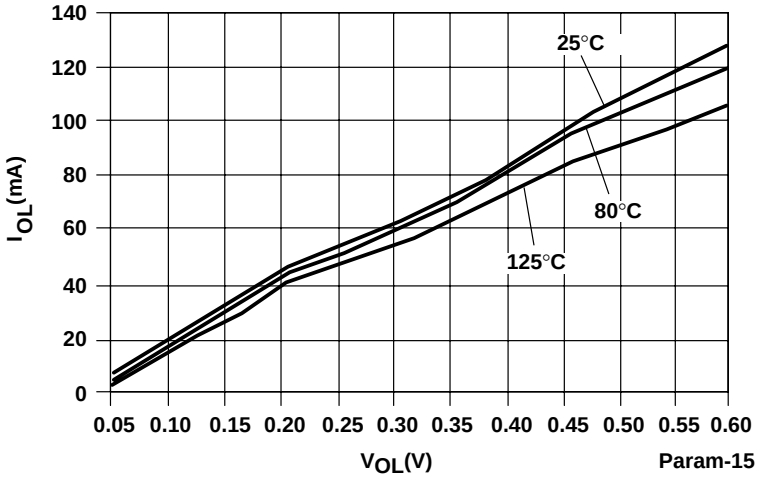

Figure 16. Output Sink Current vs Output Voltage

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265