

# High Precision OPERATIONAL AMPLIFIERS

## FEATURES

- **ULTRA LOW OFFSET VOLTAGE:** 10 $\mu$ V
- **ULTRA LOW DRIFT:**  $\pm 0.1\mu$ V/ $^{\circ}$ C
- **HIGH OPEN-LOOP GAIN:** 134dB
- **HIGH COMMON-MODE REJECTION:** 140dB
- **HIGH POWER SUPPLY REJECTION:** 130dB
- **LOW BIAS CURRENT:** 1nA max
- **WIDE SUPPLY RANGE:**  $\pm 2$ V to  $\pm 18$ V
- **LOW QUIESCENT CURRENT:** 800 $\mu$ A/amplifier
- **SINGLE, DUAL, AND QUAD VERSIONS**
- **REPLACES OP-07, OP-77, OP-177**

## APPLICATIONS

- **TRANSDUCER AMPLIFIER**
- **BRIDGE AMPLIFIER**
- **TEMPERATURE MEASUREMENTS**
- **STRAIN GAGE AMPLIFIER**
- **PRECISION INTEGRATOR**
- **BATTERY POWERED INSTRUMENTS**
- **TEST EQUIPMENT**

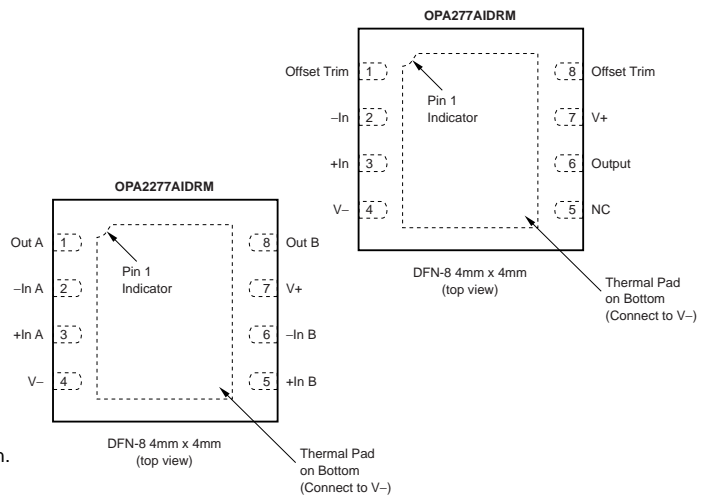
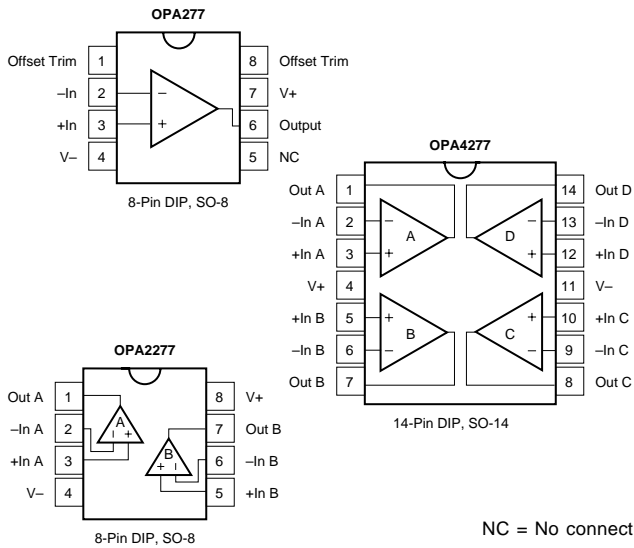
## DESCRIPTION

The OPA277 series precision op amps replace the industry standard OP-177. They offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultra low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection. Single, dual, and quad versions have identical specifications for maximum design flexibility.

OPA277 series op amps operate from  $\pm 2$ V to  $\pm 18$ V supplies with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA277 series is specified for real-world applications; a single limit applies over the  $\pm 5$ V to  $\pm 15$ V supply range. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage ( $\pm 20\mu$ V max) is so low, user adjustment is usually not required. However, the single version (OPA277) provides external trim pins for special applications.

OPA277 op amps are easy to use and free from phase inversion and overload problems found in some other op amps. They are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single (OPA277) and dual (OPA2277) versions are available in DIP-8, SO-8, and DFN-8 (4mm x 4mm) packages. The quad (OPA4277) comes in DIP-14 and SO-14 surface-mount packages. All are fully specified from  $-40^{\circ}$ C to  $+85^{\circ}$ C and operate from  $-55^{\circ}$ C to  $+125^{\circ}$ C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage .....	36V
Input Voltage .....	(V-) -0.7V to (V+) +0.7V
Output Short-Circuit <sup>(2)</sup> .....	Continuous
Operating Temperature .....	-55°C to +125°C
Storage Temperature .....	-55°C to +125°C
Junction Temperature .....	150°C
Lead Temperature (soldering, 10s) .....	300°C
ESD Rating (Human Body Model) .....	2000V
(Machine Model) .....	100V

NOTE: (1) Stresses above these rating may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

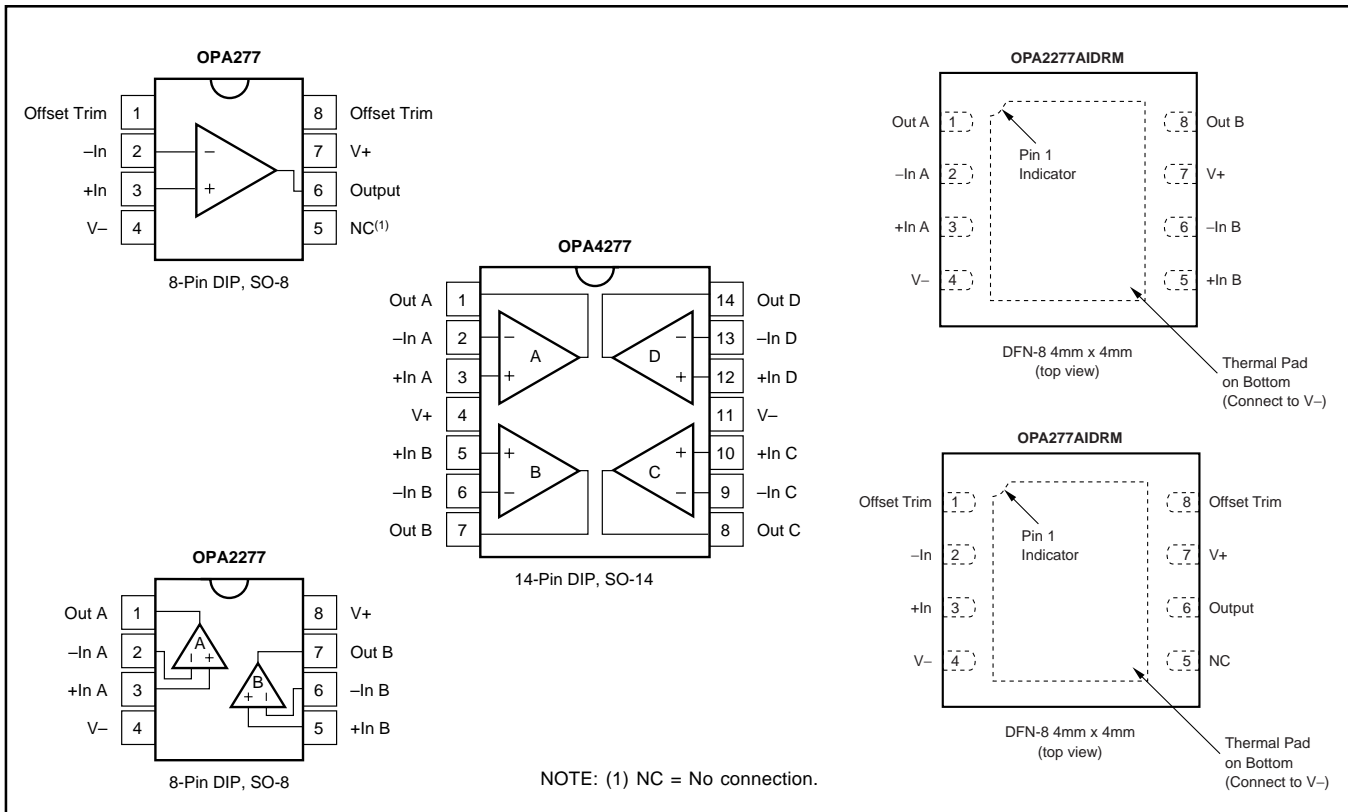
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	OFFSET VOLTAGE max, $\mu\text{V}$	OFFSET VOLTAGE DRIFT max, $\mu\text{V}/^\circ\text{C}$	PACKAGE-LEAD
<b>Single</b> OPA277PA OPA277P OPA277UA OPA277U OPA277AIDRM	$\pm 50$ $\pm 20$ $\pm 50$ $\pm 20$ $\pm 100$	$\pm 1$ $\pm 0.15$ $\pm 1$ $\pm 0.15$ $\pm 1$	DIP-8 DIP-8 SO-8 Surface Mount SO-8 Surface Mount DFN-8 (4mm x 4mm)
<b>Dual</b> OPA2277PA OPA2277P OPA2277UA OPA2277U OPA2277AIDRM	$\pm 50$ $\pm 25$ $\pm 50$ $\pm 25$ $\pm 100$	$\pm 1$ $\pm 0.25$ $\pm 1$ $\pm 0.25$ $\pm 1$	DIP-8 DIP-8 SO-8 Surface Mount SO-8 Surface Mount DFN-8 (4mm x 4mm)
<b>Quad</b> OPA4277PA OPA4277UA	$\pm 50$ $\pm 50$	$\pm 1$ $\pm 1$	DIP-14 SO-14 Surface Mount

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet or visit the TI web site at [www.ti.com](http://www.ti.com).

## PIN DESCRIPTIONS



# ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ to $V_S = \pm 15V$

At  $T_A = +25^\circ C$ , and  $R_L = 2k\Omega$ , unless otherwise noted.

**Boldface** limits apply over the specified temperature range,  $-40^\circ C$  to  $+85^\circ C$ .

PARAMETER	CONDITION	OPA277P, U OPA2277P, U			OPA277PA, UA OPA2277PA, UA OPA4277PA, UA			OPA277AIDRM, OPA2277AIDRM			UNITS		
		MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX			
<b>OFFSET VOLTAGE</b> Input Offset Voltage: $V_{OS}$ OPA277P, U (high grade, single) OPA2277P, U (high grade, dual) All PA, UA, Versions AIDRM Versions  <b>Input Offset Voltage Over Temperature</b> OPA277P, U (high grade, single) OPA2277P, U (high grade, dual) All PA, UA, Versions AIDRM Versions  <b>Input Offset Voltage Drift</b> $dV_{OS}/dT$ OPA277P, U (high grade, single) OPA2277P, U (high grade, dual) All PA, UA, AIDRM Versions  Input Offset Voltage: (all models) vs Time vs Power Supply PSRR $T_A = -40^\circ C$ to $+85^\circ C$ Channel Separation (dual, quad)	$T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$  $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$  $V_S = \pm 2V$ to $\pm 18V$ $T_A = -40^\circ C$ to $+85^\circ C$ $V_S = \pm 2V$ to $\pm 18V$ dc		$\pm 10$	$\pm 20$							$\mu V$		
			$\pm 10$	$\pm 25$		$\pm 20$	$\pm 50$		$\pm 35$	$\pm 100$		$\mu V$	
					$\pm 30$			$\pm 100$			$\pm 165$		$\mu V$
				$\pm 0.1$	$\pm 0.15$								$\mu V/^\circ C$
			$\pm 0.1$	$\pm 0.25$		$\pm 0.15$	$\pm 1$		$\pm 0.15$	$\pm 1$		$\mu V/^\circ C$	
			0.2			*			*			$\mu V/mo$	
			$\pm 0.3$	$\pm 0.5$		*	$\pm 1$		*	$\pm 1$		$\mu V/V$	
				$\pm 0.5$		*	$\pm 1$		*	$\pm 1$		$\mu V/V$	
			0.1			*			*			$\mu V/V$	
<b>INPUT BIAS CURRENT</b> Input Bias Current $I_B$ $T_A = -40^\circ C$ to $+85^\circ C$ Input Offset Current $I_{OS}$ $T_A = -40^\circ C$ to $+85^\circ C$			$\pm 0.5$	$\pm 1$		*	$\pm 2.8$			$\pm 2.8$		nA	
				$\pm 2$			$\pm 4$			$\pm 4$		nA	
			$\pm 0.5$	$\pm 1$		*	$\pm 2.8$			$\pm 2.8$		nA	
				$\pm 2$			$\pm 4$			$\pm 4$		nA	
<b>NOISE</b> Input Voltage Noise, $f = 0.1$ to $10Hz$  Input Voltage Noise Density, $f = 10Hz$ $e_n$ $f = 100Hz$ $f = 1kHz$ $f = 10kHz$  Current Noise Density, $f = 1kHz$ $i_n$			0.22			*			*			$\mu V_{PP}$	
				0.035			*		*			$\mu V_{rms}$	
				12			*		*			$nV/\sqrt{Hz}$	
				8			*		*			$nV/\sqrt{Hz}$	
				8			*		*			$nV/\sqrt{Hz}$	
				8			*		*			$nV/\sqrt{Hz}$	
			0.2			*		*				$pA/\sqrt{Hz}$	
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range $V_{CM}$ Common-Mode Rejection CMRR $T_A = -40^\circ C$ to $+85^\circ C$		$(V-) + 2$		$(V+) - 2$	*		*	*		*		V	
		130	140		115	*		115	*			dB	
		<b>128</b>			<b>115</b>			<b>115</b>				<b>dB</b>	
<b>INPUT IMPEDANCE</b> Differential Common-Mode			100    3			*			*			M $\Omega$    pF	
		$V_{CM} = (V-) + 2V$ to $(V+) - 2V$	250    3			*			*			G $\Omega$    pF	
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain $A_{OL}$  $T_A = -40^\circ C$ to $+85^\circ C$		$V_O = (V-) + 0.5V$ to $(V+) - 1.2V$ , $R_L = 10k\Omega$		140		*			*			dB	
		$V_O = (V-) + 1.5V$ to $(V+) - 1.5V$ , $R_L = 2k\Omega$	126	134		*	*		*	*		dB	
		$V_O = (V-) + 1.5V$ to $(V+) - 1.5V$ , $R_L = 2k\Omega$	126			*			*			<b>dB</b>	
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product GBW Slew Rate SR Settling Time, 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise THD+N			1			*			*			MHz	
			0.8			*			*			V/ $\mu s$	
		$V_S = \pm 15V$ , $G = 1$ , 10V Step	14			*			*			$\mu s$	
		$V_S = \pm 15V$ , $G = 1$ , 10V Step	16			*			*			$\mu s$	
		$V_{IN} \cdot G = V_S$	3			*			*			$\mu s$	
		1kHz, $G = 1$ , $V_O = 3.5V_{rms}$	0.002			*			*			%	

\* Specifications same as OPA277P, U.

NOTE: (1)  $V_S = \pm 15V$ .

# ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ to $V_S = \pm 15V$ (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.

**Boldface** limits apply over the specified temperature range,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

PARAMETER	CONDITION	OPA277P, U OPA2277P, U			OPA277PA, UA OPA2277PA, UA OPA4277PA, UA			OPA277AIDRM, OPA2277AIDRM			UNITS
		MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
<b>OUTPUT</b> Voltage Output $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$  $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Short-Circuit Current Capacitive Load Drive	$V_O$   $I_{SC}$ $C_{LOAD}$	$R_L = 10\text{k}\Omega$									V
		$R_L = 10\text{k}\Omega$									V
		$R_L = 2\text{k}\Omega$									V
		$R_L = 2\text{k}\Omega$									V
			$\pm 35$			*			*		mA
		See Typical Curve					*		*		
<b>POWER SUPPLY</b> Specified Voltage Range Operating Voltage Range Quiescent Current (per amplifier) $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$V_S$  $I_Q$										V
											V
		$I_O = 0$		$\pm 790$	$\pm 825$		*	*	*	*	$\mu\text{A}$
		$I_O = 0$			<b><math>\pm 900</math></b>			*		*	$\mu\text{A}$
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Range Thermal Resistance SO-8 Surface-Mount DIP-8 DIP-14 SO-14 Surface-Mount DFN-8 <sup>(2)</sup>	$\theta_{JA}$										$^\circ\text{C}$
											$^\circ\text{C}$
											$^\circ\text{C}$
											$^\circ\text{C}/\text{W}$
								*			$^\circ\text{C}/\text{W}$
								*			$^\circ\text{C}/\text{W}$
								*			$^\circ\text{C}/\text{W}$
											$^\circ\text{C}/\text{W}$
								45		$^\circ\text{C}/\text{W}$	

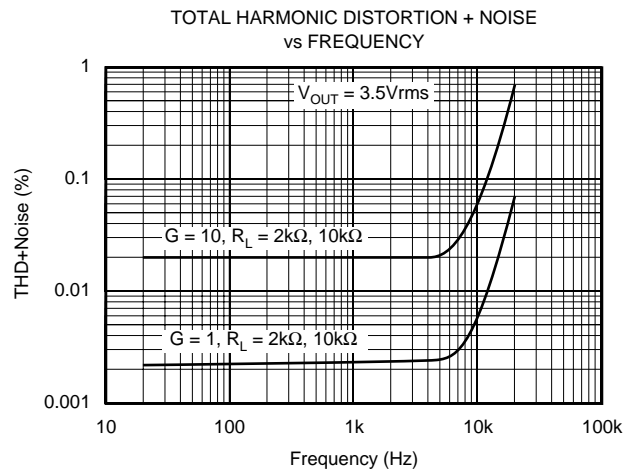
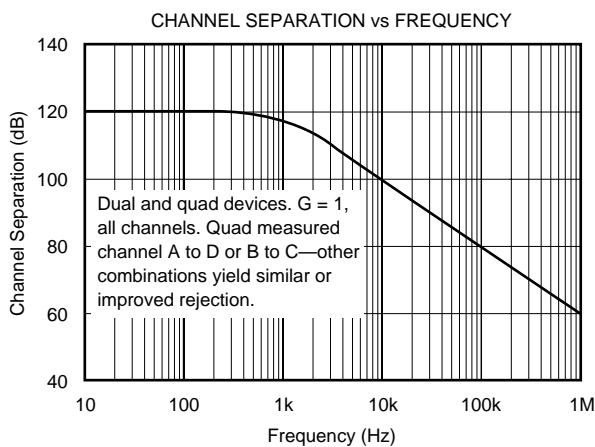
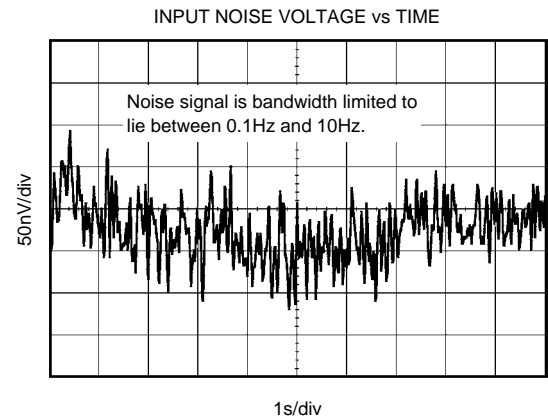
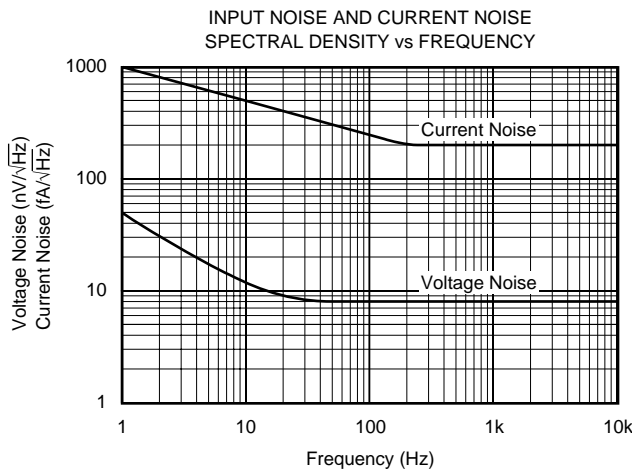
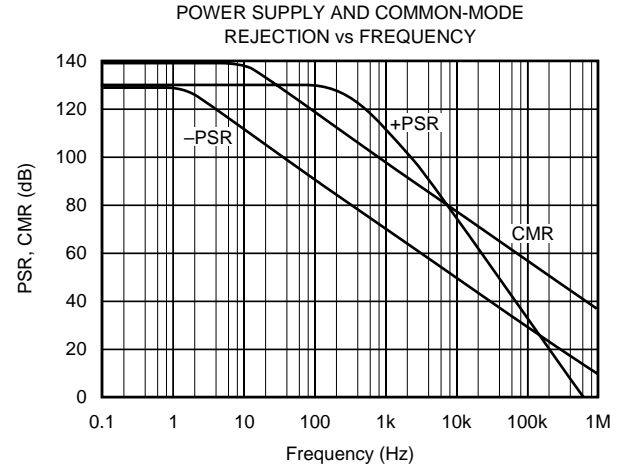
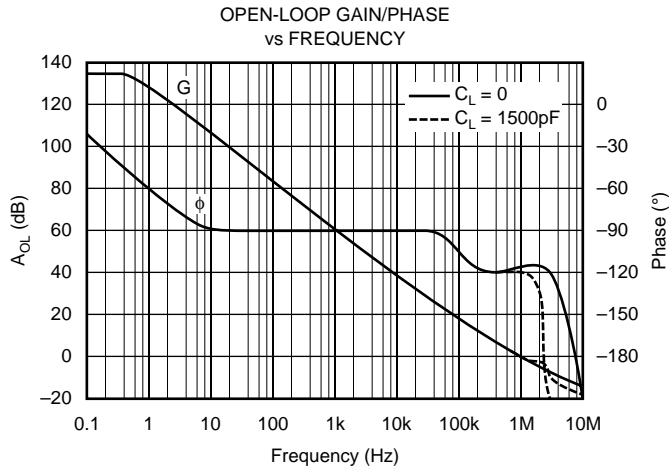
\* Specifications same as OPA277P, U.

NOTES: (1)  $V_S = \pm 15V$ .

(2) Thermal pad soldered to printed circuit board (PCB).

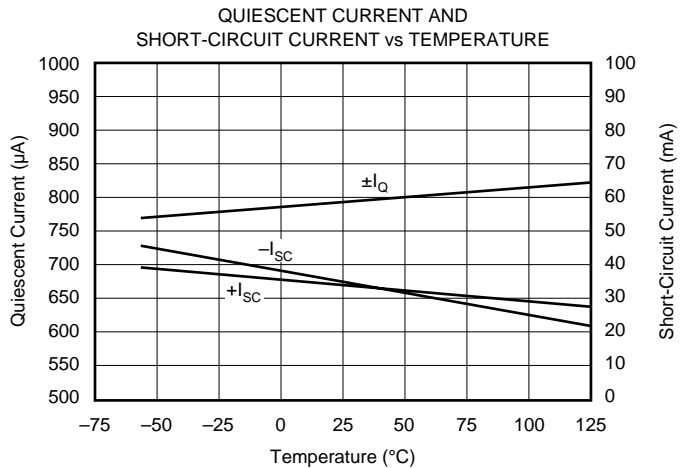
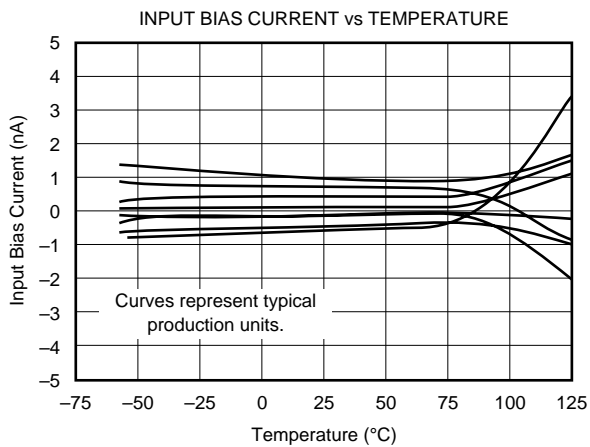
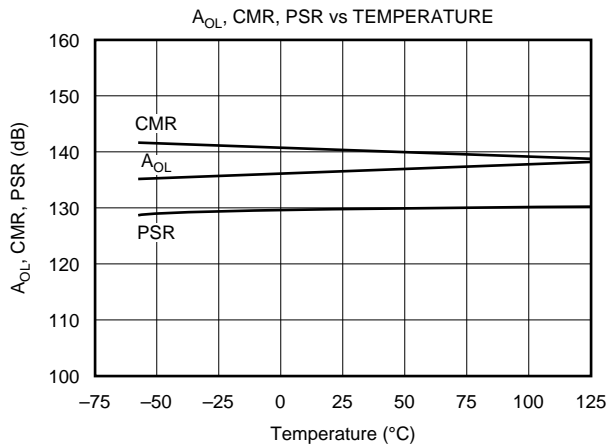
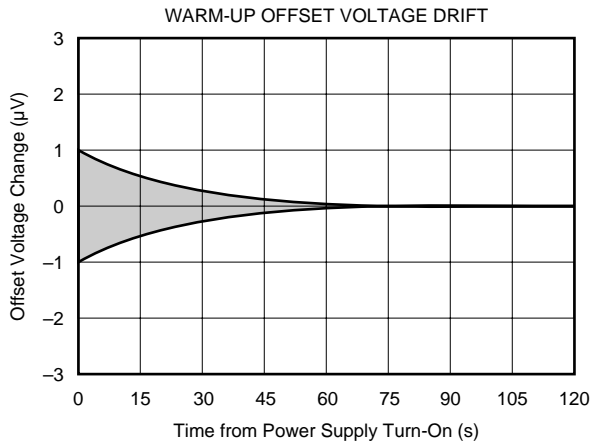
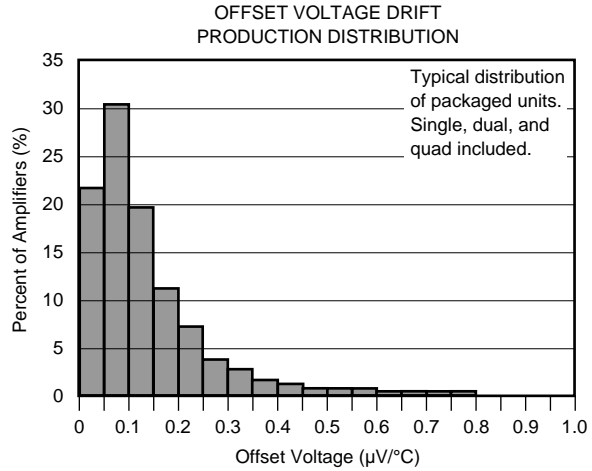
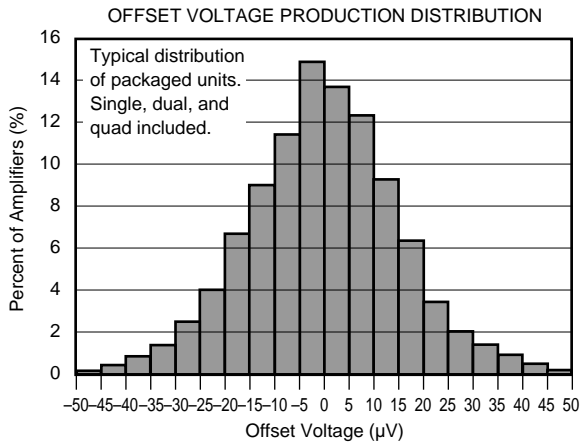
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



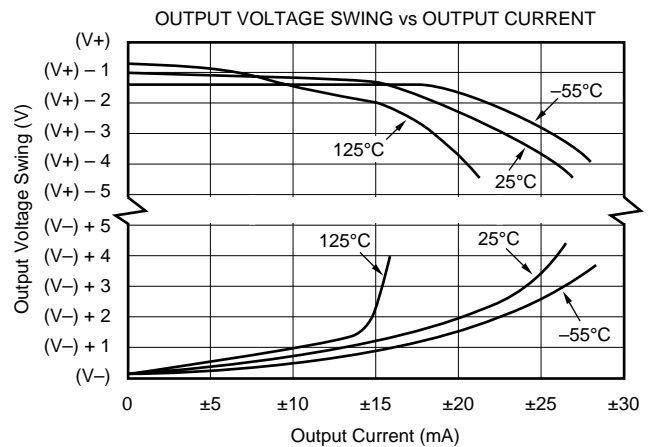
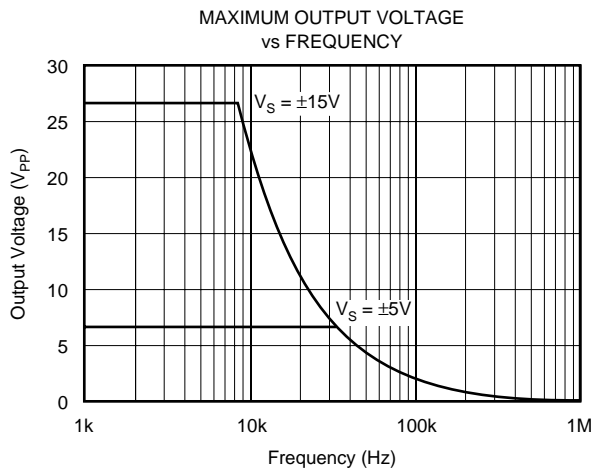
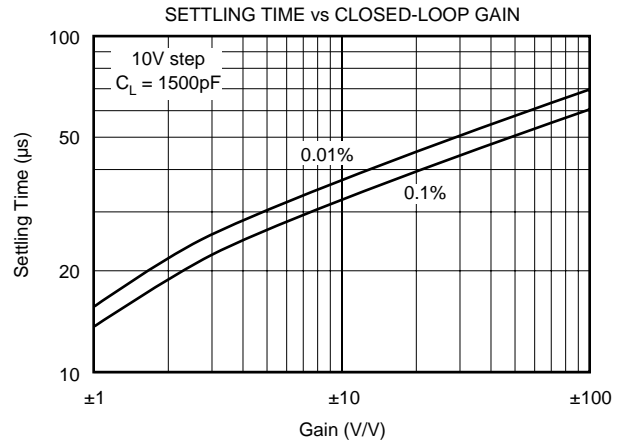
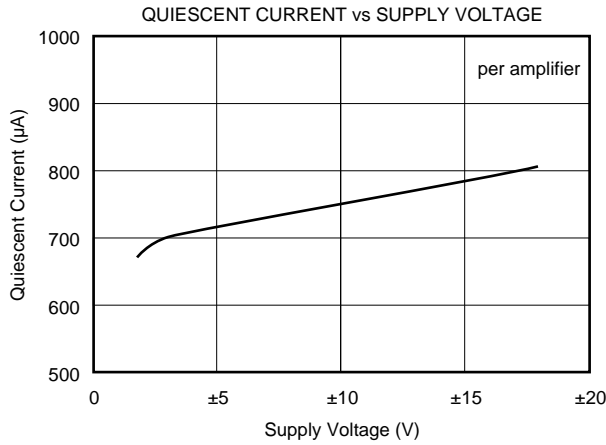
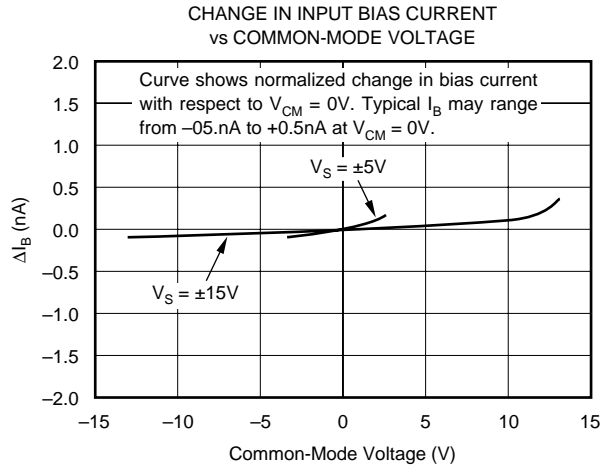
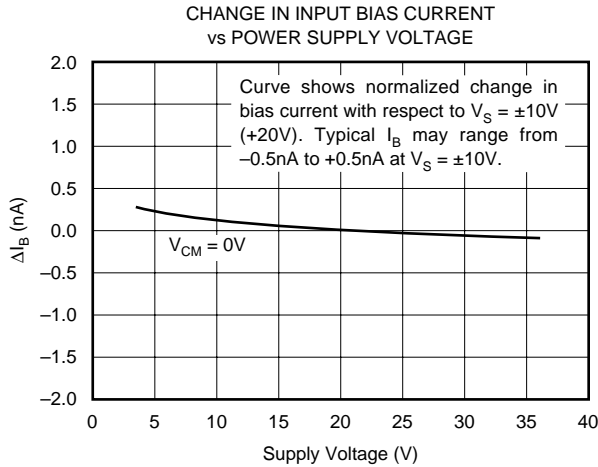
# TYPICAL CHARACTERISTICS (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



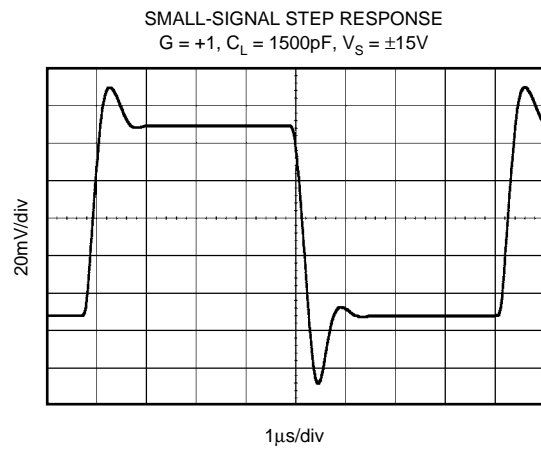
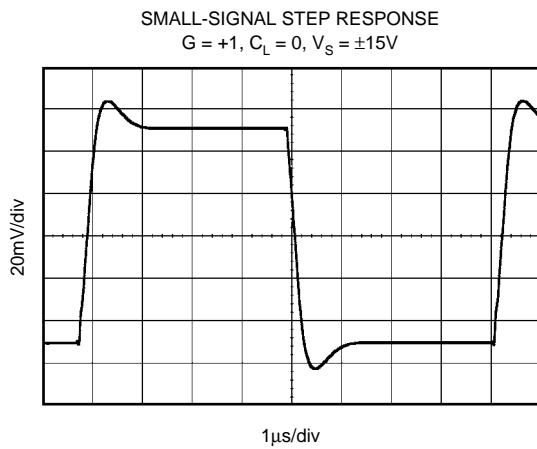
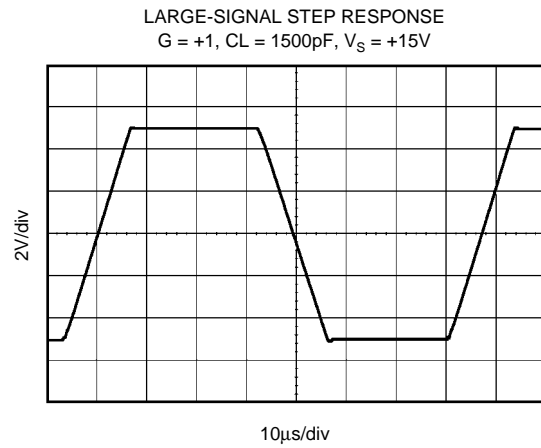
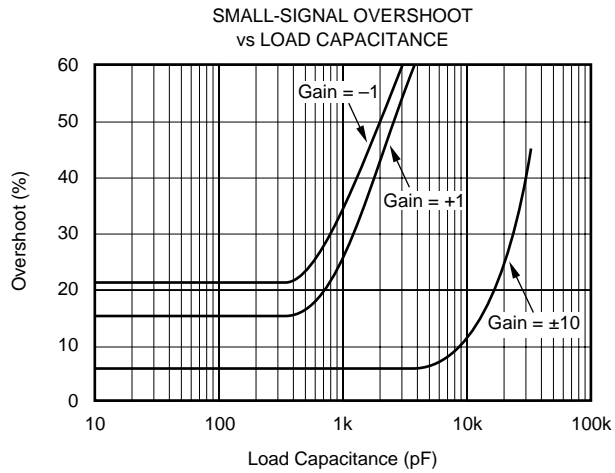
# TYPICAL CHARACTERISTICS (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# APPLICATIONS INFORMATION

The OPA277 series is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases 0.1µF capacitors are adequate.

The OPA277 series has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions should be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can degrade the ultimate performance of the OPA277 series. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield op amp and input circuitry from air currents such as cooling fans.

## OPERATING VOLTAGE

OPA277 series op amp operate from ±2V to ±18V supplies with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA277 series is specified for real-world applications; a single limit applies over the ±5V to ±15V supply range. This allows a customer operating at  $V_S = \pm 10V$  to have the same assured performance as a customer using ±15V supplies. In addition, key parameters are assured over the specified temperature range, -40°C to +85°C. Most behavior remains unchanged through the full operating voltage range (±2V to ±18V). Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

## OFFSET VOLTAGE ADJUSTMENT

The OPA277 series is laser-trimmed for very low offset voltage and drift so most circuits will not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. Offset voltage can be adjusted by

connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce additional temperature drift.

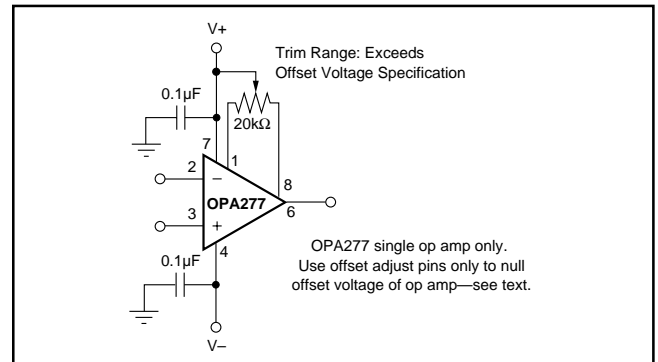


FIGURE 1. OPA277 Offset Voltage Trim Circuit.

## INPUT PROTECTION

The inputs of the OPA277 series are protected with 1kΩ series input resistors and diode clamps. The inputs can withstand ±30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are over-driven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

## INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA277 series is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor as is often done with other op amps (Figure 2). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

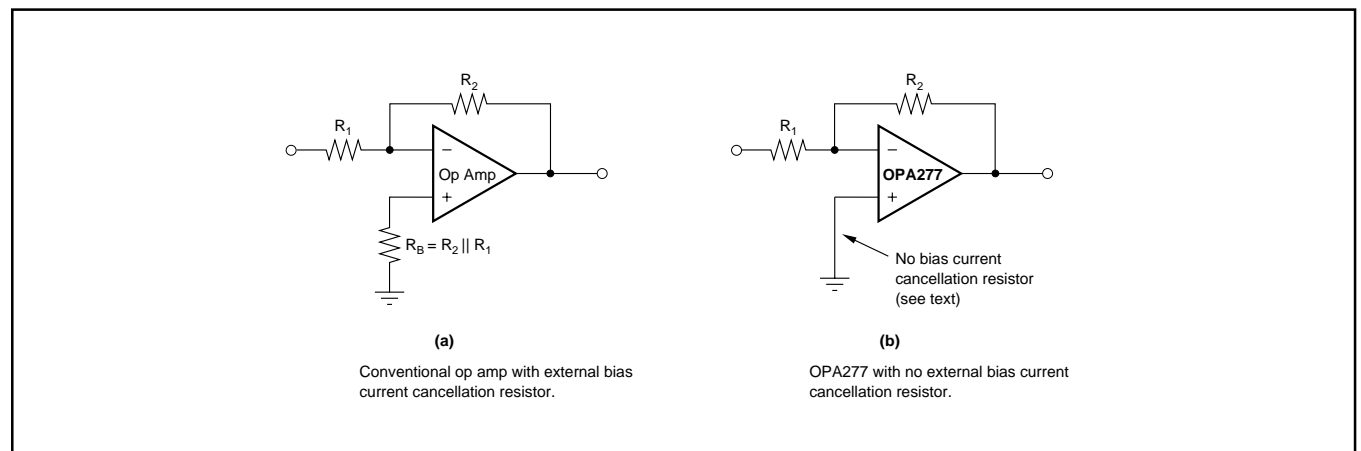


FIGURE 2. Input Bias Current Cancellation.

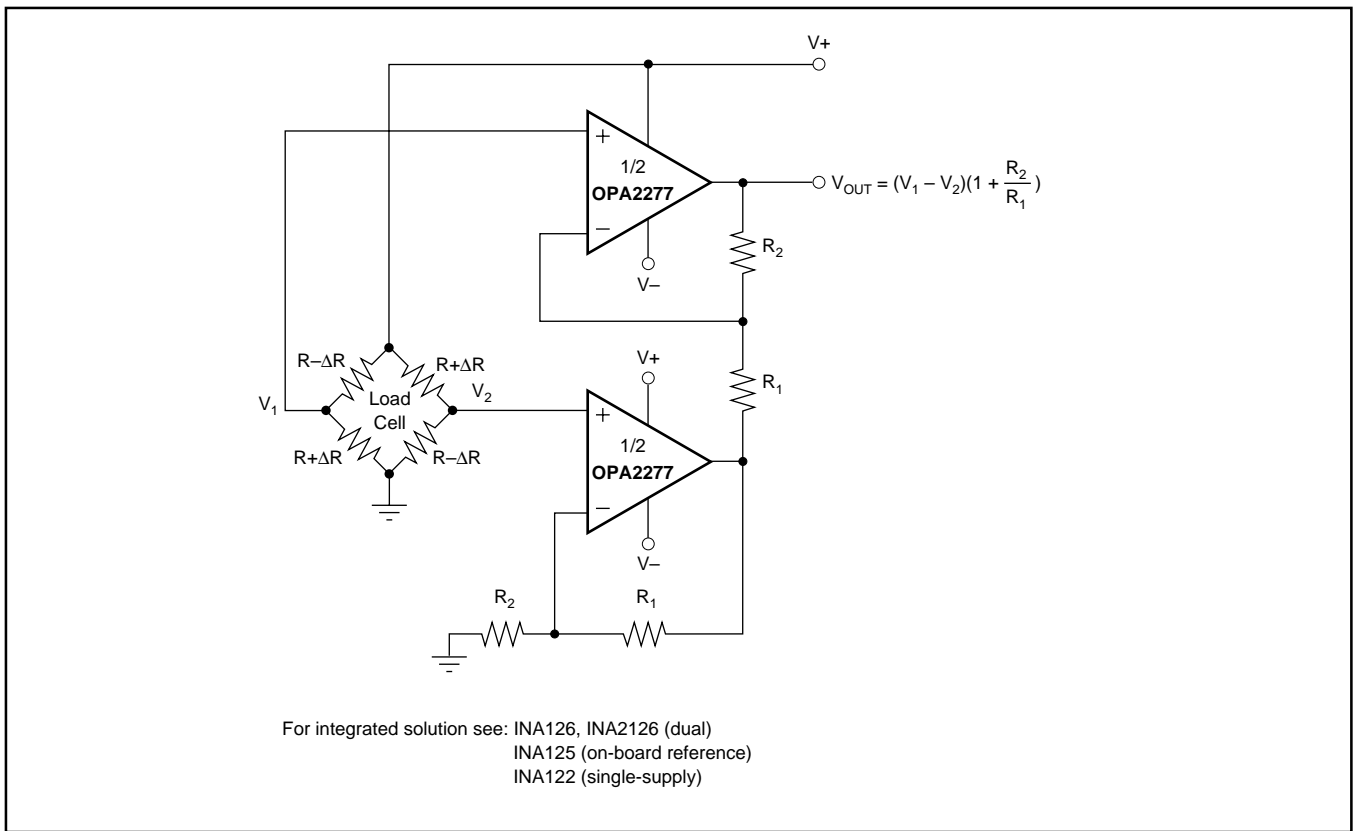


FIGURE 3. Load Cell Amplifier.

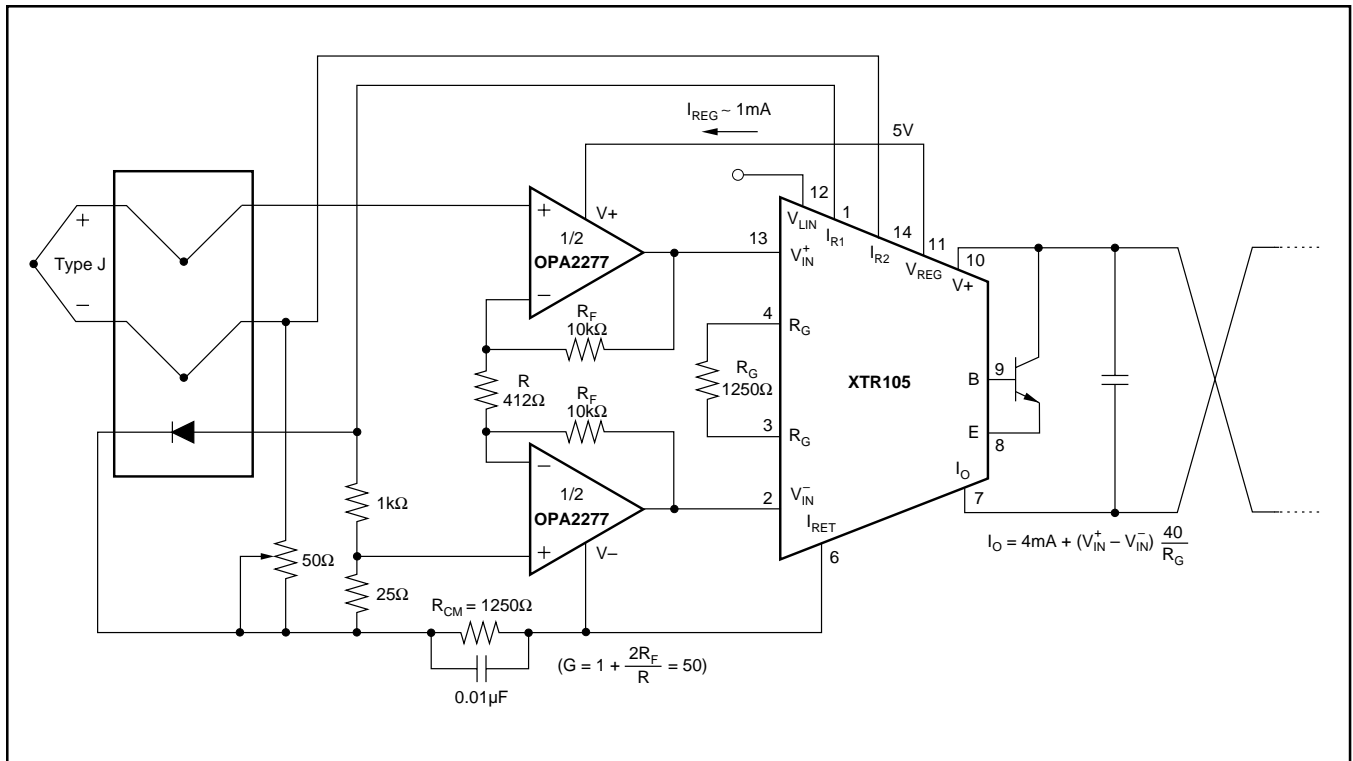


FIGURE 4. Thermocouple Low Offset, Low Drift Loop Measurement with Diode Cold Junction Compensation.

## DFN PACKAGE

The OPA277 series uses the 8-lead DFN (also known as SON), which is a QFN package with contacts on only two sides of the package bottom. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at [www.ti.com](http://www.ti.com).

**The exposed leadframe die pad on the bottom of the package should be connected to V–.**

## LAYOUT GUIDELINES

The leadframe die pad should be soldered to a thermal pad on the PCB. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad **must** be soldered to the PCB to provide structural integrity and long-term reliability.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
OPA2277AIDRMR	ACTIVE	SON	DRM	8	3000	TBD	Call TI	Call TI
OPA2277AIDRMT	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2277AIDRMTG4	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2277P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277AIDRMR	ACTIVE	SON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMRG4	ACTIVE	SON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMT	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMTG4	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
OPA277U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA277UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4277PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4277UA	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UA/2K5	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UA/2K5E4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UAE4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UAG4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

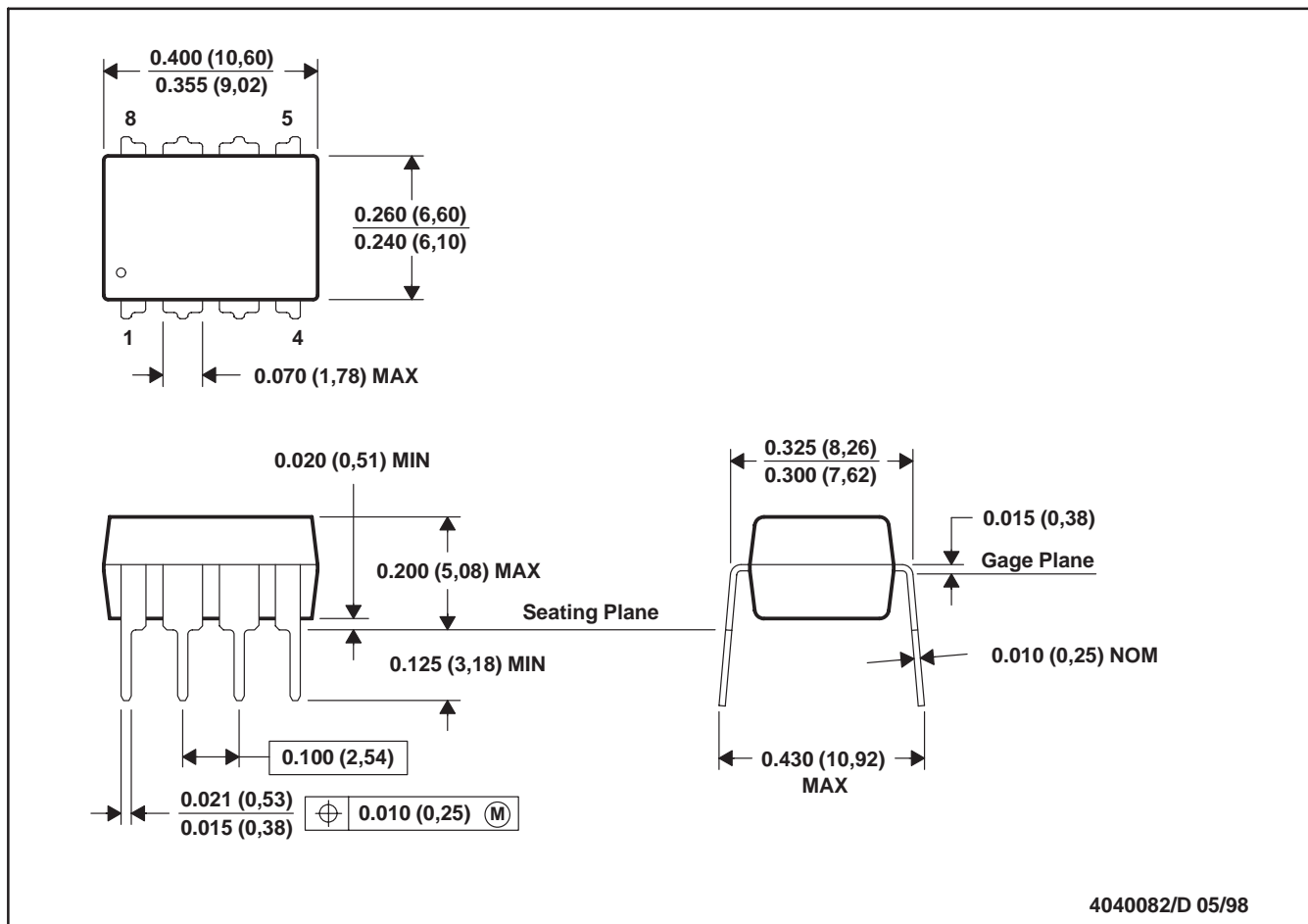
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is

provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

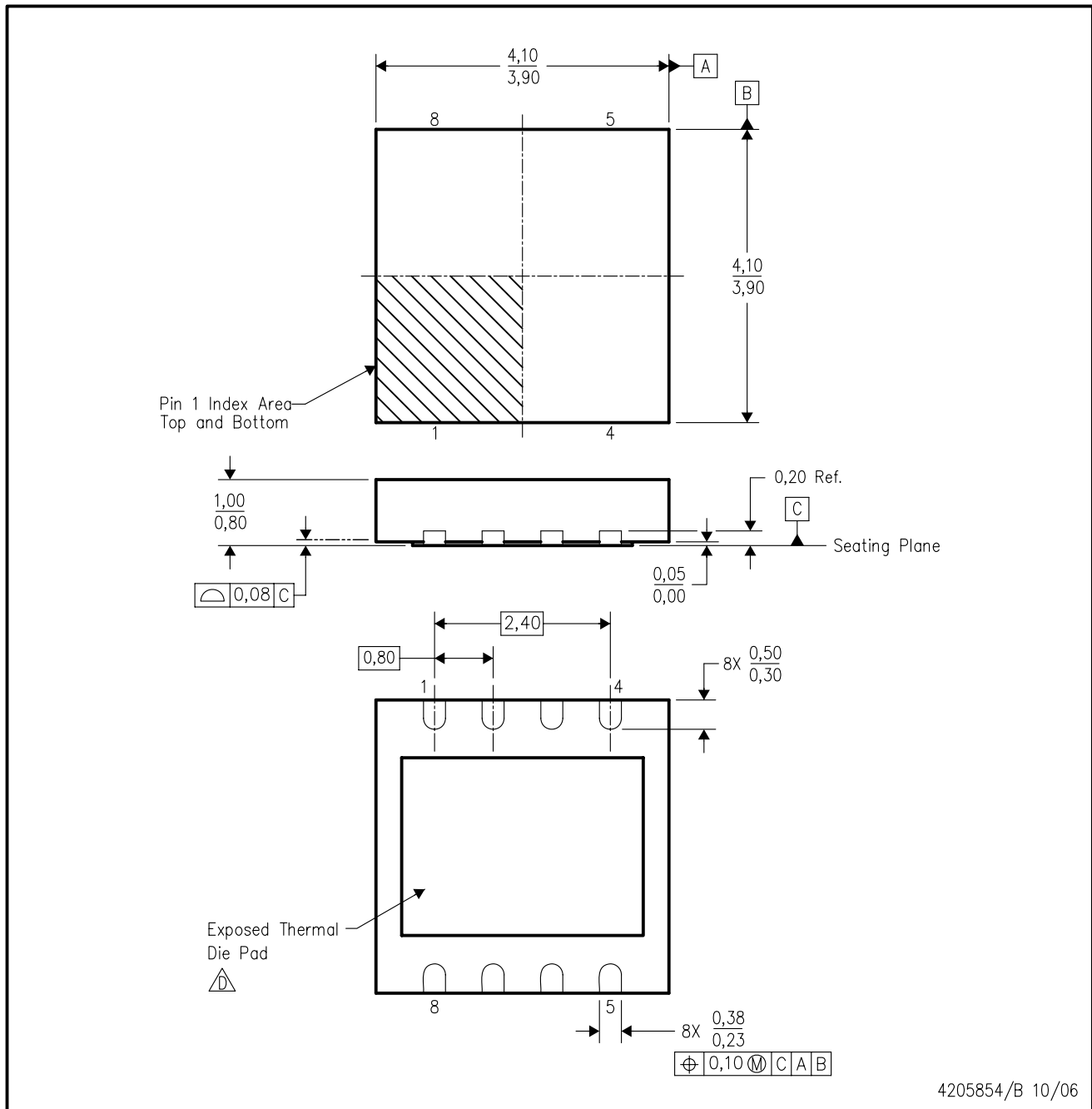


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DRM (S-PDSO-N8)

PLASTIC SMALL OUTLINE

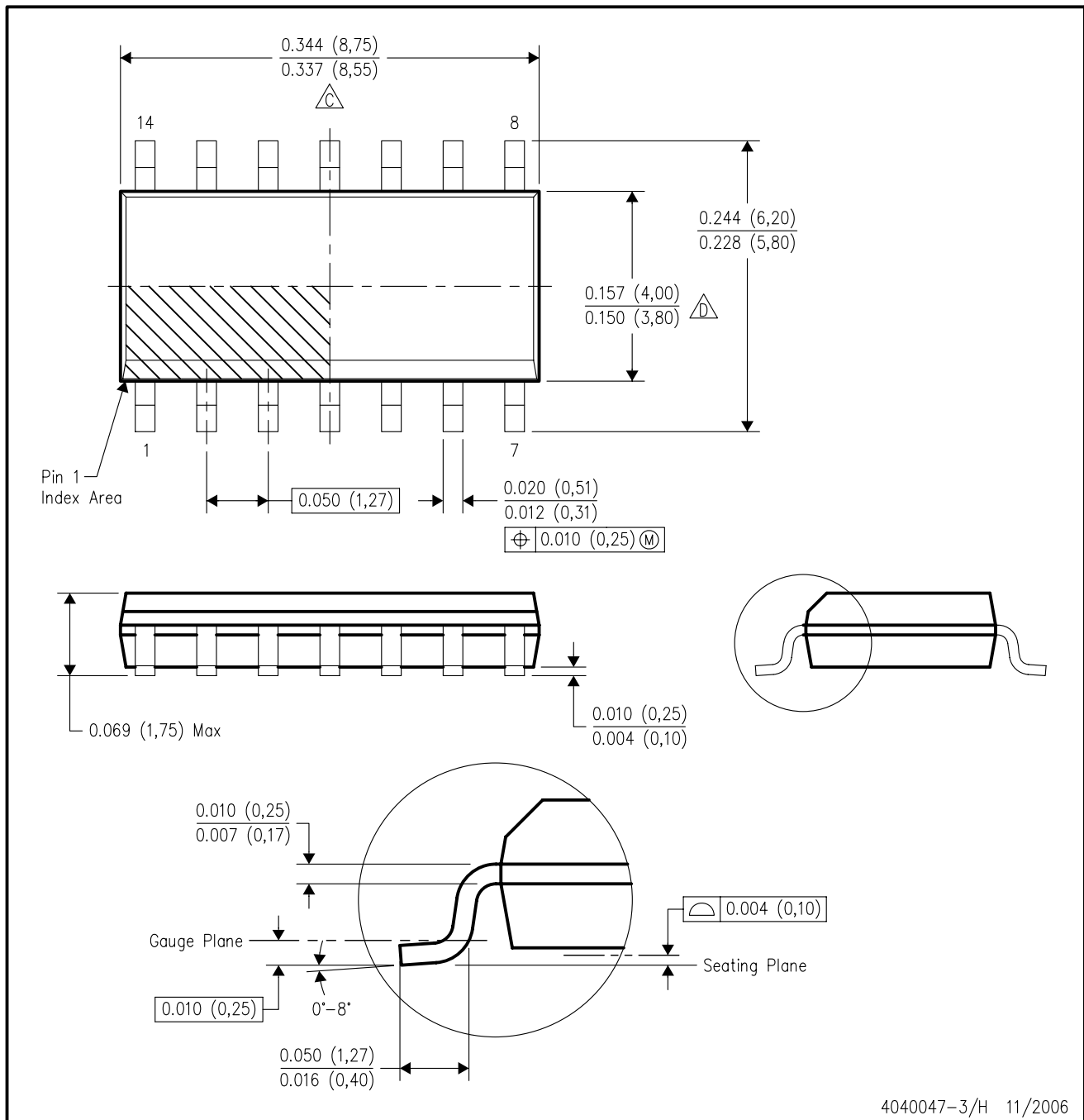


4205854/B 10/06

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - $\triangle$  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Package complies to JEDEC MO-229.

D (R-PDSO-G14)

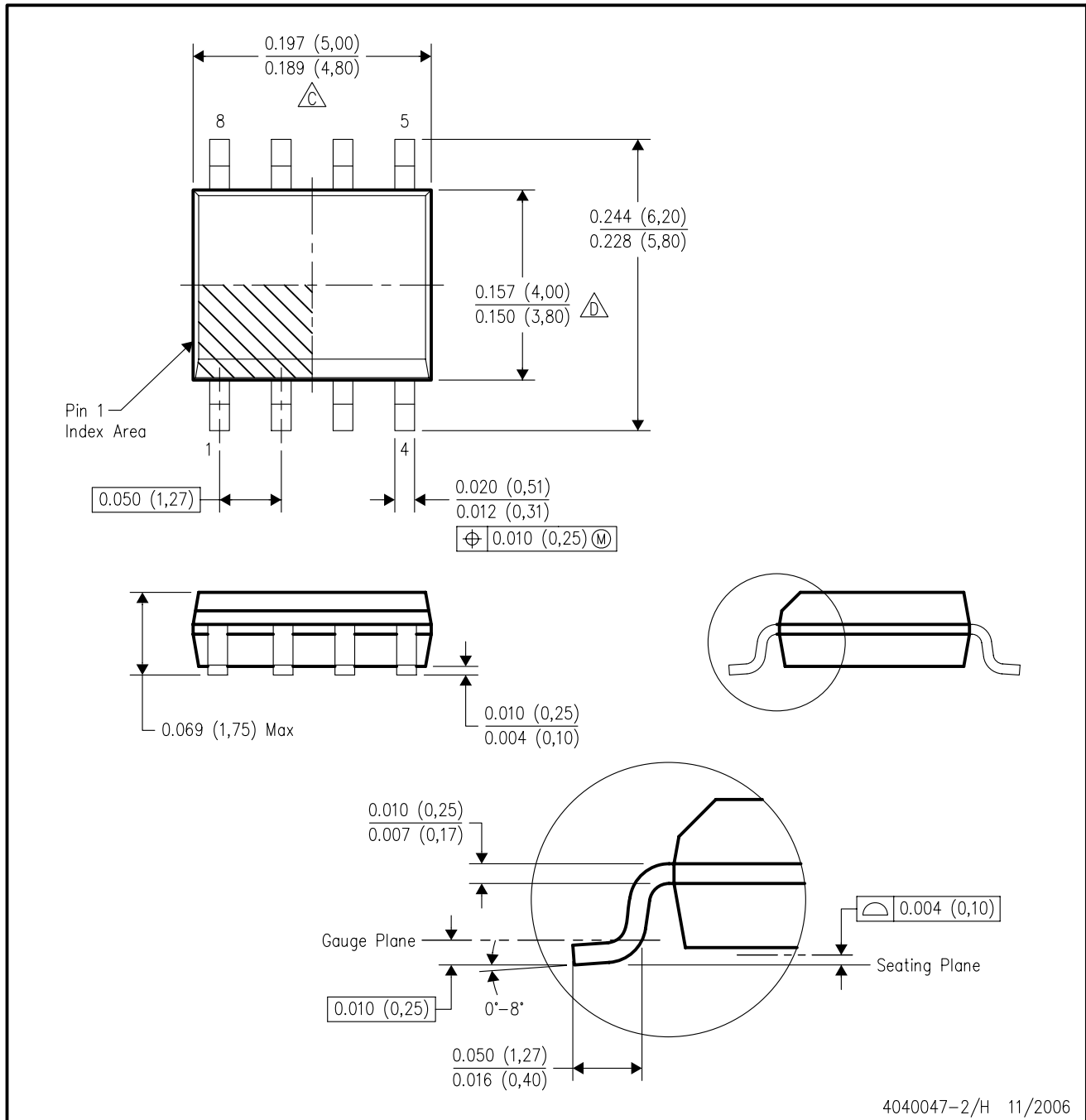
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265