



VSP3010

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SpeedPLUS™ 12-Bit, 12MHz CCD/CIS SIGNAL PROCESSOR

FEATURES

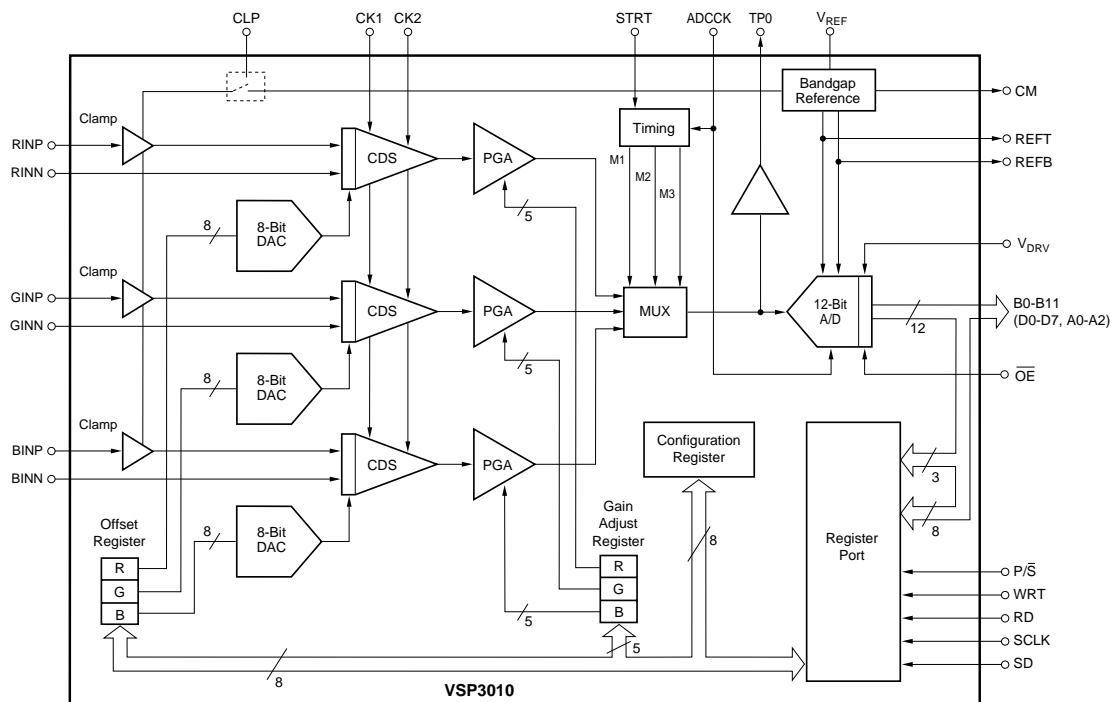
- 12-BIT, 12MHz A/D CONVERTER
- GUARANTEED NO MISSING CODES
- 3-CHANNEL, 4MHz COLOR SCAN MODE:
Correlated Double Samplers
8-Bit Offset Adjustment DACs
0dB to +13dB PGAs
- A/D INPUT MONITOR
- INTERNAL VOLTAGE REFERENCE
- SINGLE +5V SUPPLY
- 3V OR 5V DIGITAL OUTPUT
- LOW POWER: 500mW typ (CCD Mode)

APPLICATIONS

- CCD AND CIS COLOR SCANNERS
- FAX AND MULTI-FUNCTION MACHINES
- INDUSTRIAL/MEDICAL IMAGING SYSTEMS

DESCRIPTION

The VSP3010 is a complete, three-channel image signal processor for Charge Coupled Device (CCD) or Contact Image Sensor (CIS) systems. Each channel contains sensor signal sampling, Black Level adjustment and a programmable gain amplifier. The three inputs are multiplexed into a high speed, 12-bit analog-to-digital converter. Input circuitry can be configured, by digital command, for CCD or CIS sensors. A Black Clamp and Correlated Double Samplers (CDS) are provided for CCD sensors. For CIS devices, the VSP3010 provides a single-ended sampler and a reference input. The VSP3010 is available in a 48-lead LQFP package and operates from 0°C to +85°C with a single +5V supply.



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 Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = full specified temperature range, $V_{DDA} = +5V$, $V_{DDD} = +5V$, $f_{ADCCK} = 6MHz$, $f_{CK1} = 2MHz$, $f_{CK2} = 2MHz$, and PGA gain = 1, unless otherwise specified.

PARAMETER	CONDITIONS	VSP3010Y			UNITS
		MIN	TYP	MAX	
RESOLUTION			12		Bits
CONVERSION CHARACTERISTICS					
3-Channel CCD Mode		12			MHz
3-Channel CIS Mode		12			MHz
ANALOG INPUTS					
Full-Scale Input Range		0.5		3.5	Vp-p
Input Capacitance			10		pF
External Reference Voltage Range		0.25		1.75	V
Reference Input Resistance			800		Ω
Input Limits		$GND_A - 0.3$		$V_{DDA} + 0.3$	V
DYNAMIC CHARACTERISTICS					
Integral Non-Linearity (INL)			± 1	± 2	LSB
Differential Non-Linearity (DNL)			0.3	0.75	LSB
No Missing Codes			12		Bits
Input-Referred Noise			0.3		LSBs rms
PSRR	$V_{DDA} = +5V \pm 0.25V$		0.04		% FSR
DIGITAL INPUTS					
Logic Family			CMOS		
Convert Command	Start Conversion		Rising Edge of ADCCK		
High Level Input Current ($V_{IN} = V_{DDD}$)				20	μA
Low Level Input Current ($V_{IN} = 0V$)				20	μA
Positive-Going Threshold Voltage		3.00	3.40	3.80	V
Negative-Going Threshold Voltage		1.25	1.65	2.05	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			CMOS		
Logic Coding			Straight Binary		
V_{DRV} Supply Range		+2.7		+5.3	V
Output Voltage, $V_{DRV} = +5V$					
Low Level	$I_{OL} = 50\mu A$			+0.1	V
High Level	$I_{OH} = 50\mu A$	+4.6			V
Low Level	$I_{OL} = 1.6mA$			+0.4	V
High Level	$I_{OH} = 0.5mA$	+2.4			V
Output Voltage, $V_{DRV} = +3$					
Low Level	$I_{OL} = 50\mu A$			+0.1	V
High Level	$I_{OH} = 50\mu A$	+2.5			V
3-State Enable Time	$\overline{OE} = LOW$		20	40	ns
3-State Enable Time	$\overline{OE} = HIGH$		2	10	ns
Output Capacitance			5		pF
Data Latency			6		Clock Cycles
Data Output Delay	$C_L = 15pF$			12	ns
DC ACCURACY					
Zero Error			0.8		% FS
Gain Error			1.5		% FS
POWER SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	4.7	5	5.3	V
Supply Current: $+I_S$	3-Channel Mode		100	108	mA
	1-Channel Mode		82	90	mA
Power Dissipation	3-Channel Mode		500	540	mW
	1-Channel Mode		410	450	mW
Thermal Resistance, θ_{JA}			100		$^{\circ}C/W$
SPECIFIED TEMPERATURE RANGE		0		+85	$^{\circ}C$

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, (V_{DDA} , V_{DDD} , V_{DRV})	+6V
Analog Input	(-0.3V) to (+ V_{DDA} + 0.3V)
Logic Input	(-0.3V) to (+ V_{DDD} + 0.3V)
Operating Temperature	0°C to +85°C
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

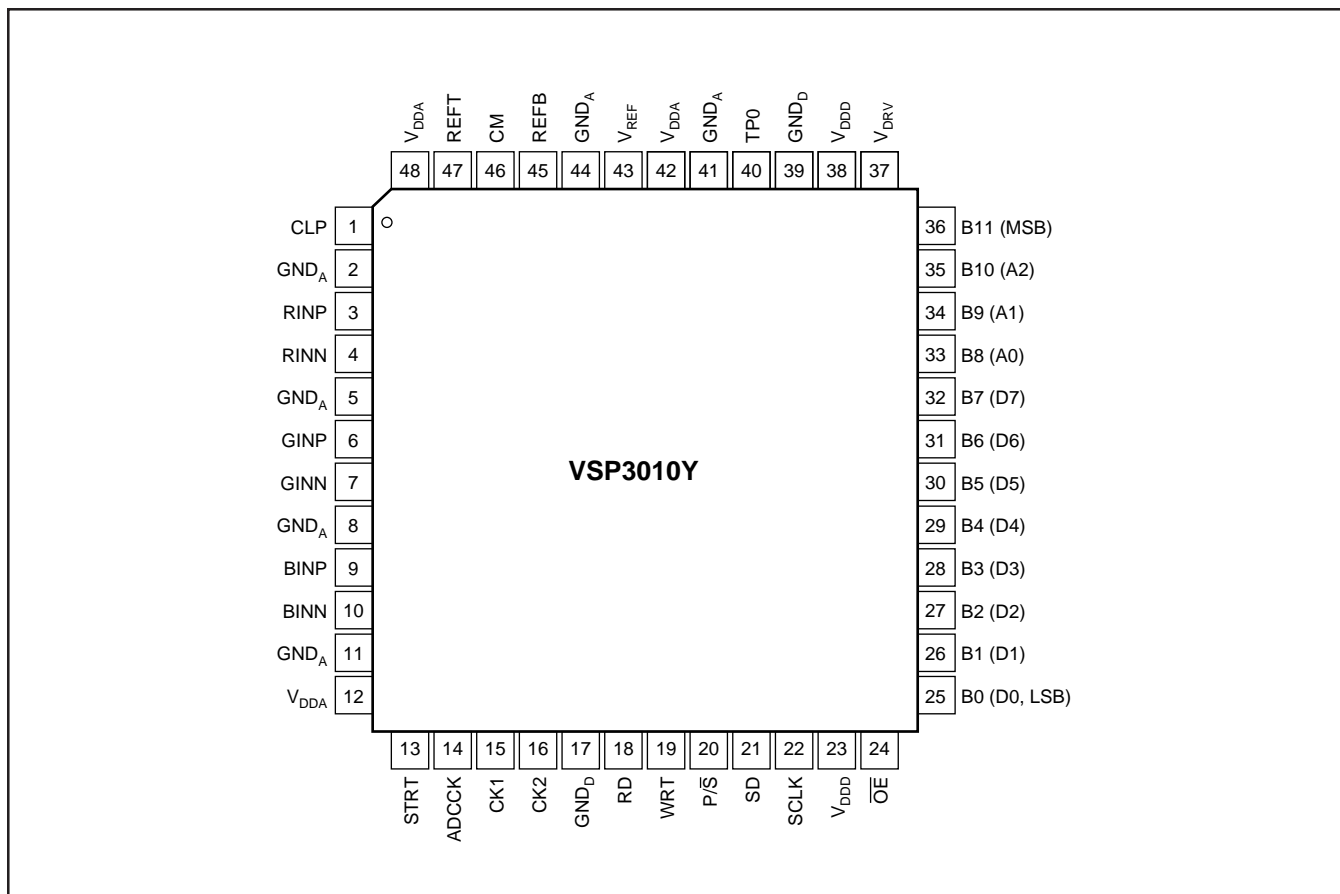
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽²⁾	TRANSPORT MEDIA
VSP3010Y "	LQFP-48 "	340 "	0°C to +85°C "	VSP3010Y "	VSP3010Y VSP3010Y/2K	250-Piece Tray Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "VSP3010Y/2K" will get a single 2000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

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PIN CONFIGURATION



PIN DESCRIPTIONS

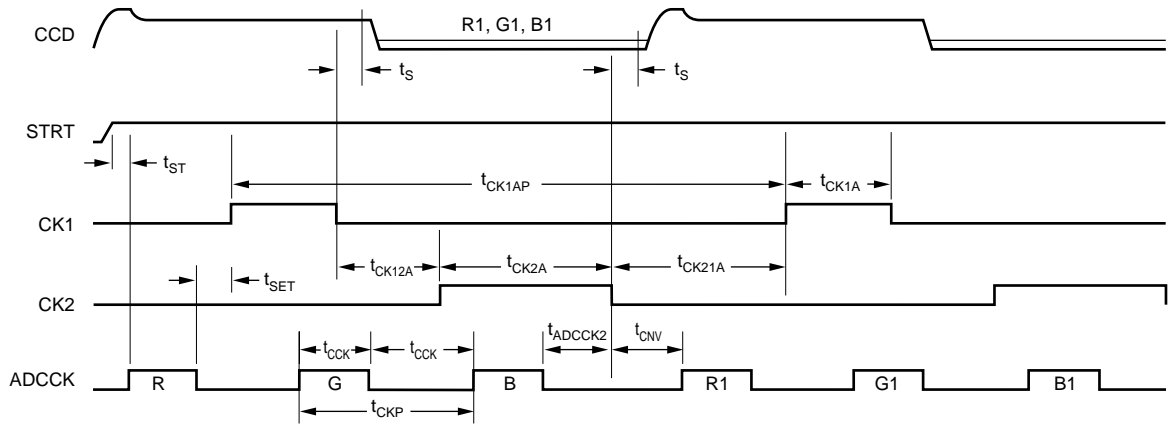
PIN	DESIGNATOR	TYPE	DESCRIPTION	PIN	DESIGNATOR	TYPE	DESCRIPTION
1	CLP	DI	Clamp Enable	25	B0 (D0) LSB	DIO	A/D Output (Bit 0) and Register Data Port (Bit 0)
2	GND _A	P	Analog Ground	26	B1 (D1)	DIO	A/D Output (Bit 1) and Register Data Port (Bit 1)
3	RINP	AI	Red-Channel Analog Input	27	B2 (D2)	DIO	A/D Output (Bit 2) and Register Data Port (Bit 2)
4	RINN	AI	Red-Channel Reference Input	28	B3 (D3)	DIO	A/D Output (Bit 3) and Register Data Port (Bit 3)
5	GND _A	P	Analog Ground	29	B4 (D4)	DIO	A/D Output (Bit 4) and Register Data Port (Bit 4)
6	GINP	AI	Green-Channel Analog Input	30	B5 (D5)	DIO	A/D Output (Bit 5) and Register Data Port (Bit 5)
7	GINN	AI	Green-Channel Reference Input	31	B6 (D6)	DIO	A/D Output (Bit 6) and Register Data Port (Bit 6)
8	GND _A	P	Analog Ground	32	B7 (D7)	DIO	A/D Output (Bit 7) and Register Data Port (Bit 7)
9	BINP	AI	Blue-Channel Analog Input	33	B8 (A0)	DIO	A/D Output (Bit 8) and Register Address (Bit 0)
10	BINN	AI	Blue-Channel Reference Input	34	B9 (A1)	DIO	A/D Output (Bit 9) and Register Address (Bit 1)
11	GND _A	P	Analog Ground	35	B10 (A2)	DIO	A/D Output (Bit 10) and Register Address (Bit 2)
12	V _{DDA}	P	Analog Power Supply, +5V	36	B11 MSB	DO	A/D Output (Bit 11)
13	STRT	DI	Start Line Scanning	37	V _{DRV}	P	Output Driver Voltage Supply
14	ADCKK	DI	A/D Converter Clock Input	38	V _{DD}	P	Digital Power Supply, +5V
15	CK1	DI	Sample Reference Clock	39	GND _D	P	Digital Ground
16	CK2	DI	Sample Data Clock	40	TP0	AO	A/D Converter Input Monitor Pin
17	GND _D	P	Digital Ground	41	GND _A	P	Analog Ground
18	RD	DI	Read Signal for Registers	42	V _{DDA}	P	Analog Power Supply, +5V
19	WRT	DI	Write Signal for Registers	43	V _{REF}	AIO	Reference Input/Output
20	P/S	DI	Parallel/Serial Port Select; HIGH = Parallel, LOW = Serial	44	GND _A	P	Analog Ground
21	SD	DI	Serial Data Input	45	REFB	AO	Bottom Reference
22	SCLK	DI	Serial Data Clock	46	CM	AO	Common-Mode Voltage
23	V _{DD}	P	Digital Power Supply, +5V	47	REFT	AO	Top Reference
24	OE	DI	A/D Converter Output Enable	48	V _{DDA}	P	Analog Power Supply, +5V

TIMING DIAGRAMS

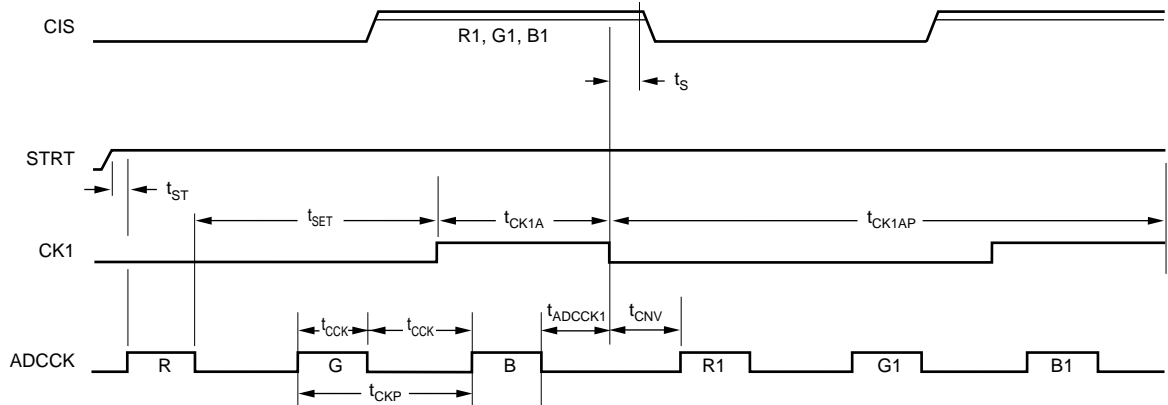
Timing specifications = t_{MIN} to t_{MAX} with +5V power supply.

Timing for 3-Channel CCD/CIS Mode

3-Channel CCD Mode



3-Channel CIS Mode

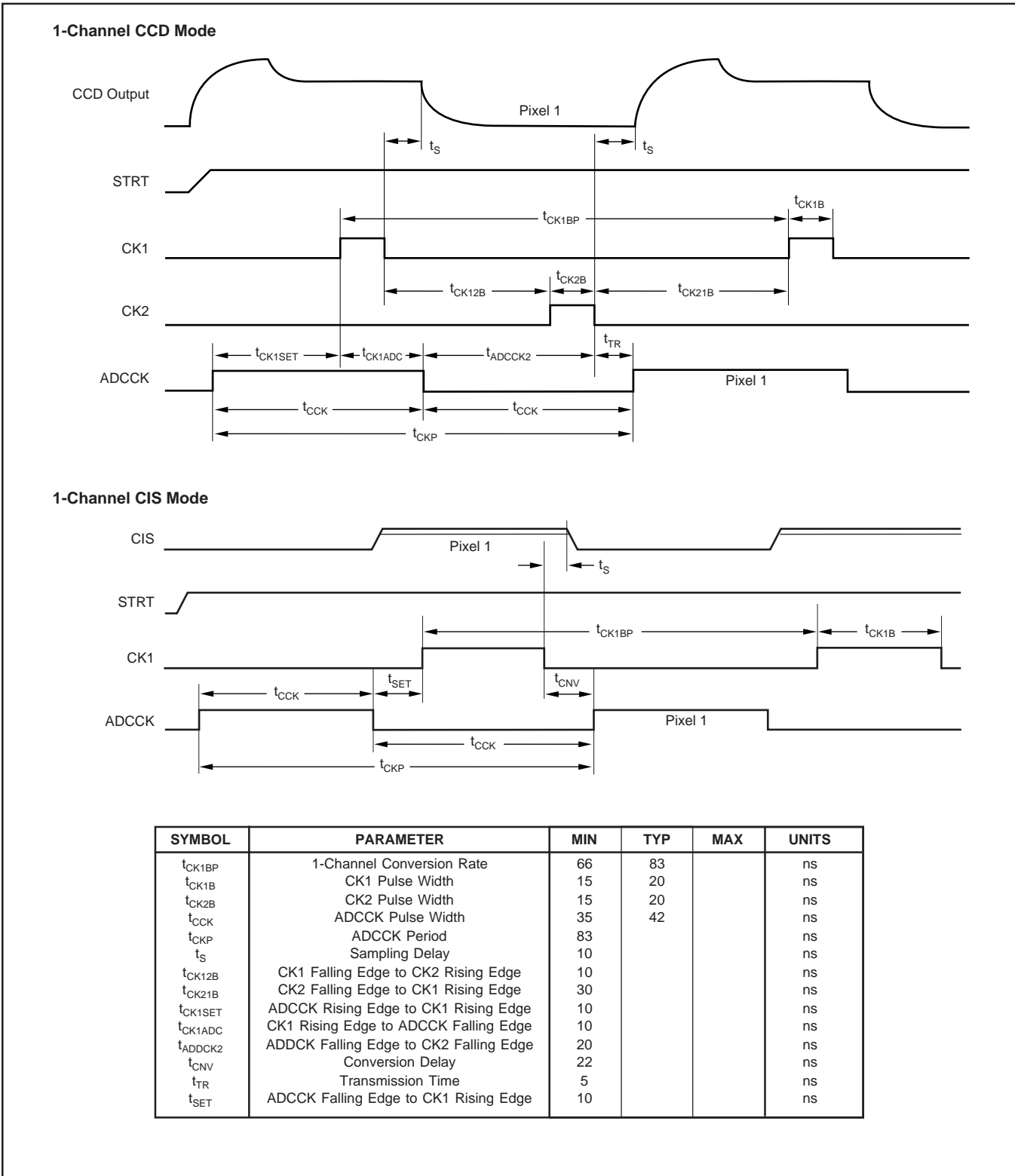


SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CK1AP}	3-Channel Conversion Rate	200	250		ns
t_{CK1A}	CK1 Pulse Width	15	70		ns
t_{CK2A}	CK2 Pulse Width	15	70		ns
t_{CCK}	ADCCK Pulse Width	35	42		ns
t_{CKP}	ADCCK Period	83			ns
t_s	Sampling Delay	10			ns
t_{CK12A}	CK1 Falling Edge to CK2 Rising Edge	15			ns
t_{CK21A}	CK2 Falling Edge to CK1 Rising Edge	50			ns
t_{SET}	ADCCK Falling Edge to CK1 Rising Edge	10			ns
$t_{ADCCCK2}$	ADCCK Falling Edge to CK2 Falling Edge	20			ns
$t_{ADCCCK1}$	ADCCK Falling Edge to CK1 Falling Edge	20			ns
t_{CNV}	Conversion Delay	22			ns
t_{ST}	Start Conversion Time	20	100		ns

TIMING DIAGRAMS (cont.)

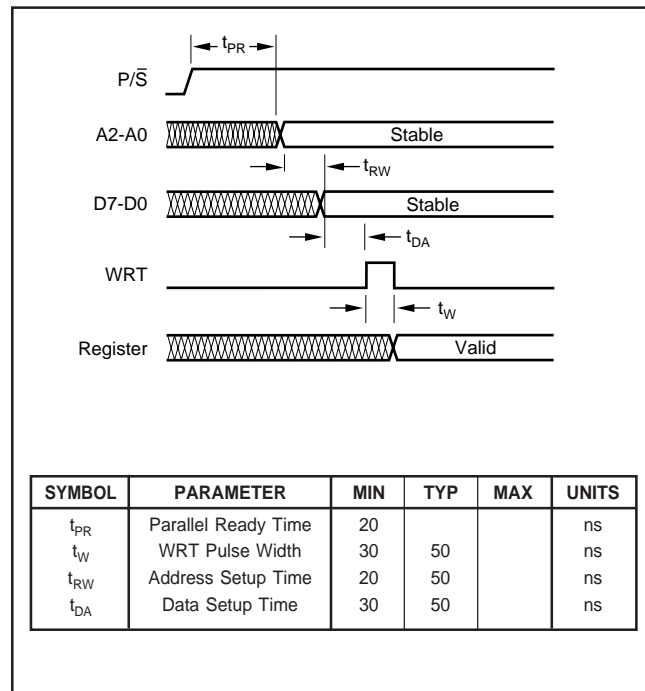
Timing specifications = t_{MIN} to t_{MAX} with +5V power supply.

Timing for 1-Channel CCD/CIS Mode

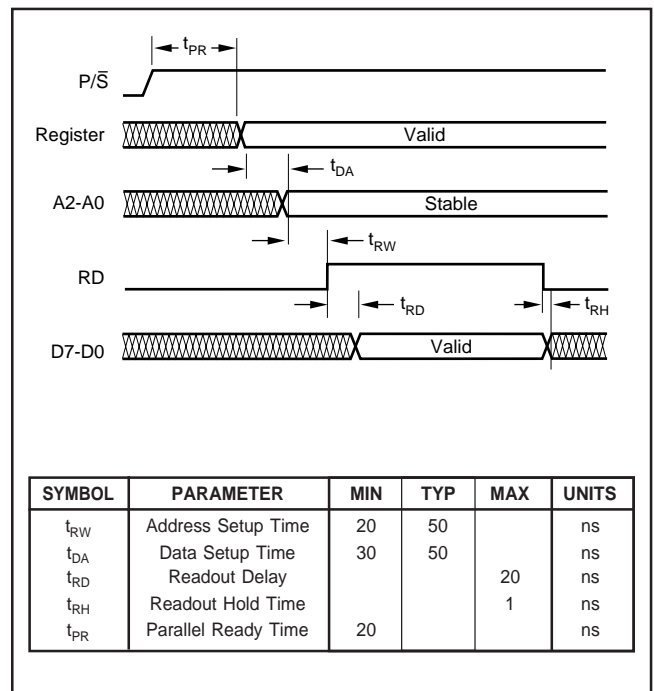


TIMING DIAGRAMS (cont.)

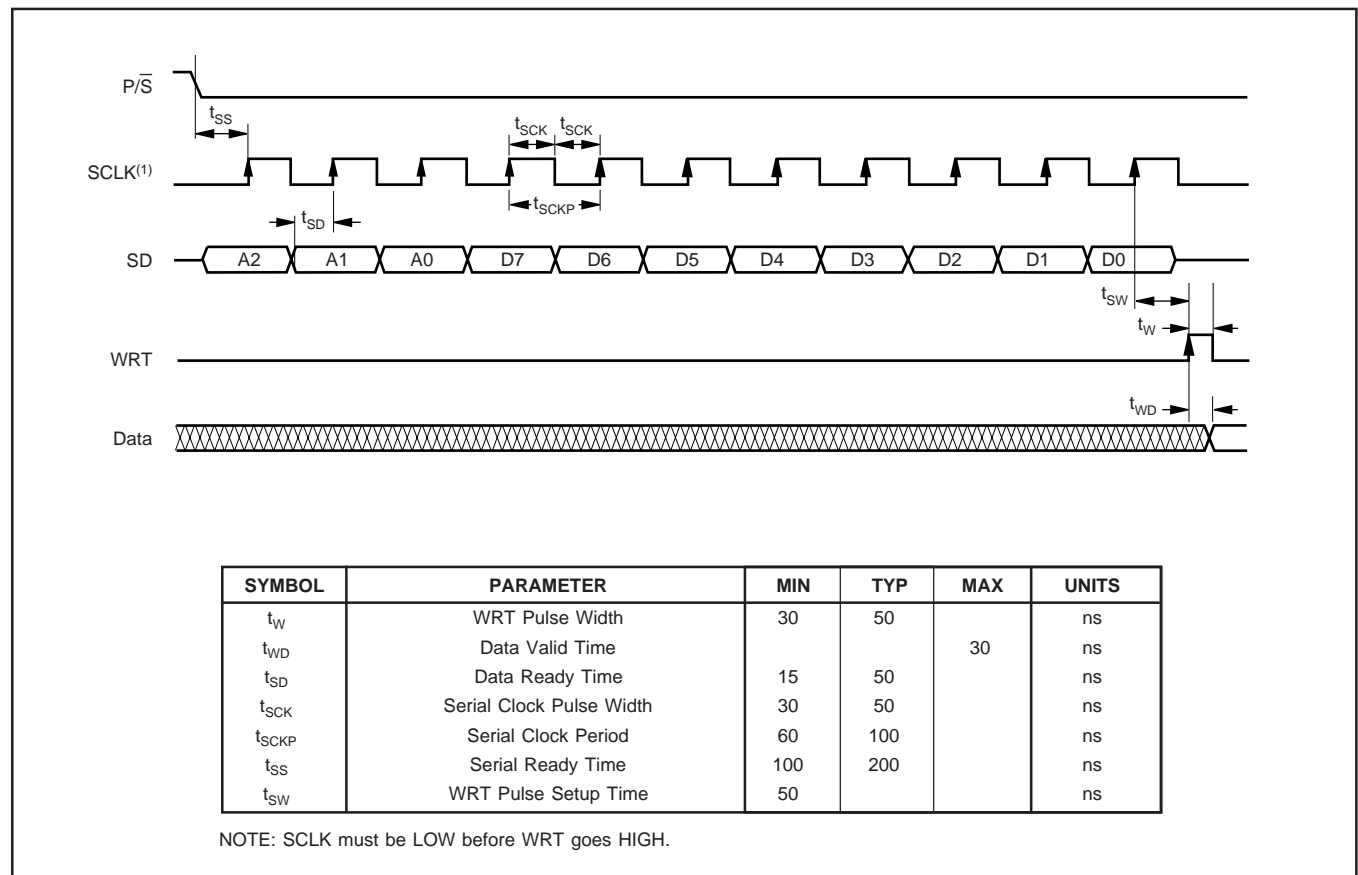
Timing for Parallel Port Writing



Timing for Reading

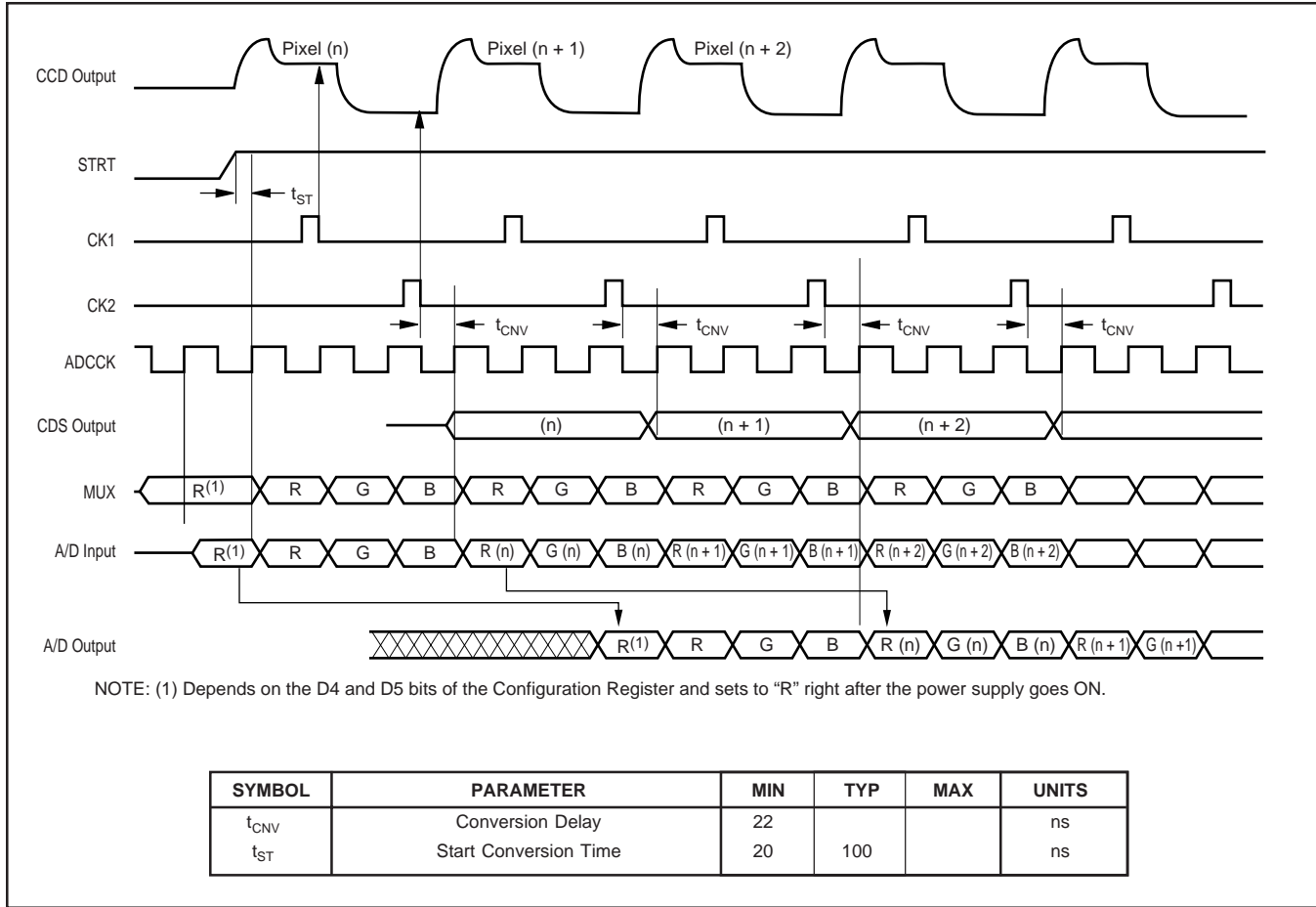


Timing for Serial Port Writing

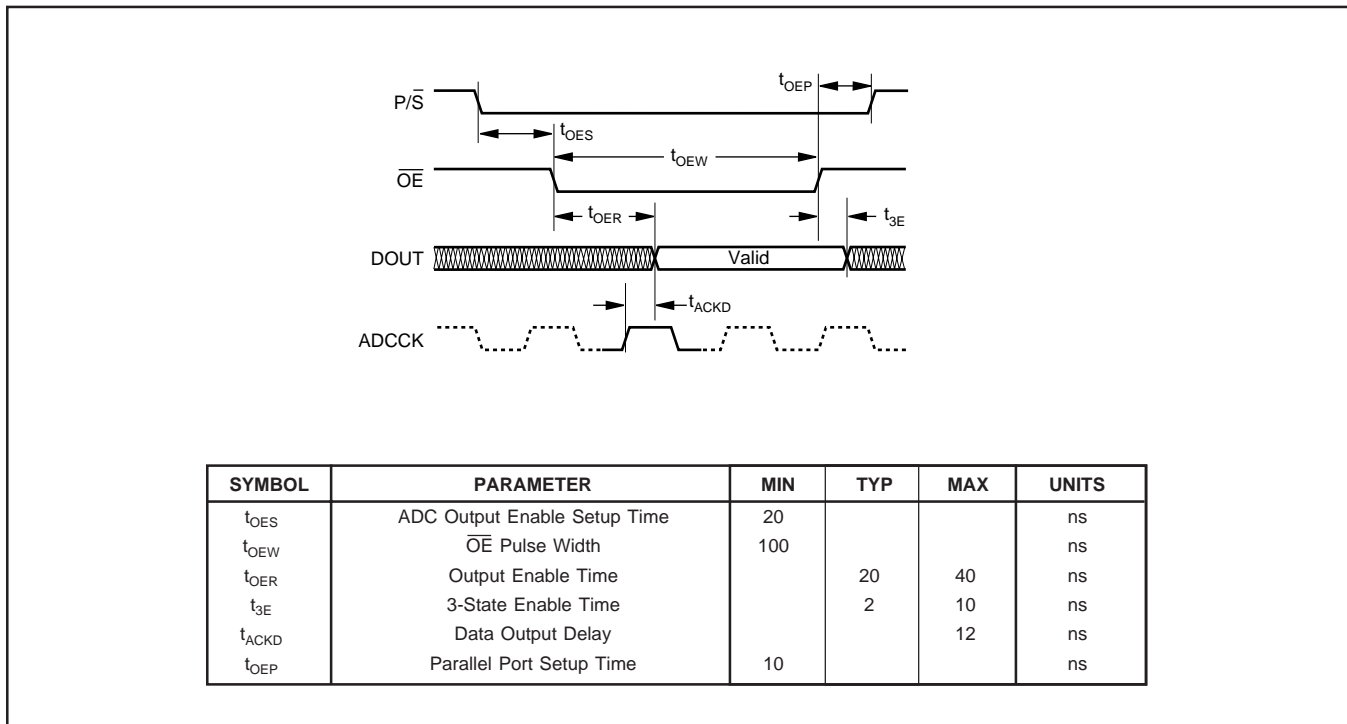


TIMING DIAGRAMS (Cont)

DOUT Timing Diagram—3-Channel CCD Mode

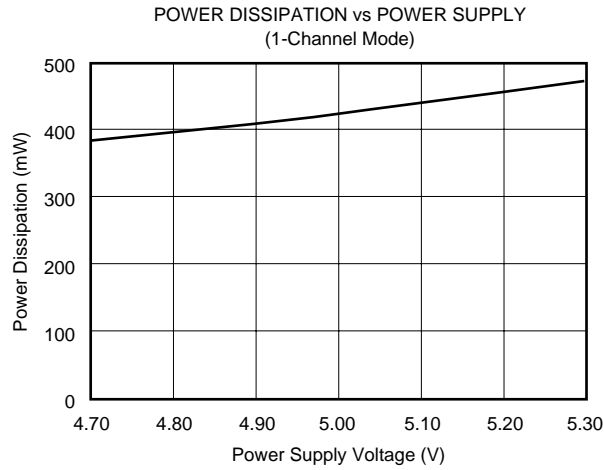
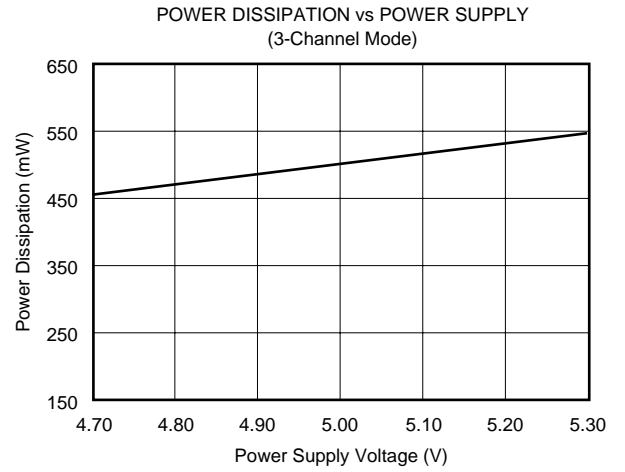
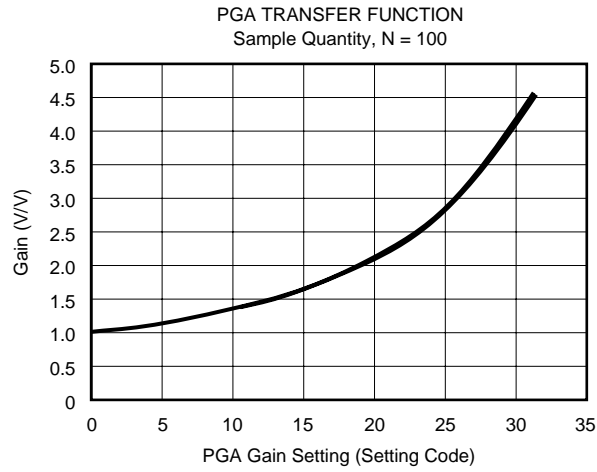


Timing for A/D Output



TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{DDA} = +5\text{V}$, $V_{DDD} = +5\text{V}$, $f_{ADCCK} = 6\text{MHz}$, $f_{CK1} = 2\text{MHz}$, and $f_{CK2} = 2\text{MHz}$, unless otherwise specified.



THEORY OF OPERATION

The VSP3010 can be operated in one of the following four modes:

- 3-Channel CCD Mode
- 3-Channel CIS Mode
- 1-Channel CCD Mode
- 1-Channel CIS Mode

3-CHANNEL CCD MODE

In this mode, the VSP3010 can simultaneously process three output CCD signals. These signals are AC-coupled to the RINP, GINP, and BINP inputs. RINN, GINN, BINN are not used in this mode and should be grounded. The CLP signal enables internal biasing circuitry to clamp these inputs to a proper voltage, enabling internal CDS circuitry to operate properly. VSP3010 inputs may be applied as DC-coupled inputs, which need to be level-shifted to a proper DC level.

The correlated double samplers take two samples of the incoming CCD signals; the CCD reference levels are taken on the falling edge of CK1 and the CCD information is taken on the falling edge of CK2. These two samples are then subtracted by the CDSs and the result is the CDS' output.

Three channels are used to process three inputs simultaneously. Each consists of a 5-bit PGA (0dB to +13dB) and an 8-bit offset digital-to-analog converter (+50mV to -150mV). A 3-to-1 analog MUX follows the CDS channels and feeds a high performance 12-bit A/D converter. The analog MUX can be programmed to cycle between red, green, and blue or blue, green, and red.

When the STRT signal is HIGH, the conversion is initiated on the rising edge of ADCCK. The STRT signal indicates the first samples for a scan line. When STRT goes LOW, the analog MUX is switched to the first sample of the sequence.

As specified in the "3-Channel CCD Mode" timing diagram, the falling edge of CK2 must be in the LOW period of ADCCK. If the falling edge of CK2 is in the HIGH period of ADCCK (in the timing diagram, ADCCK for sampling B channel), the VSP3010 will not function properly.

3-CHANNEL CIS MODE

In this mode, the VSP3010 is operated as 3-channel samplers and a digitizer. Unlike the CCD mode, VSP3010 takes only one sample on the falling edge of CK1 for each input. Since only one sample is taken, CK2 is grounded in this operation. The input signal is DC-coupled in most cases. For example, for the red channel, RINP is the CIS signal input, and RINN is the CIS reference signal. The same applies to the green channel (GINP and GINN) and blue channel (BINP and BINN).

In this mode, three CDSs become CIS signal processing circuits (acting like a track-and-hold) to process three inputs simultaneously. Each CIS signal processing circuit consists of a 5-bit PGA (0dB to +13dB) and an 8-bit offset

DAC (+50mV to -150mV). A 3-to-1 analog MUX follows the CIS signal processing circuits and feeds a high performance 12-bit A/D converter. The analog MUX can be programmed to cycle between red, green, and blue or blue, green, and red.

When the STRT signal is HIGH, the conversion is initiated on the rising edge of ADCCK. The STRT signal indicates the first sample for a scan line. When STRT goes LOW, the analog MUX is switched to the first sample of the sequence.

As specified in the "3-Channel CIS Mode" timing diagram, the falling edge of CK1 must be in the LOW period of ADCCK. If the falling edge of CK1 is in the HIGH period of ADCCK (in the timing diagram, ADCCK for sampling B channel), the VSP3010 will not function properly.

1-CHANNEL CCD MODE

In this mode, the VSP3010 processes only one CCD signal. The CCD signal is AC-coupled to RINP, GINP, or BINP (as selected by the data in the Configuration Register). RINN, GINN, BINN are not used in this mode and should be grounded. The CLP signal enables internal biasing circuitry to clamp this input to a proper voltage so that internal CDS circuitry can work properly. The VSP3010 input may be applied as a DC-coupled input, which needs to be level-shifted to a proper DC level.

The CDS takes two samples of the incoming CCD signal. The CCD reference value is taken on the falling edge of CK1 and the CCD information is taken on the falling edge of CK2. These two samples are then subtracted by the CDS and the result is the CDS' output.

In this mode, only one of the three channels is enabled. Each CDS consists of a 5-bit PGA (0dB to +13dB) and an 8-bit offset DAC (+50mV to -150mV). A 3-to-1 analog MUX is inserted between the CDSs and a high performance 12-bit A/D converter. The analog MUX is not cycling between channels in this mode. Instead, the analog MUX is connected to a specific channel, depending on the data in the Configuration Register.

As specified in the "1-Channel CCD Mode" timing diagram, the rising edge of CK1 must be in the HIGH period of ADCCK and the falling edge of the CK2 must be in the LOW period of ADCCK. Otherwise, the VSP3010 will not function properly.

1-CHANNEL CIS MODE

In this mode, the VSP3010 is operated as a 1-channel sampler and digitizer. Unlike the CCD mode, VSP3010 takes only one sample on the falling edge of CK1. Since only one sample is taken, CK2 is grounded in this operation. The input signal is DC-coupled in most cases. Here, the VSP3010 inputs are differential. For example, for the red channel, RINP is the CIS signal input, and RINN is the CIS reference signal. The same applies to the green channel (GINP and GINN) and blue channel (BINP and BINN).

In this mode, the CDS becomes a CIS signal processing circuit (acting like a track-and-hold). Each CIS signal processing circuit consists of a 5-bit PGA (0dB to +13dB) and an 8-bit offset DAC (+50mV to -150mV). A 3-to-1 analog MUX follows the CIS signal processing circuits and feeds a high performance 12-bit A/D converter. The analog MUX is not cycling between channels in this mode. Instead, the analog MUX is connected to a specific channel, depending on the data in the Configuration Register.

As specified in the “1-Channel CIS Mode” timing diagram, the active period of CK1 (t_{CK1B}) must be in the LOW period of ADCCK. If it is in the HIGH period of ADCCK, the VSP3010 will not function properly.

ANALOG PGA

There is one analog PGA on each channel. Each analog PGA is controlled by a 5-bit PGA gain register. The analog PGA gain varies from 1 to 4.44 (0dB to +13dB). The transfer function of the PGA is:

$$\text{Gain} = 4/(4 - 0.1 \cdot X)$$

where X is the integer representation of the 5-bit PGA gain register. Figure 1 shows the PGA transfer function plot.

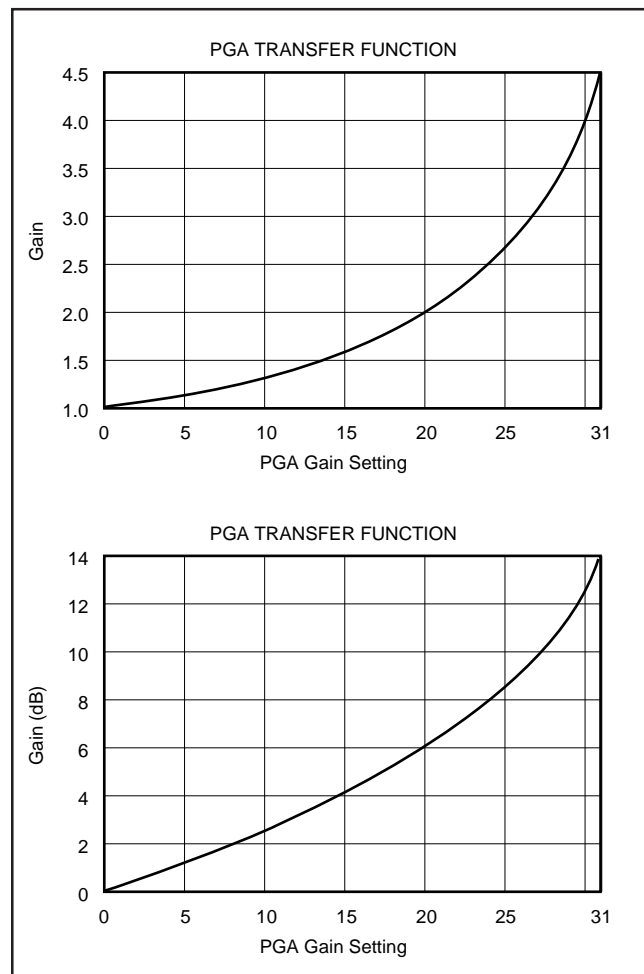


FIGURE 1. PGA Transfer Function Plot.

CHOOSING AC INPUT COUPLING CAPACITORS

The purpose of the input coupling capacitor is to isolate the DC output of the CCD array from affecting the VSP3010. The internal clamping circuitry restores the necessary DC component to the CCD output signal. The internal clamp voltage, V_{CLAMP} , is derived from the reference. V_{CLAMP} depends on the value of V_{REF} ; if V_{REF} is set to 1V, V_{CLAMP} is 2.5V and if V_{REF} is set to 1.5V, V_{CLAMP} is 3V. There are many factors that determine the size of the input coupling capacitors including CCD signal swing, voltage droop across the input capacitor since the last clamp interval, leakage current of the VSP3010 input circuitry, and the time period of CK1. Figure 2 shows a simplified equivalent circuit of the VSP3010 inputs. In this equivalent circuit, the input coupling capacitor, C_{IN} , and the sampling capacitor, C_1 , are constructed as a capacitor divider (during CK1). For AC analysis, op amp inputs are grounded. Therefore, the sampling voltage, V_S (during CK1) is:

$$V_S = (C_{IN}/C_{IN} + C_1) \cdot V_{IN}$$

From this equation, we see that a larger value of C_{IN} makes V_S closer to V_{IN} . In other words, the input signal V_{IN} will be attenuated less if C_{IN} is large. However, there is a disadvantage to using a large value of C_{IN} : the larger the C_{IN} , the more dummy or optical black pixels must be used to restore the DC component of the input signal.

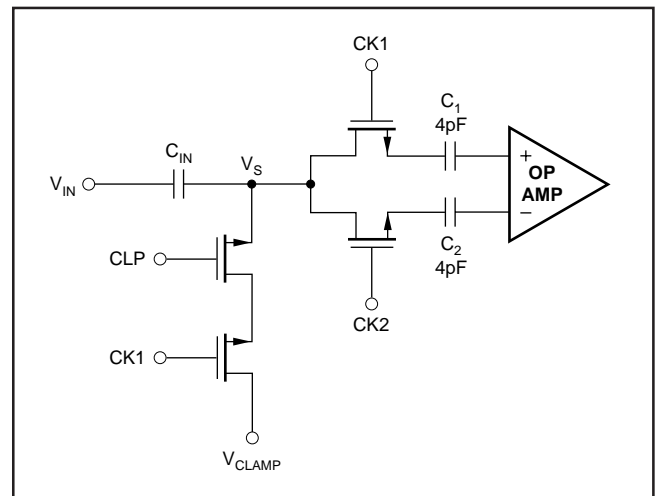


FIGURE 2. Equivalent Circuit of VSP3010 Inputs.

CHOOSING C_{MAX} AND C_{MIN}

As mentioned previously, a large C_{IN} is preferable if there is enough time for the CLP signal to charge up C_{IN} . Typically, 0.01 μ F to 0.1 μ F of C_{IN} can be used for most cases. In order to optimize C_{IN} , the following two equations can be used to calculate C_{MAX} and C_{MIN} :

$$C_{MAX} = (t_{CK1} \cdot N) / [R_{SW} \cdot \ln(V_D/V_{ERROR})]$$

where, t_{CK1} is the time when both CK1 and CLP are HIGH and N is the number of black pixels, R_{SW} is the total switch

resistance, V_D is the droop across C_{IN} and V_{ERROR} is the difference between V_S and V_{CLAMP} . The nominal value of R_{SW} is 4k Ω plus the driver's impedance. 0.1V should be tolerable for V_{ERROR} and still keep the VSP3010 working properly.

$$C_{MIN} = (I/V_{ERROR}) \cdot t$$

where, I is 10nA, the typical leakage current of the VSP3010 input circuitry and t is the time between clamp pulses.

PROGRAMMING THE VSP3010

The VSP3010 consists of three CCD or CIS channels and a 12-bit A/D converter. Each channel (red, green, and blue) has its own 8-bit offset and 5-bit gain adjustable registers to be programmed by the user. There is also a 7-bit Configuration Register on-chip to program the different operation modes. These registers are as follows:

ADDRESS			REGISTER
A2	A1	A0	
0	0	0	Configuration Register (7-Bit)
0	0	1	Red Channel Offset Register (8-Bit)
0	1	0	Green Channel Offset Register (8-Bit)
0	1	1	Blue Channel Offset Register (8-Bit)
1	0	0	Red Channel Gain Register (5-Bit)
1	0	1	Green Channel Gain Register (5-Bit)
1	1	0	Blue Channel Gain Register (5-Bit)
1	1	1	Reserved

These Registers can be accessed by either the parallel or serial port. In the parallel mode, the address and data port are combined with the ADC data output pins. The data bus is assigned as D0 to D7 (pin 25 to pin 32) and the address bus is A0 to A2 (pin 33 to pin 35). In the serial mode, serial data (SD), serial clock (SCLK), and write signal (WRT pin for both parallel and serial writing) are assigned. The following table shows how to access these modes.

\overline{OE}	P/\overline{S}	MODE
0	0	A/D Data Output Enabled, Serial Mode Enabled
0	1	Prohibit Mode
1	0	A/D Data Output Disabled, Serial Mode Enabled
1	1	A/D Data Output Disabled, Parallel Mode Enabled

Configuration Register

The Configuration Register is designed as follows:

BIT	LOGIC '0'	LOGIC '1'
D0	CCD Mode	CIS Mode
D1	$V_{REF} = 1V$	$V_{REF} = 1.5V$
D2	Internal Reference	External Reference
D3	3-Channel, D4 and D5 Disabled	1-Channel, D4 and D5 Enabled
		D4 D5
		0 0 Red Channel
		0 1 Green Channel
		1 0 Blue Channel
		1 1 Reserved
D6	R > G > B MUX Sequence	B > G > R MUX Sequence
D7	Reserved	Reserved

For Reading/Writing to the Configuration Register, the address will be:

$$A2 = '0', A1 = '0', \text{ and } A0 = '0'$$

Example:

A 3-channel CCD with internal reference $V_{REF} = 1V$ (2V full-scale input), the mode will be:

$$\Rightarrow D0 = '0', D1 = '0' \text{ and } D3 = '0'$$

For this example, V_{REF} will be 1V.

Bypass V_{REF} with 10 μF and 0.1 μF capacitors when internal reference mode is used.

Example:

A 1-channel CIS mode (red channel) with external 1.2V reference:

$$\Rightarrow D0 = '1', D1 = X, D2 = '1', D4 = '0' \text{ and } D5 = '0'$$

For this example, V_{REF} will be an input pin, applied with 1.2V. This input will set the full-scale input of the VSP3010 at 2.4V.

Offset Registers

Offset registers control the analog offset input to the channel prior to the PGA. There is an 8-bit Offset Register on each channel. The offset range varies from -150mV to +50mV. The Offset Register uses a Straight Binary code. All '0's correspond to -150mV and all '1's correspond to +50mV of the offset adjustment.

PGA Gain Registers

The PGA Gain Registers control the analog gain to the channels prior to the A/D converter. There is a 5-bit PGA Gain Register on each channel. The gain range varies from 1 to 4.44 (0dB to +13dB). The PGA Gain Register is a Straight Binary code. All '0's correspond to analog gain of 0dB and all '1's correspond to the analog gain of 13dB.

OFFSET AND GAIN CALIBRATION SEQUENCE

DIGITAL OUTPUTS

The digital outputs of the VSP3010 are designed to be compatible with both high-speed TTL and CMOS logic families. The driver stage of the digital outputs is supplied through a separate supply pin, VDRV, which is not connected to the analog supply pins. By adjusting the voltage on VDRV, the digital output levels will vary respectively. Thus, it is possible to operate the VSP3010 on a +5V analog supply while interfacing the digital outputs to 3V logic.

It is recommended to keep the capacitive loading on the data lines as low as possible (typically less than 15pF). Larger capacitive loads demanding higher charging current surges can feed back to the analog portion of the VSP3010 and influence the performance. If necessary, external buffers or latches may be used which provide the added benefit of isolating the VSP3010 from any digital noise activities on

the bus coupling back high frequency noise. In addition, resistors in series with each data line may help minimize the surge current. Their use depends on the capacitive loading seen by the converter. As the output levels change from low to high and high to low, values in the range of 100Ω to 200Ω will limit the instantaneous current the output stage has to provide for recharging the parasitic capacitances.

GROUNDING, BYPASSING, AND POWER SUPPLY RECOMMENDATIONS

Proper grounding, bypassing, short lead length and the use of ground planes are particularly important for high frequency designs. Multi-layer PC boards are recommended for the best performance since they offer distinct advantages such as minimizing ground impedance, separation of signal layers by ground layers, etc. It is recommended that analog and digital ground pins of the VSP3010 be joined together at the IC and connected only to the analog ground of the system.

The VSP3010 has analog and digital supply pins, however, the converter should be treated as an analog component and all supply pins should be powered by the analog supply. This will ensure the most consistent results since digital supply lines often carry high levels of noise that would otherwise be coupled into the converter and degrade the achievable performance.

As the result of the high operation speed, the converter also generates high frequency current transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently

bypassed. Figure 3 shows the recommended decoupling schemes for the entire chip. In most cases, 0.1μF ceramic chip capacitors are adequate to keep the impedance low over the wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin.

When the VSP3010 is powered on, it will be initialized as a 3-channel CCD, 1V internal (2V full scale) reference mode with analog gain of 1. This mode is commonly used for CCD scanner applications. The calibration procedure is done at the very beginning of the scan. Once calibration is done, registers on VSP3010 will keep this information (offset and gain for each channel) during the operation.

To calibrate the VSP3010, use the following procedure:

- Step 1: Set the VSP3010 to the proper mode.
- Step 2: Set analog PGA gain to 1 (code: 00_H) and offset to 0mV (code: C0_H).
- Step 3: Scan a dark line.
- Step 4: Calculate the pixel offsets according to the ADC output.
- Step 5: Readjust input Offset Registers.
- Step 6: Scan a white line.
- Step 7: Calculate gain. It will be the ADC full scale divided by the ADC output when the white line is scanned.
- Step 8: Set the Gain Register. If the ADC output is not close to full scale, go back to Step 3. The calibration is complete if the output is close to full scale.

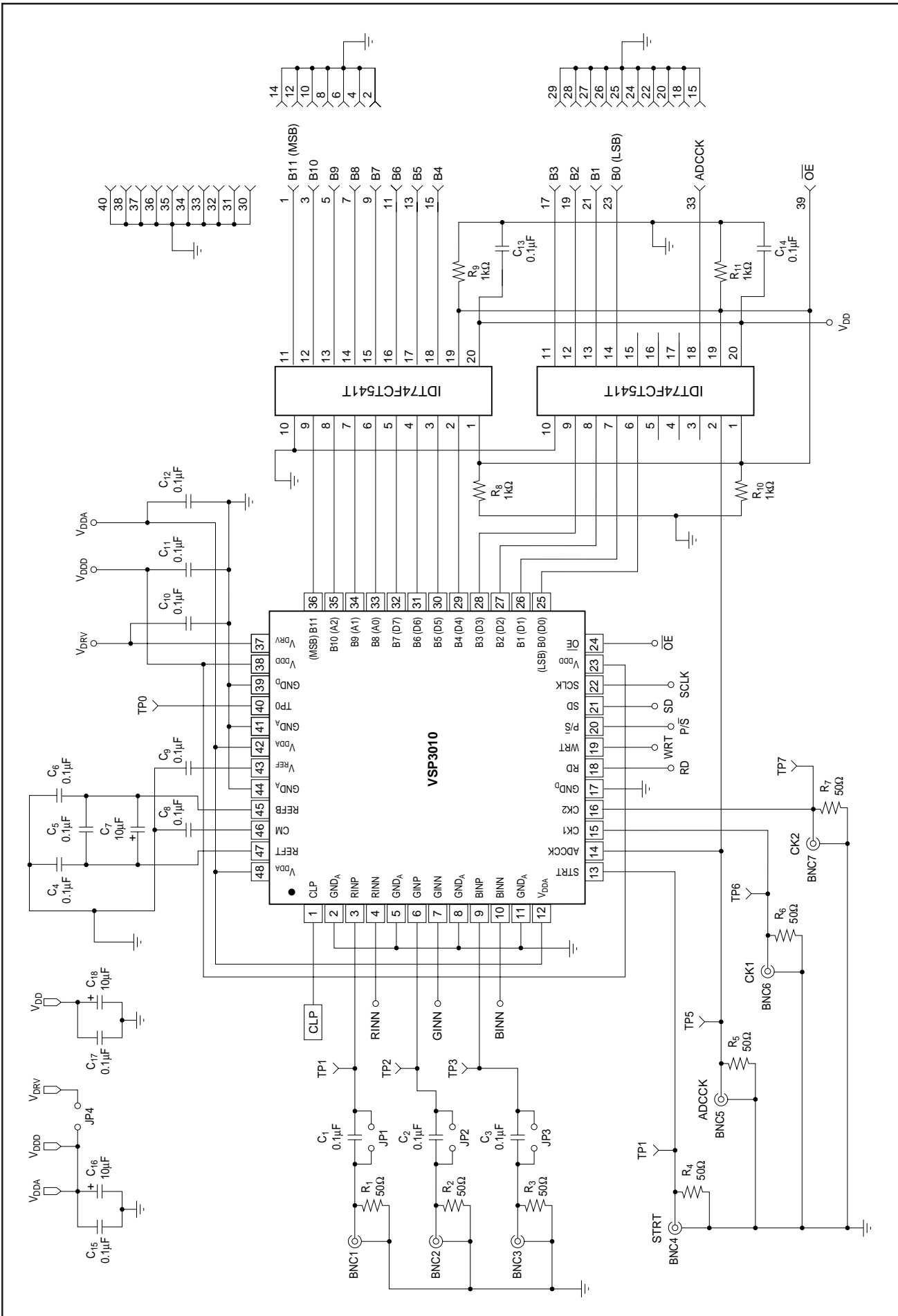


FIGURE 3. VSP3010 Evaluation Board Schematic

APPLICATION EXAMPLES

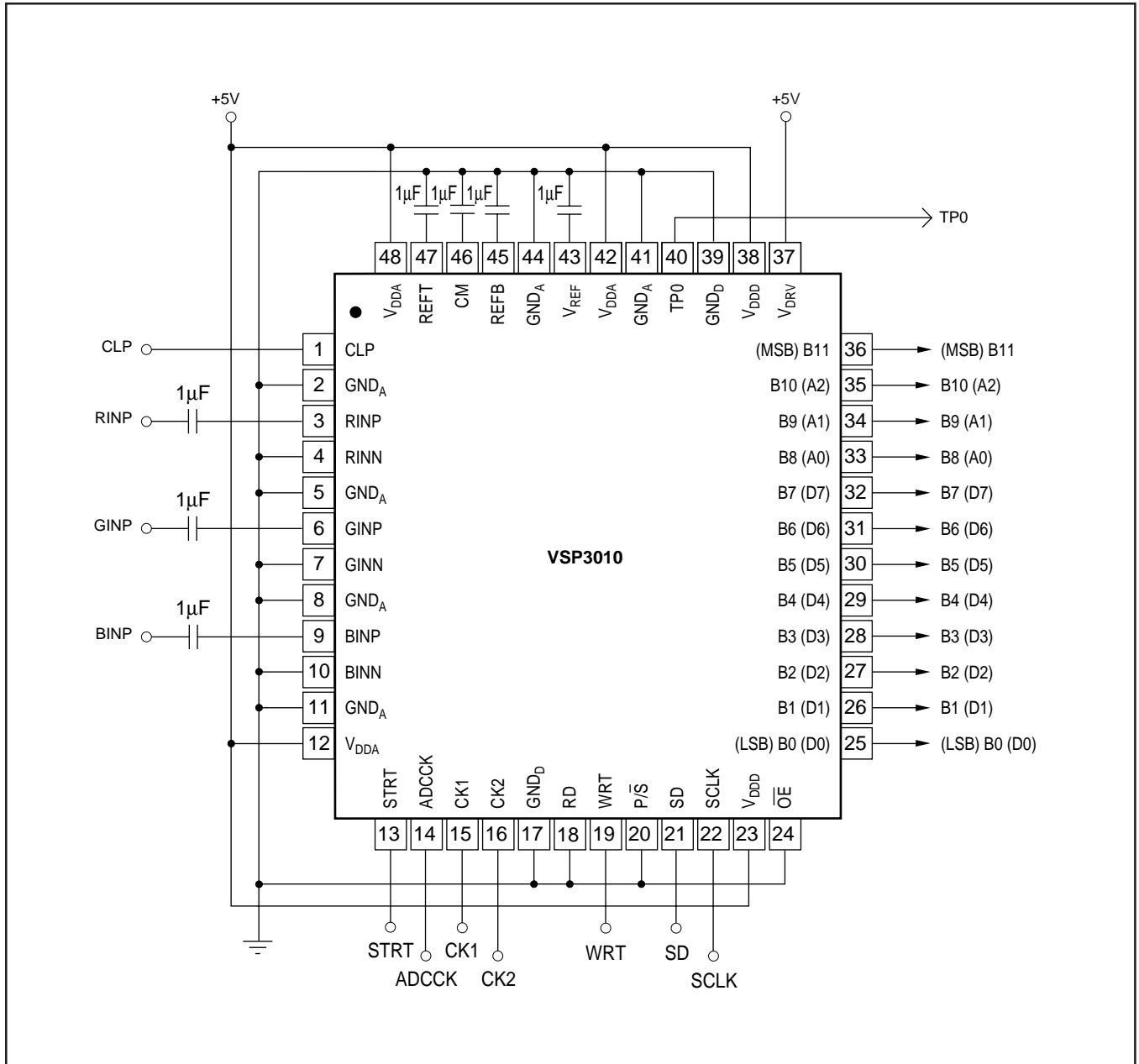


FIGURE 4. CCD Application Example.

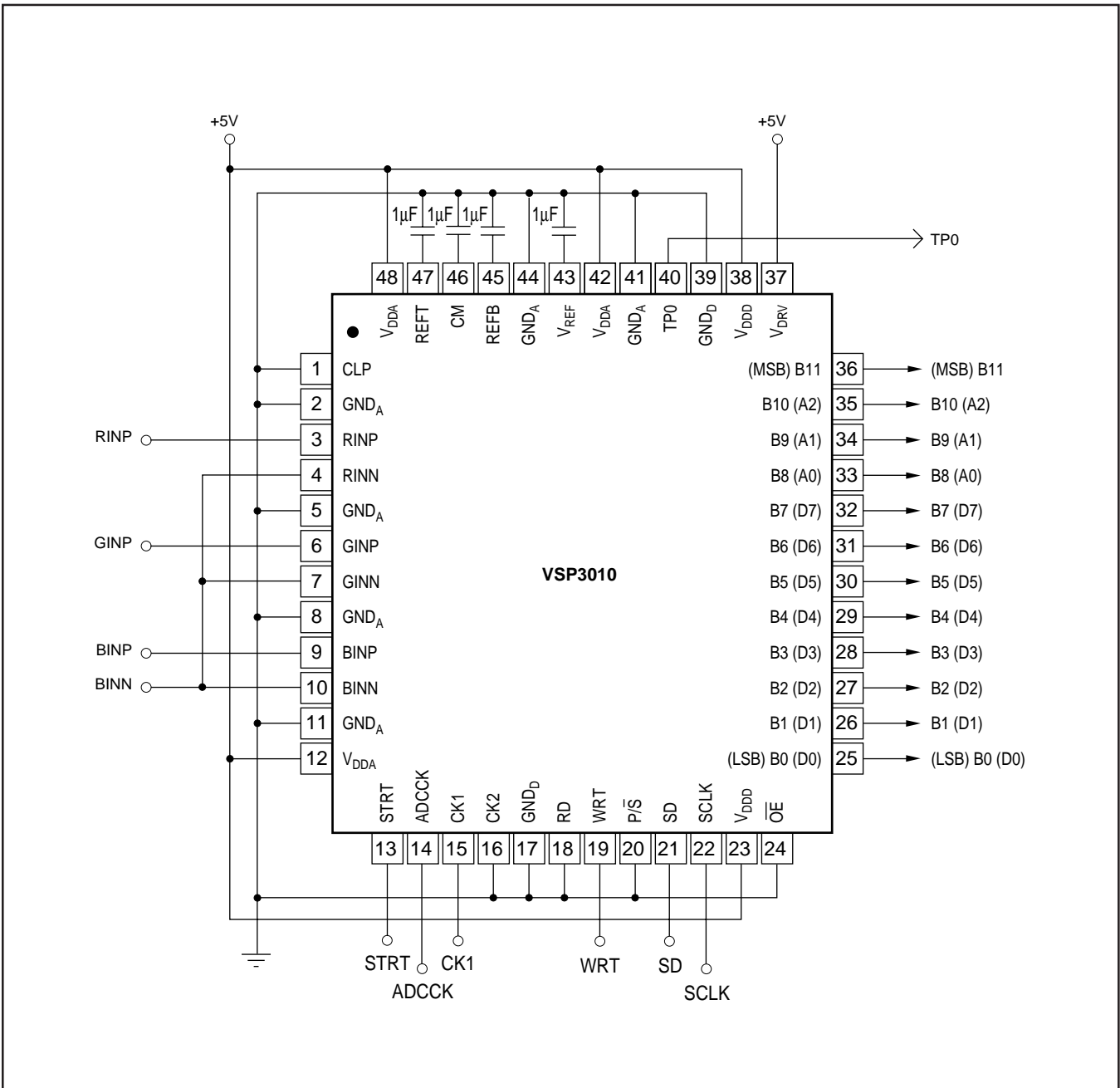


FIGURE 5. CIS Application Example.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
VSP3010Y	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
VSP3010Y/2K	ACTIVE	LQFP	PT	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
VSP3010Y/2KG4	ACTIVE	LQFP	PT	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
VSP3010YG4	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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